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Reconfigurable U-Shaped Tunnel Field-Effect Transistor

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Abstract: A reconfigurable U-shaped tunnel field-effect transistor (RUTFET) is proposed as a low-power dynamically programmable logic device. It has several advantages over conventional reconfigurable TFETs: 1) Excellent scalability without any degradation of subthreshold swing (*SS*) and drain-induced barrier thinning (DIBT) with recessed channel structure. 2) High current drivability with increased band-to-band tunneling junction 3) Scaling of *SS* with tunneling barrier width defined by geometrical parameters. In this manuscript, its electrical characteristics are examined by technology computer-aided design (TCAD) simulation. It shows ~30× higher ON-state current than control devices and 41.8 mV/dec-*SS* during drain current increase by five orders magnitude. The reconfigurable operations for *n*- and *p*-type FETs are also discussed.

Keywords: reconfigurable field-effect transistor (RFET), tunnel field-effect transistor (TFET), recessed channel, scaling down, logic device, subthreshold swing, steep switching

Classification: Electron Device

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1 Introduction

During the last few decades, scaling down of field-effect transistors (FETs) has been the main stream in microelectronics for increasing the functionality of logic devices with better performance. However, the industry as well as academia have agreed to the expectation that Moore's Law will be end-up in the near future after sub-10 nm node due to its fundamental scaling limit, increasing chip costs and power consumption [1]. A functional extension of switching elements has been regarded as an alternative approach for beyond Moore's Law by adding computational values [2]. Unlike to the conventional complementary metal-oxide-semiconductor (CMOS) devices which have static electrical functions determined during the fabrication, reconfigurable FETs (RFETs) are dynamically programmable to *n*- or *p*-type FET by changing electric signals during the operation. Thus, it is desirable for the highly adaptable logic architectures with their enhanced functionality [3] - [6].

Reducing the power consumption is another technical issue for future logic device technology. Since MOSFETs have a fundamental limit of 60 mV/dec subthreshold swing (*SS*) at room temperature, scaling supply voltage (V_{DD}) is contradictory to the high-level ON-state current (I_{ON}), however. Several alternatives have been studied to achieve sub-60 mV/dec-*SS* [7] - [9]. Among them, tunnel FETs (TFETs) have attracted a large amount of attention and been regarded as one of the most promising candidates for next-generation low-power device due to it CMOS compatibility and high scalability [9] - [21]. Recently, RFETs based on TFETs (RTFET) have been studied [22]. However, disappointing I_{ON} and random variation issues still remain as a bottleneck for the practical application of TFETs [9] - [22]. In order to address these technical issues, herein, a novel reconfigurable U-shaped TFET (RUTFET) is proposed for the first time and its electrical characteristics are examined by technology computer-aided design (TCAD) simulation, Silvaco Atlas™ [23].

2 Reconfigurable U-Shaped Tunnel Field-Effect Transistor

2.1 Features of RUTFET and TCAD simulation

Fig. 1 shows a two-dimensional (2D) schematic diagram of RUTFET. It features

buried control gate (CG) inside the U-shape recessed channel and two polarity gates (PGs) located at the outside of channel nearby source (PG1) and drain (PG2) overlapping with CG, respectively. The PGs dynamically control *n*- or *p*-type TFET operation with appropriate bias scheme. In detail, an intrinsic silicon-on-insulator (SOI) substrate is used for suppressing random dopant fluctuation (RDF) and for symmetric switching characteristics for both *n*- and *p*-type TFET operation. Considering CMOS-process compatibility titanium nitride (TiN) with 4.6 eV work function (W_{FN}) and nickel silicide (NiSi) with 4.5 eV-W_{FN} are used for gates (i.e., CG and PGs) and source/drain metals, respectively [24], [25]. In order to examine RUTFET operation, nonlocal band-to-band tunneling (BTBT), field-dependent mobility, drift-diffusion, Fermi-Dirac statistics, Schottky barrier tunneling (SBT) and lowering models are considered in TCAD simulation [23]. Detail device parameters used for simulation are listed on the Table I, unless there is any other indication.

Table I. Summary of device parameter

Parameters and Definitions	Values
PGs AND CG WORK-FUNCTION	4.6 eV
NiSi Schottky barrier height	0.45 eV
Equivalent oxide thickness (EOT) of gate dielectric	0.8 nm
PGs length (L_{PG}) and CG length (L_{CG})	20 nm
PGs height (H_{PG}) and CG height (H_{CG})	50 nm
Overlap height between PGs and CG (H_{OV})	20 nm
Underlap height between PGs and CG ($H_{UN} = H_{PG} - H_{OV}$)	30 nm
Source/drain length (L_{SD})	6 nm

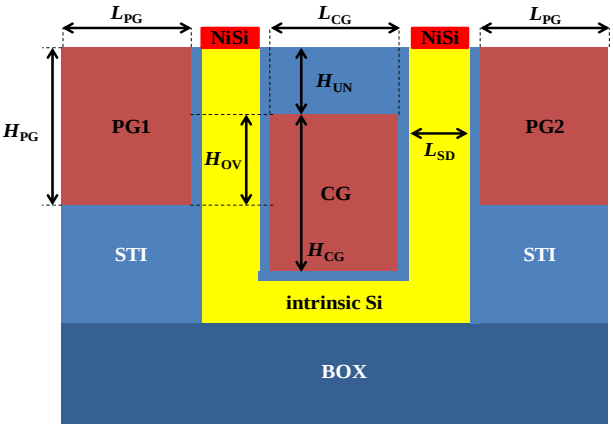


Fig. 1 Schematic structure diagram of RUTFET.

2.2 Operation mechanism

The total current of RUTFET consists of four mechanisms. Figs. 2 (b), (c) and (d) show energy band diagrams for region ①, ④ and ②, respectively during *n*-type TFET operation. In region ①, a sufficient negative PG1 voltage (V_{PG1}) allows electrons to be injected into valence band (E_V) of channel from the source (Fig. 2 (b)). If the potential difference between V_{PG1} and CG voltage (V_{CG}) is large enough,

E_V at PG1 interface and conduction band (E_C) edge at CG interface are aligned to each other and BTBT is occurred perpendicular to the channel direction (Fig. 2 (a), region ② and 2 (d)). These electrons are move toward drain side based on drift/diffusion mechanism as depicted in Fig. 2 (a), region ③. Finally, a sufficient positive PG2 voltage (V_{PG2}) pulls down the E_C and makes Schottky barrier (SB) width thin enough for intra-band tunneling (i.e., SBT) at region ④ (Fig. 2 (c)).

Fig. 3 confirms that BTBT in RUTFET is mainly occurred at CG-to-PG1 overlap region (i.e., Fig. 2 (a), region ②). Thus, an investigation on the effects of several device parameters related to the region ②, such as H_{OV}, L_{SD} and H_{UN}, are required for understanding of operation mechanism in depth and for further optimization/improvement of performance. In this simulation work, only x-direction of tunneling was calculated from hand-defined mesh. More details on this matter will be discussed in Chapter 3.

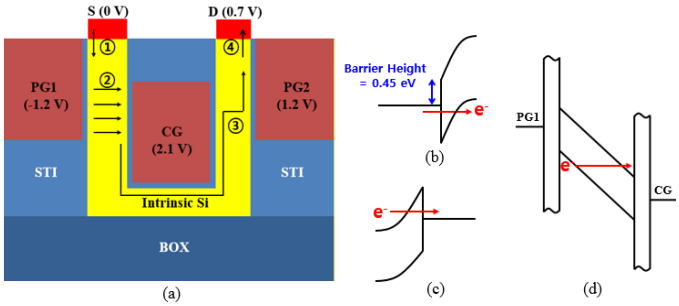


Fig. 2 Conceptual diagram for operation mechanism of RUTFET. There are four different operation regions: ① (Fig.2 (b)). SBT through E_V, ② (Fig.2 (d)). BTBT, ③ drift/diffusion and ④ (Fig.2 (c)). SBT via E_C. Band diagrams depict current flow in each region when RUTFET is turned-on (i.e., -1.2 V-V_{PG1}, 1.2 V-V_{PG2}, 2.1 V-V_{CG} and 0.7 V-drain voltage (V_D)).

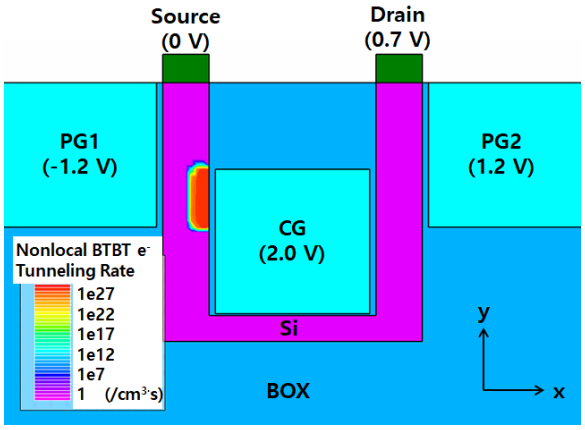


Fig. 3 Simulated BTBT electron generation rate in RUTFET.

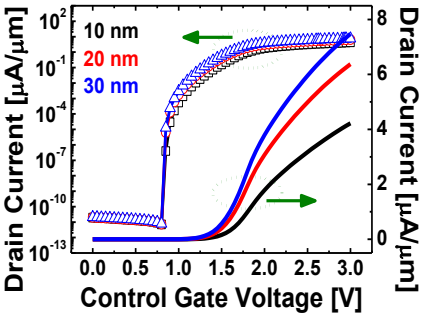


Fig. 4 The effect of H_{OV} on transfer curves. The left y-axis shows log-scale and right y-axis depicts linear-scale drain current (I_D). The H_{OV} impacts on neither *SS* nor turn-on characteristics, whereas I_{ON} linearly depends on H_{OV}. RUTFET determines it with H_{OV} irrelevant to device feature size and scaling down.

3 Results And Discussions

3.1 Effect of gate overlap height (H_{OV})

Fig. 4 shows transfer characteristics with different H_{OV} (10, 20, 30 nm). The other parameters are the same as listed in Table 1 where V_{PGS1}, V_{PGS2} and drain voltage (V_{DS}) are applied for -1.2 V, 1.2 V and 0.7 V, respectively. With a large H_{OV}, a greater I_{ON} is obtained. Thus, RUTFET can improve current drivability without any integration density penalty by adjusting H_{OV} [26]. It is attributed to the increase of BTBT junction cross-sectional area (A_{TUN}) which is determined by H_{OV} not by shallow inversion layer thickness in conventional RTFET [10] - [12], [19]. But, it is not exactly proportional to H_{OV} because as H_{OV} increases, the overall channel resistance also increases.

3.2 Effect of source/drain length (L_{SD})

Fig. 5 shows the effect of L_{SD} (i.e., length of intrinsic source/drain between PGs and CG) on transfer characteristics. In case of RUTFET, L_{SD} is corresponded to the tunneling barrier width (W_{TUN}) which is a dominant factor for *SS* as well as drain current (I_D) [33]. If L_{SD} decrease, the BTBT rate is exponentially increased which

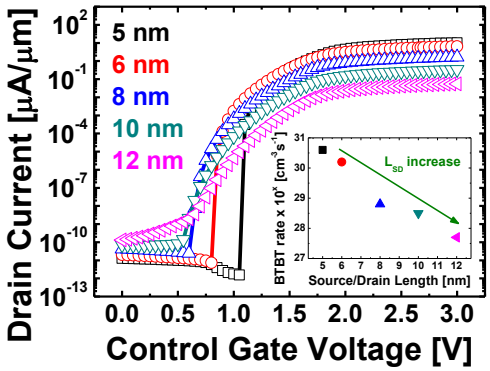


Fig. 5 Transfer characteristics with various L_{SD}.

contributes to improvements of *SS* and I_{ON} (inset of Fig. 5) [26], [27]. On the other hand, a coupling between V_{CG} and channel surface potential (ψ_S) becomes lessen due to the increase of depletion capacitance (C_D) [26]. As a result, there is a significant increase of turn-on voltage (V_{ON}) which is defined as V_{CG} when I_D starts to increase from 10^{-12} A/μm. Considering trade-off correlation between *SS*, I_{ON} and V_{ON}, the optimum L_{SD} is determined by 6 nm.

3.3 Effect of gate underlap height (H_{UN})

Fig. 6 shows transfer characteristics with a variable H_{UN} (i.e., height of underlap between PGs and CG). If the H_{UN} goes less than 20 nm, both OFF-state current (I_{OFF}) and *SS* are increased with a large amount. Although there is I_{ON} improvement, these drawbacks are problematic for RUTFET's practical low-power applications and needed to be analysed, in depth.

There are two carrier injection mechanism in SB at source-channel junction: 1) SBT and 2) thermionic emission over SB [28]. The I_{OFF} and *SS* degradations are in

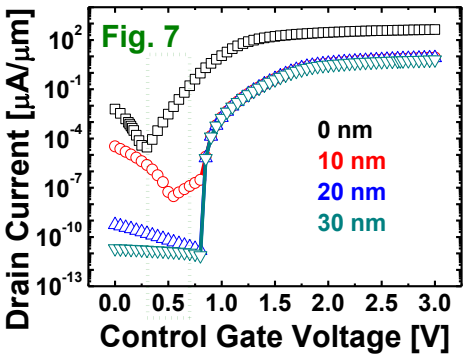
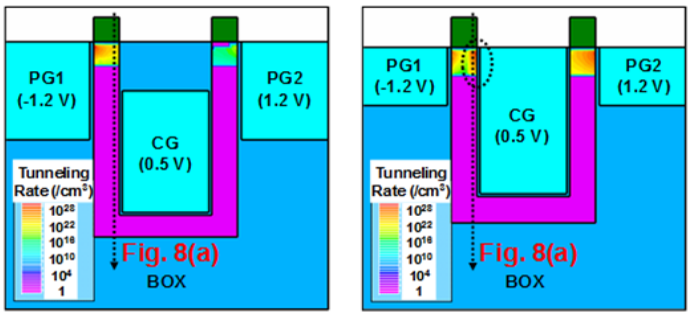
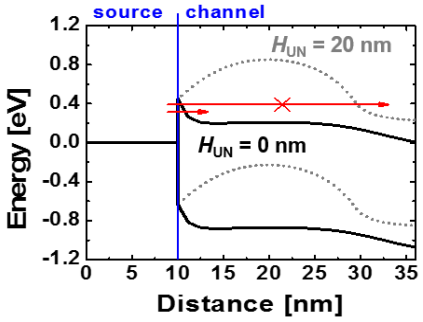


Fig. 6 The effect of H_{UN} on transfer characteristics. As H_{UN} decreases below 20 nm, there are severe degradations in terms of I_{OFF} and *SS*. These phenomena are analyzed in Figs 7-9.

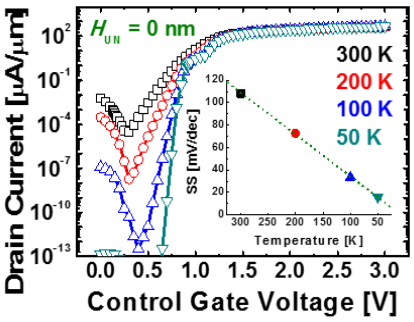


(a) (b)

Fig. 7 SBT rates for (a) 20 nm and (b) 0 nm-H_{UN} at V_{CG} = 0.5 V (i.e., olive colored box in Fig. 6). (a) If H_{UN} is large, there only exists SBT though E_V which cannot contribute to I_D (i.e., no SBT at drain junction). (b) Positively biased V_{CG} pulls down E_C at the channel that induces SBT through E_C at channel under CG.



(a)



(b)

Fig. 8 (a) Band diagrams with different H_{UN}s along the dot lines in Fig. 7. The former increase SBT while the latter increase thermionic emission. (b) Temperature (T) dependence of transfer curves for 0 nm-H_{UN}. The SS is decreased as a function of T.

part attributed to the former and in part related to the latter. Figs. 7 (a) and (b) show SBT rates under the subthreshold condition (i.e., V_{CG} = 0.5 V) with different H_{UN}s (i.e., 20 nm and 0 nm). In both cases, there are electron injections from source into channel under the PG1. Since it occurs through E_V, these electrons cannot contribute to I_D unless there is BTBT occurrence at CG-to-PG1 overlap region. On the other hand, there is another SBT at channel under CG for 0 nm-H_{UN} as shown black circled region in Fig. 6. It comes from E_V thinning with the help of positively biased CG (Fig. 8 (a)). In other word, RUTFET operates like as Schottky FET which result in higher I_{ON} but poor SS and I_{OFF}.

3.4 Scalability of RUTFET

Last of all, the scalability of RUTFET is examined by changing L_{CG}. Fig. 9 shows that RUTFET has excellent scalability without any degradation of SS and drain-induced barrier thinning (DIBT) [29 – 33] since its main channel length is defined along with vertical direction. Moreover, the I_{OFF} slightly decrease due to the decrease of SRH (Shockley–Read–Hall) current while I_{ON} increases with the

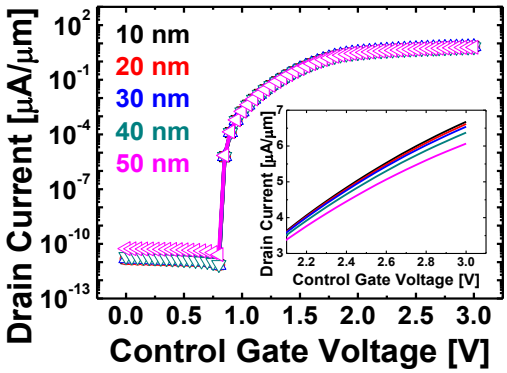


Fig. 9 The scalability of RUTFET. Transfer characteristics are plotted with the various L_{CG}s.

help of reduced channel resistance (R_{CH}). As a result, the scaling down of RUTFET guarantees better performance perfectly coincides with current device technology trends.

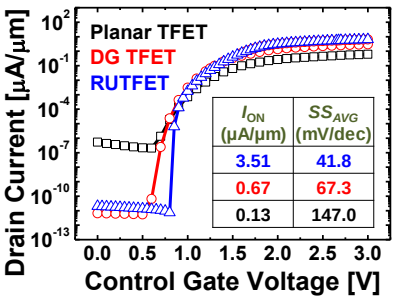
3.5 Comparison with Control Devices

Fig. 10 (a) compares transfer characteristics of RUTFET with conventional (b) planar and (c) double-gate (DG) RTFETs. For the fair comparison, average SS(SS_{AVG}) is defined as SS for five decades of I_D increase and I_{ON} is extracted for V_{CG}=V_{ON} +1.0 V. In addition, W_{fin} of DG-TFET is 6 nm same as RUTFET. RUTFET shows much better performance than the control devices in terms of both SS_{AVG} as well as I_{ON}/I_{OFF} with the help of its novel device structure which can efficiently increase A_{TUN}, decrease W_{TUN} and exclude underlaps between PGs and CG. As discussed before, it is attributed in part to the small W_{TUN} and in part to the large A_{TUN} with the help of its novel device structure. In fact, in this simulation work, only x-direction tunneling component was considered since nonlocal BTBT was calculated along with hand-defined x-directional mesh. Consequently, the SS value obtained through simulation may be overestimated. However, it can be confirmed that the proposed device has relatively superior characteristics compared to conventional devices. In addition, the simulation results are not so much overestimated because y-direction tunneling component is relatively small compared to the x-direction.

3.6 Reconfigurable operation

Conventional CMOS technology determines n-type or p-type FETs at the manufacturing stage. Instead of the conventional selective doping process, reconfigurable FET technologies can change polarity (n- or p-type) during operation by setting a polarity gate electrode (PG) bias [3] - [6]. The type of charge carrier for the conduction is determined by the appropriate gate voltage tuning at the Schottky junction of the source region. Reconfigurable FETs offer several advantages over conventional MOSFETs, such as dopant free channel which leads to less mobility degradation due to impurity scattering and immunity against RDF. They have also shown promising circuit performance by providing a fine grain

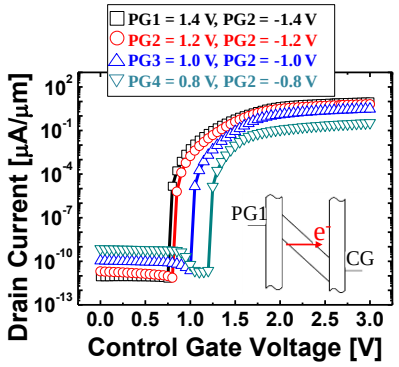
reconfiguration of various logic functions.



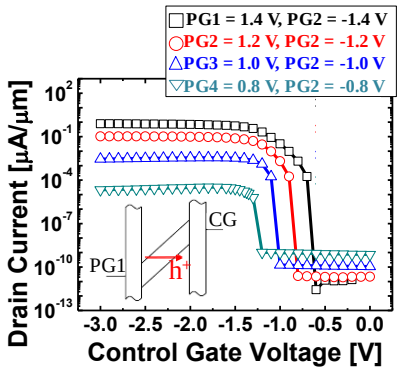
(a)

(b) (c)

Fig. 10 (a) Comparison of transfer characteristics among RUTFET, planar and DG RTFETs. The simulated structure for (b) planar and (c) DG RTFETs.



(a)



(b)

Fig. 11 Reconfigurable operation of RUTFET for (a) *n*-type and (b) *p*-type FETs.

Fig. 11 shows reconfigurable n- and p-type FET operations with different V_{PG}s. Reconfigurable operation means one device can operate as two different types, PMOS and NMOS by biasing opposite V_{PG}. As expected, RUTFET can be dynamically programmable by changing the polarities of source/drain each other. The increase of SB resistance and W_{TUN} are expected to be the main reasons for the I_{ON} decrease as the magnitude of $|V_{PG}|$ decrease. The difference between n- and p-FET is attributed to the different carrier effective mass [34]. These issues can be moderated by adopting appropriate metals for source/drain to adjust SB height and for gate to have a symmetric V_{ON} [35]. Also, it has great advantage for the highly adaptable logic architectures with distinctive functionality as mentioned in chapter 1.

4 Conclusion

RUTFET is a promising candidate for the next-generation low-power logic device with functional extension of switching features. TCAD simulation results expected RUTFET showing more than 10^{10} I_{ON}/I_{OFF} with 41.8 mV/dec-SS_{AVG} over five decades I_D increase. Further performance improvement is possible by adopting narrow band gap material(s) for channel and optimizing metals used for gate, source and drain [35]. Since deep trench, metal gate and silicide processes are highly matured techniques, RUTFET can be realized without any aggressive process capabilities to enable beyond Moore's Law.

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