



# Redox-based memristive devices for new computing paradigm

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## ABSTRACT

Memristive devices have been a hot topic in nanoelectronics for the last two decades in both academia and industry. Originally proposed as digital (binary) nonvolatile random access memories, research in this field was predominantly driven by the search for higher performance solid-state drive technologies (e.g., flash replacement) or higher density memories (storage class memory). However, based on their large dynamic range in resistance with analog-tunability along with complex switching dynamics, memristive devices enable revolutionary novel functions and computing paradigms. We present the prospects, opportunities, and materials challenges of memristive devices in computing applications, both near and far terms. Memristive devices offer at least three main types of novel computing applications: in-memory computing, analog computing, and state dynamics. We will present the status in the understanding of the most common redox-based memristive devices while addressing the challenges that materials research will need to tackle in the future. In order to pave the way toward novel computing paradigms, a rational design of the materials stacks will be required, enabling nanoscale control over the ionic dynamics that gives these devices their variety of capabilities.

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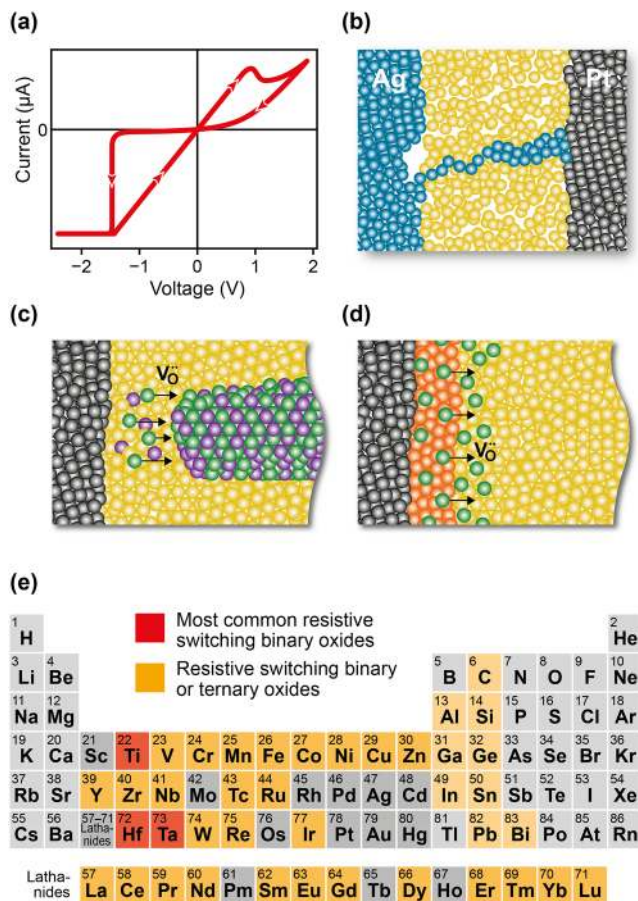
## I. INTRODUCTION

A hysteretic change in the resistance of binary transition metal oxides, as sketched in Fig. 1(a), was reported already in the 1960s.<sup>1,2</sup> Additional research activity started in the late 1990s by Asamitsu *et al.*<sup>3</sup> and Beck *et al.*<sup>4</sup> who observed similar phenomena also in complex perovskite-type oxides. However, the greatest interest in this phenomenon was triggered when it was recognized that these resistively switching cells can be described as so-called memristors<sup>5</sup> which had been predicted by Leon Chua as the fourth basic circuit element because of the conceptual symmetry with the resistor, inductor, and capacitor.<sup>6</sup> This concept was later generalized to a broader class of nonlinear, dynamical systems called memristive devices,<sup>7</sup> which describe resistive switching cells more accurately.<sup>8</sup> In the simplest case, memristive devices exhibit a change between a low resistance state (LRS) and a high resistance state (HRS) which can be interpreted as a switch between a logical “1” and “0,” respectively. However, memristive devices also

show fully analog-to-continuous changes of the resistive state with applied electrical stimulus, which enables a plethora of novel functions, data storage, and data processing. With the end of Moore’s law in mind, research on memristive devices has evolved as a major trend in the last decade. We will present the status in the understanding of the most common memristive devices as well as current and future practical applications. Based on this, we will address the challenges which materials research will have to tackle in order to pave the way toward these novel computing paradigms.

## II. MECHANISMS AND MATERIALS

A variety of different physical phenomena comprising purely electronic phenomena, multiferroic tunneling, electrochemical processes, and phase transitions can result in memristive behavior. Comprehensive review articles on the different types can be found in Refs. 9–11. The most mature memristive devices, besides the already



**FIG. 1.** (a) Current voltage-curve for bipolar switching memristive device. (b) Sketch of an ECM with Ag as electrochemically active electrode. (c) Sketch of a filamentary VCM cell. Black spheres: high work function electrode; yellow spheres: metal oxide in the fully oxidized state; green spheres: oxygen vacancies; purple spheres: metal oxide in a reduced valence state. (d) Sketch of an area-dependent VCM cell. Black spheres: high work function electrode; orange spheres: metal oxide tunnel barrier; green spheres: oxygen vacancies; yellow spheres: metal oxide in the fully oxidized state. (e) Overview of metals in the periodic table of elements whose oxides are reported to show bipolar VCM-type resistive switching either in binary form or on the B-site of  $ABO_3$  perovskites.

commercially available phase change memories, are based on redox processes which occur in conjunction with the motion of ions in ionically conducting materials. Whereas phase change memory (PCM) exhibits so-called unipolar switching, meaning that the two resistive states can be addressed with one polarity but different amplitude, redox-based memristive devices often show a so-called bipolar switching process, where different voltage polarities are needed to switch between the two resistive states [see Fig. 1(a)]. The different types of memristive systems showing bipolar switching are illustrated in Fig. 1, namely, electrochemical metallization (ECM) cells also called conductive bridge memories (CBRAM) [Fig. 1(b)] and valence change mechanism (VCM) cells [Figs. 1(c) and 1(d)]. ECM cells operate by the electrochemical dissolution of an active electrode metal such as Ag or Cu, a drift of cations through a metal

ion conductor, and a formation of a metal nanofilament. The VCM is typically found in metal oxides that show sufficient ion mobility of the host lattice such as oxygen ion or metal cation migration in metal oxides. The migration of these ions changes the local stoichiometry and, hence, leads to a redox-reaction accompanied with a valence change in the cation sublattice and a change in the electronic conductivity. This valence change usually takes place within small filaments [Fig. 1(c)] but can also be extended to the whole device area [Fig. 1(d)].

ECM cells rely on the oxidation and reduction of electrochemically active metal cations and their migration in a solid electrolyte. Different kinetic factors of the material system such as ion mobilities and redox-rates lead to different filament growth directions and switching properties.<sup>12</sup> Commonly, Cu, Ag, or their compounds are used as electrodes for injecting cations, but a variety of other metals such as Al, Au, Fe, Ni, Ta, Ti, V, and Zr have been employed as well.<sup>13</sup> The Gibbs free energy of formation of the metal/metal cation combinations is crucial for the switching properties as well as for the reliability. Solid electrolyte materials comprise poor ion conductors such as oxides ( $SiO_2$  and  $Ta_2O_5$ ) and nitrides as well as good ion-conductors such as sulfides, iodides, selenides, tellurides, and ternary chalcogenides.<sup>10</sup>

VCM-type resistive switching has been demonstrated in a large variety of binary metal oxides. Figure 1(e) highlights the elements in the periodic table of elements which have been employed as binary oxides or on the B-site of  $ABO_3$  perovskite-type complex oxide. Although many rare earth metal oxides show resistive switching, the most common materials are among the transition metal oxides. The most commonly used VCM materials are amorphous or polycrystalline binary band-insulating oxides such as  $TiO_2$ ,  $HfO_2$ , and  $Ta_2O_5$ , combined with one valve metal electrode, providing an ohmic contact and one high workfunction metal such as Pt or TiN inducing a Schottky barrier. It has been shown that these materials can exhibit highly reliable switching properties and are fairly straight-forward to grow in thin film form. However, it is important to note that the switching performance such as the resistance window between maximum and minimum resistance values, switching speed, and reliability is often not determined by the material itself but by the interplay with the interface oxide layers formed at the valve metal electrode. In order to mimic this effect, many groups are employing bilayers of different oxides in order to adjust the cell properties. It is interesting to note that bilayers of strongly oxygen deficient, n-conducting oxides or p-conducting oxides stacked with highly stoichiometric, insulating oxides often exhibit an area dependent VCM switching process<sup>14</sup> [see Fig. 1(c)] in contrast to the usually observed filamentary switching.

Besides simple binary oxides, many complex perovskite-type oxides with 3d transition metal oxides on the B-site such as titanates, manganites, ferrates, cobaltides, nickelates, and cuprates have been reported to exhibit resistive switching. Most of these materials show strong correlation effects, and it has been suggested that these will enhance the resistance change resulting from the redox-process-induced changes in the carrier concentration.<sup>15</sup> Moreover, layered oxides such as Brownmillerite-type cobaltides and ferrates contain channels of fast diffusion which offer a pathway to enhance the ionic motion in certain crystallographic directions.<sup>16</sup> Therefore, these systems provide in their single crystalline form a highly attractive

playground for basic studies on the interrelation between crystallographic orientation, ionic transport, and switching kinetics. The same holds for single model systems of more conventional memristive materials such as  $\text{TiO}_2$ <sup>17</sup> and  $\text{SrTiO}_3$ ,<sup>18</sup> which have provided deep insights into the basic switching mechanisms and the role of certain types of defects such as dislocations<sup>19</sup> or intentionally engineered phase boundaries.<sup>20</sup> However, single crystalline materials are less attractive for future computing applications than their polycrystalline or amorphous counterparts due to the required high growth temperature that is incompatible with complementary metal-oxide semiconductors (CMOSs). Complex, multicomponent materials will also face an enormous hurdle to enter industrial production lines since they have to compete with simple binary memristive oxides such as  $\text{HfO}_2$  or  $\text{ZrO}_2$  which are already available as gate-oxides in today's CMOS lines.

Significant progress has been made in the last decade with respect to the microscopic understanding of both ECM and VCM cells. This is based on the insights provided by advanced analysis tools such as synchrotron-based spectromicroscopy as well as high resolution electron microscopy and spectroscopy,<sup>21</sup> partly performed in an *in-operando* mode.<sup>22,23</sup> Moreover, physics-based compact models are available which nicely reproduce the current-voltage curves and describe the highly nonlinear switching kinetics of the filamentary systems.<sup>24</sup> On the other hand, the intense research in this field has also identified numerous processes which have been disregarded in the early days of research on these devices. It comprises processes such as the oxygen exchange with the electrodes<sup>25</sup> and the surrounding atmosphere,<sup>26</sup> the incorporation of protons<sup>27</sup> or moisture,<sup>28</sup> and the movement of metal ions in VCM cells,<sup>29</sup> which all might crucially influence both switching performance and device reliability.

### III. STATE OF THE ART

The development of filamentary VCM type memristive devices has progressed rapidly since the mid-2000s in both industry and academia. With respect to scalability, CMOS integrated planar cell sizes down to  $10 \text{ nm} \times 10 \text{ nm}$  have already been demonstrated for  $\text{HfO}_x/\text{Hf}$  ReRAM.<sup>30</sup> By employing a sidewall electrode geometry, operating  $\text{HfO}_2$ -based VCM cells with an area of  $1 \text{ nm} \times 3 \text{ nm}$  have been successfully fabricated.<sup>31</sup> Recently, well addressable cross-bar arrays of  $\text{HfO}_2$ - $\text{TiO}_x$  VCM bilayer devices with  $6 \text{ nm}$  half-pitch and  $2 \text{ nm} \times 2 \text{ nm}$  area have been demonstrated.<sup>32</sup> According to the thermally assisted ionic motion in filamentary systems in combination with the small distances which have to be overcome to move ions in the spatially confined interface region [see Fig. 1(c)], the write speed can be on the order of nanoseconds. In dedicated studies, ReRAM devices have been observed to switch as fast as  $100 \text{ ps}$ <sup>33</sup> and potentially even faster.<sup>34</sup>

Instead of striving toward the highest possible switching speed, the combination of requirements on the write operation, the read operation, and the retention time imposes a voltage time dilemma on the switching kinetics of memory cells.<sup>9</sup> The application of a write pulse (e.g.,  $3 \text{ V}$ ) during a nanosecond write time should lead to the switching process, while (in worst case) a constant train of smaller read voltage pulses (e.g.,  $0.3 \text{ V}$ ) during the retention time should not change the resistance state of the cell. A ratio of 10 between read and write voltage requires an acceleration of the switching

time of approximately  $10^{15}$  in order to guarantee a retention time of 10 years. For filamentary VCM devices, the temperature assisted, field accelerated motion of ions provides a sufficient nonlinearity of the switching kinetics in order to solve the voltage-time dilemma.<sup>35</sup> With respect to low power consumption, it has been demonstrated for TaOx based nanodevices that they can switch at sub-2-ns times under sub-2 V with less than  $10 \mu\text{A}$ , resulting in a sub-picojoule/bit operation energy.<sup>36</sup> By performing temperature accelerated lifetime tests, a retention time of 10 years has been demonstrated for a large variety of materials, e.g., in HfOx based cells.<sup>37</sup> Typically, an endurance of  $10^6$ – $10^8$  cycles is reported; however, a best performance of  $10^{12}$  cycles has been demonstrated for TaOx based VCM cells.<sup>38</sup> However, one has to note that an endurance and retention trade-off was identified for ReRAM.<sup>39</sup> Therefore, best performance in both retention and endurance has not been realized so far. A crucial issue for the commercialization of ReRAM is the cell-to-cell and cycle-to-cycle variability. According to the stochastic process of filament formation during forming and switching, variability is an inherent problem for filamentary ReRAM cells. For more detailed information about the performance of ReRAM devices, we recommend the comprehensive performance table in Ref. 40, including several material combinations published within the last years. Driven by the superior power consumption of ReRAM in comparison with flash memory, Panasonic released in 2013 the world's first mass-production of an 8-bit microcomputer with  $180 \text{ nm}$  node,  $64 \text{ kB}$  embedded ReRAM for portable healthcare products. In the meantime, Panasonic has succeeded with the fabrication of prototype ReRAM in the  $40 \text{ nm}$  node and is striving to enter the market for IoT application in the near future.<sup>41</sup> Within this context, it is important to note that the leading foundry TSMC announced to offer embedded ReRAM in combination with  $22 \text{ nm}$  FinFET technology in 2019. If this holds true, it would be a considerable breakthrough for embedded memory products based on ReRAM technology.

Although impressive advances have been obtained so far,<sup>42</sup> the storage capacity of ReRAM is still below most of the competing memory technologies such as phase change memory (PCM), spin-torque magnetic random access memory (STT-MRAM), and NAND flash.<sup>40</sup>

### IV. PROSPECTS

Information technology of the near future will be challenged by the need to provide ubiquitous computing across billions of devices and sensors as well as storage and processing for tremendous amounts of data, while being strongly constrained by energy supplies and cooling to operate it all. Memristive devices have the potential to impact these technology challenges across many dimensions. This includes substantial, although evolutionary, improvements developing higher density and higher performance data storage systems. Higher performance, 3D integrated ReRAM could extend the capabilities of today's solid-state drives, while bringing nonvolatility and higher data densities to higher memory layers could improve many application areas. Both of these would extend the lifetime of today's von Neumann computing systems. There is also the prospect to enable more revolutionary architectures that substantially reduce or eliminate most data movement, hence increasing performance and reducing energy consumption substantially. Computing



near-memory or in-memory is enabled by not only the nonvolatility of memristive devices but also their high-density integration with CMOS logic and processing elements. Looking even further out, there is interest among researchers in the suite of novel functionalities possible in memristive devices and their ability to play roles typically associated with biological synapses, neurons, axons, and other known elements of the nervous system. This section provides an outlook for how memristive devices may play various roles in pushing computing technology across time scales from today, the near future, and to much longer term. The range of computing and storage opportunities, along with materials challenges, is captured in the table in Fig. 2, while the connection to the intrinsic memristive device properties is illustrated in Fig. 3.

### A. Evolutionary: Nonvolatile and high density memory

There are many orders of magnitude in performance that separate dynamic random access memory (DRAM) from the slower primary storage devices such as hard disk drives and solid state drives (SSDs).<sup>43</sup> The holy grail for the memory industry has been to develop a new memory, a “storage class memory” (SCM), filling the gap from a performance and price-per-byte perspective. There are opportunities both to improve current solid-state drives with higher performance, as well as to bring nonvolatility to already high performance memories. In the former category, the goal has been to out-perform NAND flash technology with lower latencies in write and read times, add the feature of byte-addressability, as well as improvements in endurance that currently limit flash. Meanwhile, nonvolatile persistence is provided, same as in flash, with the aim of achieving similar data densities as well. However, as a result of the breakthroughs in 3D NAND flash technology with densities up to terabit on a single chip, much of the industry has considered it very challenging to displace flash’s incumbency in solid state drives. Therefore, the majority of IT related companies are currently considering ReRAM for embedded memory applications rather than for stand-alone memories. The chance that a 2D ReRAM approach will be able to compete on the

market is becoming increasingly unlikely and highly sophisticated 3D approaches such as the 3D X-point technology of Intel and Micron based on PCRAM will have to be developed for ReRAM in order to compete.

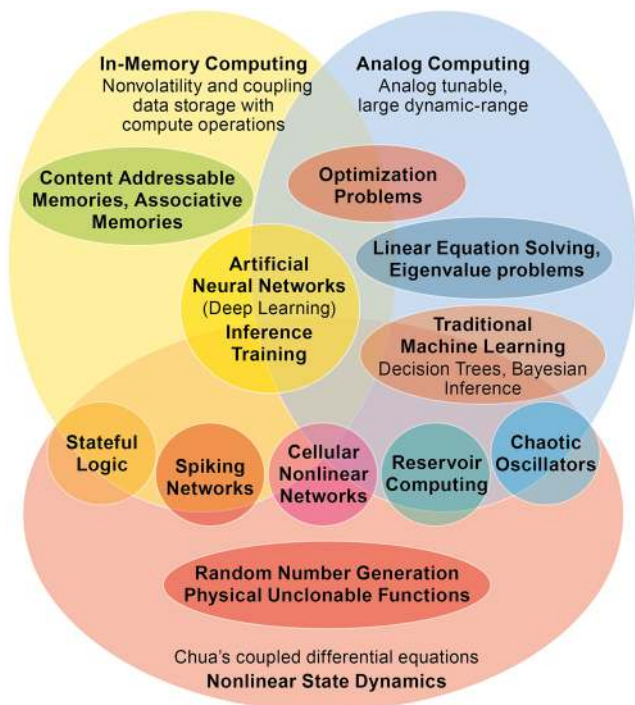
The development of a SCM with ReRAM remains attractive, as indicated in Fig. 2, and aims to bring higher total random access memory available compared to pure DRAM, while also introducing nonvolatility. It is important to note that all stand-alone memory approaches discussed here will continue to undergo the most aggressive pitch scaling and cost reduction pressures among all possible data storage applications. Nonetheless, for many computational workloads, the increased nonvolatile data available from an SCM enable applications to keep local and fast access to data instead of fetching from an SSD or even slower hard disk drives. With adjustments to the overlying software to exploit the SCM persistence, performance gains of 50× are possible.<sup>44</sup> In order for these higher performance SSDs or nonvolatile SCMs to be realized, improvements and engineering are required in the ReRAM technology.

### B. Revolutionary: Advanced and neuromorphic architectures

Even as memristive devices may enable the creation of extra tiers between memory and storage, it has become clear that this cache/memory/storage hierarchy itself cannot fully address the bottlenecks in today’s computing systems. The challenge is that memory performance growth has not kept pace with that of processors. This gap is referred to as the “memory wall,”<sup>45</sup> and it is exacerbated by the von Neumann arrangement that separates the central processing unit (CPU) and memory. The data movement between these units costs time and energy, and new architectures that can reduce such movement are desired. Thus, a revolution is gaining steam in the computing architecture community to overturn von Neumann’s layout wherever possible. As noted by Hennessy and Patterson in their Turing award lecture,<sup>46</sup> the fact that exponential gains in computing performance have slowed from a doubling

Technological Opportunity		Memristive Materials Challenges	Computing Applications	Potential Gains	Refs
Storage-class memory, nonvolatile, higher density local memory		Foundry compatible processing; higher performance read and write; Lower retention acceptable; Improved endurance;	General Purpose Computing	1.5–50 ×	44
Novel Functions: Random Number Generation, Physical Unclonable Function, Content Addressable Memory (CAM)		Control of variability, stochasticity, dynamics	General Purpose Computing, IoT, Security, Networking	2–50 ×	64, 77–78
Advanced Architectures	Near-memory computing	Conductance range and multilevel are desirable; 3D and area scaling; Improved endurance;	General Purpose, Data bandwidth intensive	2–100 ×	51
	In-memory computing	Conductance range and multilevel are critical; 3D and area scaling; Integration with logic and processing elements; Improved endurance;	General Purpose, Data bandwidth intensive, graph analytics, search	10–100 ×	52–56
Neuromorphic Architectures	Accelerate Today’s Machine Learning	Programming asymmetry, nonlinearity, variability; low current;	Artificial Neural Networks, Signal processing, Sci. computing	10–1,000 ×	60–63, 65–68
	Bio-inspired Systems	Low current; some variability and stochasticity tolerable; Nonvolatile (synaptic) and volatile (neuron) device properties	Robotics, Multimodal sensor processing; cognitive reasoning;	≥ 1,000 ×	69–75

FIG. 2. Prospects and opportunities for memristive devices in computing technologies, spanning near and far terms.



**FIG. 3.** Memristive devices offer at least three main types of computing applications: in-memory computing, analog computing, and nonlinear state dynamics. In-memory operations utilize the nonvolatility and ability to couple compute operations with the data, such as through Ohm's law to perform multiplication. Extremely data-heavy applications, such as artificial neural networks, take advantage of this by reducing the amount of data movement compared to out-of-memory (von Neumann) architectures. Analog computing leverages the large dynamic range of conductance, and the ability to finely tune to stable intermediate conductance values. This can be utilized, for example, in constructing analog circuits that solve linear systems of equations in constant rather than polynomial time.<sup>62</sup> Finally, the history-dependence intrinsic to memristors is described by Chua's coupled differential equations and drives highly nonlinear dynamics and the capability for "local activity." This can be used in spiking neural networks, cellular nonlinear networks, random number generators, and chaotic oscillators.

every 1.5 years to currently doubling every 20 years (or more) opens up a "new golden age for computer architecture." The other fuel to this revolution is the explosion in several types of computing workloads for which the traditional computing architecture is poorly suited, namely, artificial neural networks (ANN), and especially the large deep learning<sup>47</sup> networks that have matched or surpassed human level capabilities in such areas as image and audio processing, language translation, and several competitive strategy games. As these networks grow in size, the computing resources to train and deploy them grow well beyond what is reasonable with current computing systems.<sup>48</sup>

Memristive devices offer many key advantages that may be exploited in novel architectures to achieve higher performance and enhanced capabilities. Figure 3 gives a high-level overview for three of the key memristive properties that offer novel computing advantages, as well as some example application areas that exploit these

properties. These are not comprehensive but meant to illustrate a connection between intrinsic device properties and some important application areas. As noted above, the main challenge in the present-day von Neumann layout is the dependence of processing units on data arriving through the bus from a distant memory. Near-memory computing approaches aim to supply higher density and higher performance memory as close to the processing units as possible.<sup>49</sup> This has the benefit of minimizing the changes to current computing systems, focusing on high density memory integration, but not fully addressing the memory wall. In contrast, efforts at in-memory computing<sup>50–53</sup> seek to colocate computing with memory and thereby eliminate the von Neumann bottleneck. The gains can be tremendous, but this involves changes to both the memories and the computing units themselves, with a method to couple the data storage with the data processing. Memristive devices, where data are stored in the conductance of a cell and may be reprogrammed depending on the voltage applied, offer many options<sup>54</sup> to provide such coupling. This is illustrated in the leftmost oval of Fig. 3 along with some applications. It becomes possible, for example, for write operations performed on one memristor cell to depend on the conductance of another, for example, thereby performing "stateful" logic operations.<sup>55–57</sup> This takes advantage of the nonvolatility of memristive devices and can bring power savings, but such applications also favor reprogramming endurance to be far beyond what has been demonstrated to date. Other forms of in-memory computing can take advantage of the analog nature of memristive devices, illustrated in the rightmost oval of Fig. 3. These can also operate in a "read" mode, dramatically reducing the endurance requirements. An example is performing important multiplication and addition (or MAC) operations directly in large resistive arrays. Such operations are costly in the digital domain, but massive parallelism is possible by taking advantage of Ohm's law to perform the multiplication between a set of input voltages and programmed conductances in an array and leveraging Kirchoff's law for summing the currents. This can perform vector-matrix multiplications in a single compute cycle, which are the dominant operations performed in modern neural networks.<sup>58–61</sup> Another exciting example is solving linear systems of equations and eigenvalue/eigenvector problems directly in analog crossbar arrays in constant time,<sup>62</sup> even surpassing quantum approaches. Other implementations use the nonvolatility of memristive devices to lower the power in building content addressable memories,<sup>63</sup> which have applications in network routing and security. Finally, by also leveraging the dynamics and reprogrammability of memristive devices (bottom oval in Fig. 3), it is possible, for example, to accelerate the costly training of large neural networks. Here, the full back-propagation algorithm is accelerated dramatically, including the tuning of the synaptic weights that are encoded in memristive devices, as well as the above matrix computations.<sup>64–67</sup>

While significant progress has been made using modern neural networks to solve many important classification tasks, there remains a significant distance to cover to match the feats performed by humans and other mammals in processing visual, auditory, tactile, and other sensory input in real-time. Responding to novel and unpredictable environments by enacting complex movements is unparalleled by artificial systems. Simultaneously, such biological computations and actuations are performed while operating well below 100 Watts of power consumption. Thus, there

are significant efforts to understand enough of how brains compute to leverage this know-how in designing future “biologically inspired” systems. It may result that altogether new computing approaches are developed that do not strictly follow the path nature has followed. Nonetheless, mimicking many of the currently known functionalities and elements in biological nervous systems, including neurons, axons, synapses, etc., is of interest at a bare minimum in order to improve our understanding. Simulating the hundreds of billions of neurons (with hundreds of different neuron types) and the 1000–10 000 synapses for each neuron is far beyond the capability of today’s supercomputers. Yet, this tremendous connectivity and scale are believed to be a crucial aspect of the computing power in biological systems. Part of the excitement in memristive devices stems from the strong analogies between the biological computing elements and memristors.<sup>68,69</sup> In addition to the clear analogies to synapses,<sup>70</sup> the spiking neuronlike behavior is also observed,<sup>71</sup> as well as axonlike transmission of signals<sup>72</sup> and the diffusive interactions with neurotransmitters.<sup>73,74</sup> Many of these functionalities stem from the nonlinear state dynamics in memristive devices (bottom oval in Fig. 3), and while there is a rich history in implementing such functionalities in CMOS elements,<sup>75</sup> memristive devices offer a promising approach that may take orders of magnitude fewer elements to achieve similar functionality. Additionally, many of the device challenges such as variability and stochastic responses may not be significant obstacles when mimicking the highly unreliable neuronal firing, for example. Such randomness may, in fact, provide a valuable computing resource, allowing the system to explore a larger optimization landscape, avoid overfitting, and enable generalization and abstraction. It is notable that true random number generation can be expensive to achieve in digital systems, yet inexpensive and fast in memristive systems.<sup>76,77</sup> There are many open questions in the area of biophysical computing, and memristive devices offer the potential to build scaled-up emulation platforms that would otherwise take orders of magnitude more CMOS elements to construct. Whether such emulation platforms would be trained by interacting with environmental stimulus, or would be cloned based on other trained systems, re-programmability and yield would still be critical properties of the memristive devices. To reach the tremendous network sizes with hundreds of billions of neurons and several orders of magnitude more synapses, incredible densities using 3D integration will be critical, along with low power enabled by low current operation. On the other hand, many of the key requirements for shorter term technological opportunities, such as endurance and even multilevel capabilities, may be significantly relaxed. This is an exciting prospect as it means that conquering many of today’s challenges in memristive devices may be the hardest ones faced, with the rewards being not just improved memories and storage but also higher performance computing and the ability to control and understand biological cognition itself.

## V. CHALLENGES

For all fields of applications, further improvements in ReRAM technology are required. Most importantly, the cell-to-cell and cycle-to-cycle variabilities must achieve high volume manufacturing thresholds to be commercialized. While ReRAM technology shows overall favorable scaling down to the single-digit

nanometer dimensions of CMOS nodes, however, it has to be clarified if these dimensions may exacerbate the impact of atomic-scale sources of variability. Higher data densities must be achieved through 3D fabrication approaches, as well as nonlinear selector devices that eliminate sneak path currents.<sup>78</sup> Controlled engineering and processing as well as gaining control over ionic motion on the nanoscale will be required to meet these challenges.

### A. Handling trade-offs

Although best performance has been shown for memristive devices with respect to switching speed, low power dissipation, scalability, endurance, and retention, these properties have not been shown on the same devices. For the most common filamentary VCM and ECM systems, there exist several trade-offs, such as between retention and endurance.<sup>39</sup> This is related to the fact that devices with softly formed filaments and comparably low  $R_{ON}/R_{OFF}$  ratios are more sensitive to slight variations in the number of oxygen vacancies and thereby can show a worse retention. In turn, devices with strongly formed filaments and large  $R_{ON}/R_{OFF}$  ratios suffer much more from repeated cycling than small filaments. It is important to note that reliability issues such as the switching voltage variability and failure rates are improved while scaling down the devices in the submicrometer range down to 25 nm.<sup>79</sup> However, it is conceivable that further shrinking to the scale of a few nanometers may exacerbate atomic-scale sources of variability. In general, area dependent VCM systems show a much smaller cycle-to-cycle variability due to the lack of a stochastic filament formation process and a less sharp SET process which could be advantageous to establish analog switching. However, due to the lack of Joule-heating in these systems, the  $R_{ON}/R_{OFF}$  ratios are on the order of 10 or even lower. Moreover, due to the less pronounced influence of Joule-heating, the switching kinetics are expected to be less nonlinear, possibly resulting in inferior retention times and switching speeds compared to filamentary systems. This might also hold true for the softly addressed intermediate states of filamentary analog switching devices. Some of the trade-offs could possibly be eliminated in the future by exploring novel materials and/or novel material combinations. However, the different applications mentioned in Sec. IV have very different requirements with respect to variability, switching speed, retention time, and endurance (see the summary in Fig. 2). It is therefore more straight forward to tailor the materials stacks to the specific application instead of striving toward a single materials solution for all applications. As mentioned in Sec. IV, rather than fighting variability, the randomness of the ionic switching process of memristive devices may be employed to enhance the computational abilities of certain neural networks. Moreover, due to an endurance-retention trade-off, devices with poor retention may offer better endurance, which is key for the write-intensive training phase. Once the neural network converges, information can be stored more permanently, either through stronger programming<sup>80,81</sup> or by employing different materials such as the choice in electrode.<sup>81</sup> It has furthermore been shown that the time constants of volatile VCM-type devices may be tailored by engineering the electrode interfaces.<sup>82–84</sup> Tailoring the volatility of memristive devices offers the ability to match varying time constants needed in artificial neural networks or to toggle between synapselike or neuronlike functions.<sup>81</sup>



## B. Gaining control over ionic motion on the nanoscale

As a result of the need for ultimate scaling and improved reliability in devices which are based on the motion of ionic species, it will be mandatory to gain control over ionic motion on the atomic scale. This comprises the control over (i) which ionic species move in a given materials stack, (ii) how fast they move during the write procedure, and (iii) how long they stick to their position during read-out. This will require a control of the chemical composition, the electrostatic potentials, and the temperature at the atomic scale, resulting in a well defined redox-reaction rate between the different involved species. To this end, a rational stacking of building bricks of different materials (see the sketch in Fig. 4) has to be employed to tailor the energetic landscape of ionic defects and their motion on the one hand. On the other hand, the metal electrodes and/or their interfaces have to be tailored in order to provide both sufficient Joule heating and solubility of the active ionic species. Figure 4 summarizes a selection of building brick material's parameters which have to be combined within the memristive device stack to tailor the device properties such as switching speed, resistance values, switching, and forming voltages as well as retention and endurance. It is important to note that the material's properties do not combine in a linear fashion but have strong nonlinear couplings that require a system-whole analysis after exchanging a single building brick.

Systematic variations of the material's parameters such as the oxygen vacancy concentration of the oxide,<sup>85</sup> the difference in oxygen formation energy of the interface oxide,<sup>25</sup> and the mobility of certain ionic species<sup>83</sup> have been performed and their impact on the forming voltages, the switching speed, and certain devices failures has been identified. Although it is intuitively expected that a high ion mobility is beneficial for fast switching memristive devices, it will at the same time result in short retention times if the underlying rate-determining step in the switching process lacks the required strong nonlinearity to solve the voltage-time-dilemma. A rational design of device properties as proposed in Fig. 4 is furthermore impeded by the fact that the exact material's parameters in a given configuration are often unknown since the material's properties in ultrathin or even amorphous layers might strongly differ from their bulk values. Even the defect concentration in thin films grown at nonequilibrium

conditions is far away from the values of bulk materials in thermal equilibrium, and confinement effects might come into play. Therefore, strong efforts are needed to combine systematic experiments with multiscale modeling ranging from *ab initio*<sup>86</sup> to continuum simulations of materials. Finally, in order to implement memristive devices into the different computing approaches mentioned in Sec. IV, suitable compact models are requisite to enable a reliable circuit design.

## VI. CONCLUSIONS

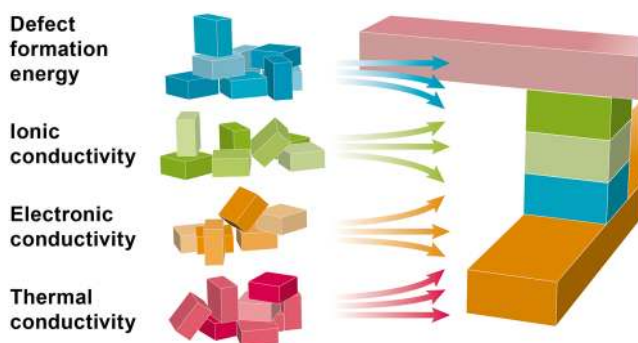
Redox-based memristive devices have the potential to be employed for a plethora of applications in information technology. This includes evolutionary improvements developing higher density and higher performance data storage systems to extend the lifetime of today's von Neumann computing systems. Besides this, they will enable revolutionary computing architectures such as in-memory computing and bio-inspired, neuromorphic computing. ReRAM technology has strongly advanced over the past 5 years. Sub-nanosecond switching, high integration densities, and first approaches for 3D stacking have been demonstrated for prototypical ReRAM systems, and no fundamental limits to use ReRAM for highly integrated data storage applications have been identified so far. However, there exist several trade-offs which could be eliminated in the future by exploring new materials and/or new material combinations. However, one should keep in mind that industrial groups have focused so far on materials which have already been introduced in their CMOS-lines, such as HfO<sub>2</sub> and Ta<sub>2</sub>O<sub>5</sub>. Therefore, a considerable threshold of performance improvement has to be overcome in order to justify the introduction of novel, more complex materials. Besides this, a large amount of processing and integration issues, in particular, with respect to 3D integration, will have to be addressed in the future for ReRAM to become competitive with both conventional and alternative emerging data storage technologies.

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## REFERENCES

- G. Dearnaley, A. M. Stoneham, and D. V. Morgan, "Electrical phenomena in amorphous oxide films," *Rep. Prog. Phys.* **33**, 1129–1191 (1970).
- D. P. Oxley, "Electroforming, switching and memory effects in oxide thin films," *Electrocomponent Sci. Technol.* **3**, 217–224 (1977).
- A. Asamitsu, Y. Tomioka, H. Kuwahara, and Y. Tokura, "Current switching of resistive states in magnetoresistive manganites," *Nature* **388**, 50–52 (1997).
- A. Beck, J. G. Bednorz, C. Gerber, C. Rossel, and D. Widmer, "Reproducible switching effect in thin oxide films for memory applications," *Appl. Phys. Lett.* **77**, 139–141 (2000).
- D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature* **453**, 80–83 (2008).
- L. Chua, "Memristor—the missing circuit element," *IEEE Trans. Circuit Theory* **18**, 507–519 (1971).
- L. Chua and S. Kang, "Memristive devices and systems," *Nature* **64**, 209–223 (1976).



**FIG. 4.** Sketch of a rational design of memristive device stacks: materials (oxides or metals) with different properties have to be combined in order to tailor the ionic motion on the nanoscale.



- <sup>8</sup>Resistive Switching—From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications, edited by D. Ielmini and R. Waser (Wiley-VCH, 2016).
- <sup>9</sup>R. Waser, R. Dittmann, G. Staikov, and K. Szot, “Redox-based resistive switching memories—Nanoionic mechanisms, prospects, and challenges,” *Adv. Mater.* **21**, 2632–2663 (2009).
- <sup>10</sup>M. N. Kozicki, M. Mitkova, and I. Valov, *Electrochemical Metallization Memories* (Wiley, 2016), Chap. 17, pp. 483–514.
- <sup>11</sup>D. S. Jeong and C. S. Hwang, “Nonvolatile memory materials for neuromorphic intelligent machines,” *Adv. Mater.* **30**, 1704729 (2018).
- <sup>12</sup>Y. Yang, P. Gao, L. Li, X. Pan, S. Tappertzhofen, S. Choi, R. Waser, I. Valov, and W. D. Lu, “Electrochemical dynamics of nanoscale metallic inclusions in dielectrics,” *Nat. Commun.* **5**, 4232–1–4232–9 (2014).
- <sup>13</sup>M. Lübben and I. Valov, “Active electrode redox reactions and device behavior in ECM type resistive switching memories,” *Adv. Electron. Mater.* **5**, 1800933 (2019).
- <sup>14</sup>A. Sawa and R. Meyer, “Interface type switching,” in *Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications*, edited by D. Ielmini and R. Waser (Wiley, 2016).
- <sup>15</sup>A. Palau, A. Fernandez-Rodriguez, J. C. Gonzalez-Rosillo, X. Granados, M. Coll, B. Bozzo, R. Ortega-Hernandez, J. Sune, N. Mestres, X. Obradors, and T. Puig, “Electrochemical tuning of metal insulator transition and nonvolatile resistive switching in superconducting films,” *ACS Appl. Mater. Interfaces* **10**, 30522–30531 (2018).
- <sup>16</sup>A. Khare, D. Shin, T. S. Yoo, M. Kim, T. D. Kang, J. Lee, S. Roh, I. Jung, J. Hwang, S. W. Kim, T. W. Noh, H. Ohta, and W. S. Choi, “Topotactic metal-insulator transition in epitaxial SrFeO<sub>x</sub> thin films,” *Adv. Mater.* **29**, 1606566 (2017).
- <sup>17</sup>R. J. Kamaladasa, A. A. Sharma, Y. T. Lai, W. Chen, P. A. Salvador, J. A. Bain, M. Skowronski, and Y. N. Picard, “In situ TEM imaging of defect dynamics under electrical bias in resistive switching rutile-TiO<sub>2</sub>,” *Microsc. Microanal.* **21**, 140 (2017).
- <sup>18</sup>H. Du, C. Jia, A. Koehl, J. Barthel, R. Dittmann, R. Waser, and J. Mayer, “Nanosized conducting filaments formed by atomic-scale defects in redox-based resistive switching memories,” *Chem. Mater.* **29**, 3164–3173 (2017).
- <sup>19</sup>K. Szot, W. Speier, G. Bihlmayer, and R. Waser, “Switching the electrical resistance of individual dislocations in single-crystalline SrTiO<sub>3</sub>,” *Nat. Mater.* **5**, 312–320 (2006).
- <sup>20</sup>S. Cho, C. Yun, S. Tappertzhofen, A. Kursumovic, S. Lee, P. Lu, Q. Jia, M. Fan, J. Jian, H. Wang, S. Hofmann, and J. L. MacManus-Driscoll, “Self-assembled oxide films with tailored nanoscale ionic and electronic channels for controlled resistive switching,” *Nat. Commun.* **7**, 12373 (2016).
- <sup>21</sup>C. Lenser, R. Dittmann, and J.-P. Strachan, “Valence change observed by nanospectroscopy and spectromicroscopy,” in *Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications*, edited by D. Ielmini and R. Waser (Wiley, 2016).
- <sup>22</sup>D. Cooper, C. Baeumer, N. Bernier, A. Marchewka, C. L. Torre, R. E. Dunin-Borkowski, S. Menzel, R. Waser, and R. Dittmann, “Anomalous resistance hysteresis in oxide ReRAM: Oxygen evolution and reincorporation revealed by in situ TEM,” *Adv. Mater.* **29**, 1700212 (2017).
- <sup>23</sup>C. Baeumer, C. Schmitz, A. Marchewka, D. N. Mueller, R. Valenta, J. Hackl, N. Raab, S. P. Rogers, M. I. Khan, S. Nemsak, M. Shim, S. Menzel, C. M. Schneider, R. Waser, and R. Dittmann, “Quantifying redox-induced Schottky barrier variations in memristive devices via in operando spectromicroscopy with graphene electrodes,” *Nat. Commun.* **7**, 12398 (2016).
- <sup>24</sup>JART, “Juelich Aachen resistive switching tools (JART),” 2019, <http://www.emrl.de/JART.html>.
- <sup>25</sup>W. Kim, S. Menzel, D. J. Wouters, Y. Guo, J. Robertson, B. Rösger, R. Waser, and V. Rana, “Impact of oxygen exchange reaction at the ohmic interface in Ta<sub>2</sub>O<sub>5</sub>-based ReRAM devices,” *Nanoscale* **8**, 17774–17781 (2016).
- <sup>26</sup>T. Heisig, C. Baeumer, U. N. Gries, M. P. Mueller, C. L. Torre, M. Lübben, N. Raab, H. Du, S. Menzel, D. N. Mueller, C.-L. Jia, J. Mayer, R. Waser, I. Valov, R. A. D. Souza, and R. Dittmann, “Oxygen exchange processes between oxide memristive devices and water molecules,” *Adv. Mater.* **30**, 1800957 (2018).
- <sup>27</sup>T. Tsuruoka, I. Valov, C. Mannequin, T. Hasegawa, R. Waser, and M. Aono, “Humidity effects on the redox reactions and ionic transport in a Cu/Ta<sub>2</sub>O<sub>5</sub>/Pt atomic switch,” *Jpn. J. Appl. Phys., Part 2* **55**, 06GJ09 (2016).
- <sup>28</sup>I. Valov and T. Tsuruoka, “Effects of moisture and redox reactions in VCM and ECM resistive switching memories,” *J. Phys. D: Appl. Phys.* **51**, 413001 (2018).
- <sup>29</sup>A. Wedig, M. Lübben, D.-Y. Cho, M. Moors, K. Skaja, V. Rana, T. Hasegawa, K. Adepalli, B. Yildiz, R. Waser, and I. Valov, “Nanoscale cation motion in Ta<sub>x</sub>, Hf<sub>x</sub>, and Ti<sub>x</sub> memristive systems,” *Nat. Nanotechnol.* **11**, 67–74 (2016).
- <sup>30</sup>B. Govoreanu, G. S. Kar, Y.-Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I. P. Radu, L. Goux, S. Clima, R. Degraeve, N. Jossart, O. Richard, T. Vandeweyer, K. Seo, P. Hendrickx, G. Pourtois, H. Bender, L. Altimime, D. J. Wouters, J. A. Kittl, and M. Jurczak, “10 × 10 nm<sup>2</sup> Hf-HfO<sub>x</sub> crossbar resistive ram with excellent performance, reliability and low-energy operation,” in *2011 IEEE International Electron Devices Meeting—IEDM '11* (IEDM Technical Digest, 2011), pp. 31.6.1–31.6.4.
- <sup>31</sup>K.-S. Li, C. Ho, M.-T. Lee, M.-C. Chen, C.-L. Hsu, J. Lu, C. Lin, C. Chen, B. Wu, Y. Hou, C. Lin, Y. Chen, T. Lai, M. Li, I. Yang, C. Wu, and F.-L. Yang, “Utilizing sub-5 nm sidewall electrode technology for atomic-scale resistive memory fabrication,” in *2014 Symposium on VLSI Technology* (Digest of Technical Papers, 2014), p. 2.
- <sup>32</sup>S. Pi, C. Li, H. Jiang, W. Xia, H. Xin, J. J. Yang, and Q. Xia, “Memristor crossbar arrays with 6 nm half-pitch and 2 nm critical dimension,” *Nat. Nanotechnol.* **14**, 35–39 (2019).
- <sup>33</sup>A. C. Torrezan, J. P. Strachan, G. Medeiros-Ribeiro, and R. S. Williams, “Sub-nanosecond switching of a tantalum oxide memristor,” *Nanotechnology* **22**, 485203 (2011).
- <sup>34</sup>S. Menzel, M. von Witzleben, V. Havel, and U. Boettger, “The ultimate switching speed limit of redox-based resistive switching devices,” *Faraday Discuss.* **213**, 197 (2018).
- <sup>35</sup>S. Menzel, M. Waters, A. Marchewka, U. Böttger, R. Dittmann, and R. Waser, “Origin of the ultra-nonlinear switching kinetics in oxide-based resistive switches,” *Adv. Funct. Mater.* **21**, 4487–4492 (2011).
- <sup>36</sup>F. Miao, J. P. Strachan, J. J. Yang, M.-X. Zhang, I. Goldfarb, A. C. Torrezan, P. Eschbach, R. D. Kelly, G. Medeiros-Ribeiro, and R. S. Williams, “Anatomy of a nanoscale conduction channel reveals the mechanism of a high-performance memristor,” *Adv. Mater.* **23**, 5633–5640 (2011).
- <sup>37</sup>Y. Y. Chen, R. Degraeve, S. Clima, B. Govoreanu, L. Goux, and A. Fantini, “Understanding of the endurance failure in scaled HfO<sub>2</sub>-based 1T1R RRAM through vacancy mobility degradation,” in *2012 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA* (IEEE, 2012), pp. 20.3.1–20.3.4.
- <sup>38</sup>M.-J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y.-B. Kim, C. J. Kim, D. H. Seo, S. Seo, U.-I. Chung, I.-K. Yoo, and K. Kim, “A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta<sub>2</sub>O<sub>5-x</sub>/TaO<sub>2-x</sub> bilayer structures,” *Nat. Mater.* **10**, 625–630 (2011).
- <sup>39</sup>Y. Chen, L. Goux, S. Clima, B. Govoreanu, R. Degraeve, G. Kar, A. Fantini, G. Groeseneken, D. Wouters, and M. Jurczak, “Endurance-retention trade-off on HfO<sub>2</sub>-metal cap 1T1R bipolar RRAM,” *IEEE Trans. Electron Devices* **60**, 1114–1121 (2013).
- <sup>40</sup>H.-S. P. Wong, C. Ahn, J. Cao, H.-Y. Chen, S. W. Fong, Z. Jiang, C. Neumann, S. Qin, J. Sohn, Y. Wu, S. Yu, X. Zheng, H. Li, J. A. Incorvia, S. B. Eryilmaz, and K. Okabe, Stanford memory trends, <https://nano.stanford.edu/stanford-memory-trends>, 2017.
- <sup>41</sup>Y. Hayakawa, A. Himeno, R. Yasuhara, W. Boullart, E. Vecchio, T. Vandeweyer, T. Witters, D. Crotti, M. Jurczak, S. Fujii, S. Ito, Y. Kawashima, Y. Ikeda, A. Kawahara, K. Kawai, Z. Wei, S. Muraoka, K. Shimakawa, T. Mikawa, and S. Yoneda, “Highly reliable TaO<sub>x</sub> RRAM with centralized filament for 28-nm embedded application,” in *2015 Symposium on VLSI Technology* (IEEE, 2015), pp. 14–15.
- <sup>42</sup>W. C. Shen, C. Y. Mei, Y. Chih, S. S. Sheu, M. J. Tsai, Y. C. King, and C. J. Lin, “High-k metal gate contact RRAM (CRRAM) in pure 28 nm CMOS logic process,” in *2012 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2012), pp. 31.6.1–31.6.4.

- <sup>43</sup>Y. Zhang and S. Swanson, "A study of application performance with non-volatile main memory," in *2015 31st Symposium on Mass Storage Systems and Technologies (MSST)* (IEEE, 2015), pp. 1–10.
- <sup>44</sup>J. Izraelevitz, J. Yang, L. Zhang, J. Kim, X. Liu, A. Memaripour, Y. J. Soh, Z. Wang, Y. Xu, S. R. Dullloor *et al.*, "Basic performance measurements of the intel optane DC persistent memory module," e-print [arXiv:1903.05714](https://arxiv.org/abs/1903.05714) (2019).
- <sup>45</sup>W. A. Wulf and S. A. McKee, "Hitting the memory wall: Implications of the obvious," *ACM SIGARCH Comput. Archit. News* **23**, 20–24 (1995).
- <sup>46</sup>J. L. Hennessy and D. A. Patterson, "A new golden age for computer architecture: Domain-specific hardware/software co-design, enhanced security, open instruction sets, and agile chip development," Turing Lecture, 2018.
- <sup>47</sup>Y. LeCun, Y. Bengio, and G. Hinton, "Deep learning," *Nature* **521**, 436 (2015).
- <sup>48</sup>E. Strubell, A. Ganesh, and A. McCallum, "Energy and policy considerations for deep learning in NLP," e-print [arXiv:1906.02243](https://arxiv.org/abs/1906.02243) (2019).
- <sup>49</sup>M. M. S. Aly, M. Gao, G. Hills, C.-S. Lee, G. Pitner, M. M. Shulaker, T. F. Wu, M. Asheghi, J. Bokor, F. Franchetti *et al.*, "Energy-efficient abundant-data computing: The N3XT 1,000x," *Computer* **48**, 24–33 (2015).
- <sup>50</sup>M. Gokhale, B. Holmes, and K. Iobst, "Processing in memory: The Terasys massively parallel PIM array," *Computer* **28**, 23–31 (1995).
- <sup>51</sup>M. Oskin, F. T. Chong, and T. Sherwood, "Active pages: A computation model for intelligent memory," in *Proceedings of 25th Annual International Symposium on Computer Architecture* (IEEE, 1998), Cat. No. 98CB36235, pp. 192–203.
- <sup>52</sup>D. G. Elliott, M. Stumm, W. M. Snelgrove, C. Cojocar, and R. McKenzie, "Computational RAM: Implementing processors in memory," *IEEE Design Test Comput.* **16**, 32–41 (1999).
- <sup>53</sup>J. Ahn, S. Hong, S. Yoo, O. Mutlu, and K. Choi, "A scalable processing-in-memory accelerator for parallel graph processing," *ACM SIGARCH Comput. Archit. News* **43**, 105–117 (2016).
- <sup>54</sup>D. Ielmini and H.-S. P. Wong, "In-memory computing with resistive switching devices," *Nat. Electron.* **1**, 333 (2018).
- <sup>55</sup>J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "Memristive switches enable 'stateful' logic operations via material implication," *Nature* **464**, 873 (2010).
- <sup>56</sup>E. Linn, R. Rosezin, S. Tappertz, U. Böttger, and R. Waser, "Beyond von neumann—Logic operations in passive crossbar arrays alongside memory operations," *Nanotechnology* **23**, 305205 (2012).
- <sup>57</sup>S. Kvatinsky, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based material implication (IMPLY) logic: Design principles and methodologies," *IEEE Trans. Very Large Scale Integr. Syst.* **22**, 2054–2066 (2013).
- <sup>58</sup>F. Alibart, E. Zamanidoost, and D. B. Strukov, "Pattern classification by memristive crossbar circuits using *ex situ* and *in situ* training," *Nat. Commun.* **4**, 2072 (2013).
- <sup>59</sup>M. Hu, C. E. Graves, C. Li, Y. Li, N. Ge, E. Montgomery, N. Davila, H. Jiang, R. S. Williams, J. J. Yang *et al.*, "Memristor-based analog computation and neural network classification with a dot product engine," *Adv. Mater.* **30**, 1705914 (2018).
- <sup>60</sup>C. Li, M. Hu, Y. Li, H. Jiang, N. Ge, E. Montgomery, J. Zhang, W. Song, N. Dávila, C. E. Graves *et al.*, "Analogue signal and image processing with large memristor crossbars," *Nat. Electron.* **1**, 52 (2018).
- <sup>61</sup>M. Le Gallo, A. Sebastian, R. Mathis, M. Manica, H. Giefers, T. Tuma, C. Bekas, A. Curioni, and E. Eleftheriou, "Mixed-precision in-memory computing," *Nat. Electron.* **1**, 246 (2018).
- <sup>62</sup>Z. Sun, G. Pedretti, E. Ambrosi, A. Bricalli, W. Wang, and D. Ielmini, "Solving matrix equations in one step with cross-point resistive arrays," *Proc. Natl. Acad. Sci. U. S. A.* **116**, 4123–4128 (2019).
- <sup>63</sup>C. E. Graves, C. Li, X. Sheng, W. Ma, S. R. Chalamalasetti, D. Miller, J. S. Ignowski, B. Buchanan, L. Zheng, S. Lam, X. Li, L. Kiyama, M. Foltin, M. P. Hardy, and J. P. Strachan, "Memristor TCAMs accelerate regular expression matching for network intrusion detection," *IEEE Trans. Nanotechnol.* **18**, 963–970 (2019).
- <sup>64</sup>G. W. Burr, R. M. Shelby, S. Sidler, C. Di Nolfo, J. Jang, I. Boybat, R. S. Shenoy, P. Narayanan, K. Virwani, E. U. Giacometti *et al.*, "Experimental demonstration and tolerancing of a large-scale neural network (165 000 synapses) using phase-change memory as the synaptic weight element," *IEEE Trans. Electron Devices* **62**, 3498–3507 (2015).
- <sup>65</sup>M. Prezioso, F. Merrih-Bayat, B. Hoskins, G. C. Adam, K. K. Likharev, and D. B. Strukov, "Training and operation of an integrated neuromorphic network based on metal-oxide memristors," *Nature* **521**, 61 (2015).
- <sup>66</sup>S. Agarwal, T.-T. Quach, O. Parekh, A. H. Hsia, E. P. DeBenedictis, C. D. James, M. J. Marinella, and J. B. Aimone, "Energy scaling advantages of resistive memory crossbar based computation and its application to sparse coding," *Front. Neurosci.* **9**, 484 (2016).
- <sup>67</sup>S. Ambrogio, P. Narayanan, H. Tsai, R. M. Shelby, I. Boybat, C. Nolfo, S. Sidler, M. Giordano, M. Bodini, N. C. Farinha *et al.*, "Equivalent-accuracy accelerated neural-network training using analogue memory," *Nature* **558**, 60 (2018).
- <sup>68</sup>L. Chua, "Memristor, Hodgkin–Huxley, and edge of chaos," *Nanotechnology* **24**, 383001 (2013).
- <sup>69</sup>M. P. Sah, H. Kim, and L. O. Chua, "Brains are made of memristors," *IEEE Circuits Syst. Mag.* **14**, 12–36 (2014).
- <sup>70</sup>S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett.* **10**, 1297–1301 (2010).
- <sup>71</sup>M. D. Pickett, G. Medeiros-Ribeiro, and R. S. Williams, "A scalable neuristor built with Mott memristors," *Nat. Mater.* **12**, 114 (2013).
- <sup>72</sup>W. Yi, K. K. Tsang, S. K. Lam, X. Bai, J. A. Crowell, and E. A. Flores, "Biological plausibility and stochasticity in scalable VO<sub>2</sub> active memristor neurons," *Nat. Commun.* **9**, 4661 (2018).
- <sup>73</sup>Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li *et al.*, "Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing," *Nat. Mater.* **16**, 101 (2017).
- <sup>74</sup>Z. Wang, M. Rao, J.-W. Han, J. Zhang, P. Lin, Y. Li, C. Li, W. Song, S. Asapu, R. Midya *et al.*, "Capacitive neural network with neuro-transistors," *Nat. Commun.* **9**, 3208 (2018).
- <sup>75</sup>G. Indiveri, B. Linares-Barranco, T. J. Hamilton, A. Van Schaik, R. Etienne-Cummings, T. Delbruck, S.-C. Liu, P. Dudek, P. Häfliger, S. Renaud *et al.*, "Neuromorphic silicon neuron circuits," *Front. Neurosci.* **5**, 73 (2011).
- <sup>76</sup>H. Nili, G. C. Adam, B. Hoskins, M. Prezioso, J. Kim, M. R. Mahmoodi, F. M. Bayat, O. Kavehei, and D. B. Strukov, "Hardware-intrinsic security primitives enabled by analogue state and nonlinear conductance variations in integrated memristors," *Nat. Electron.* **1**, 197 (2018).
- <sup>77</sup>Y. Pang, H. Wu, B. Gao, N. Deng, D. Wu, R. Liu, S. Yu, A. Chen, and H. Qian, "Optimization of RRAM-based physical unclonable function with a novel differential read-out method," *IEEE Electron Device Lett.* **38**, 168–171 (2017).
- <sup>78</sup>G. W. Burr, R. S. Shenoy, K. Virwani, P. Narayanan, A. Padilla, B. Kurdi, and H. Hwang, "Access devices for 3D crosspoint memory," *J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater., Process., Meas., Phenom.* **32**, 040802 (2014).
- <sup>79</sup>X. Sheng, C. E. Graves, S. Kumar, X. Li, B. Buchanan, L. Zheng, S. Lam, C. Li, and J. P. Strachan, "Low-conductance and multilevel CMOS-integrated nanoscale oxide memristors," *Adv. Electron. Mater.* **5**, 1800876 (2019).
- <sup>80</sup>T. Ohno, T. Hasegawa, T. Tsuruoka, K. Terabe, J. K. Gimzewski, and M. Aono, "Short-term plasticity and long-term potentiation mimicked in single inorganic synapses," *Nat. Mater.* **10**, 591–595 (2011).
- <sup>81</sup>Y. Shi, X. Liang, B. Yuan, V. Chen, H. Li, F. Hui, Z. Yu, F. Yuan, E. Pop, H. Wong, and M. Lanza, "Electronic synapses made of layered two-dimensional materials," *Nat. Electron.* **1**, 458–465 (2018).
- <sup>82</sup>J. Xiong, R. Yang, J. Shaibo, H. M. Huang, H. K. He, W. Zhou, and X. Guo, "Bienenstock, Cooper, and Munro learning rules realized in second-order memristors with tunable forgetting rate," *Adv. Funct. Mater.* **29**, 1807316-1 (2019).
- <sup>83</sup>S. Stathopoulos, A. Khiat, M. Trapatseli, S. Cortese, A. Serb, I. Valov, and T. Prodromakis, "Multibit memory operation of metal-oxide bi-layer memristors," *Sci. Rep.* **7**, 17532 (2017).

<sup>84</sup>C. Baeumer, C. Schmitz, A. H. H. Ramadan, H. Du, K. Skaja, V. Feyer, P. Muller, B. Arndt, C. Jia, J. Mayer, R. A. D. Souza, C. M. Schneider, R. Waser, and R. Dittmann, "Spectromicroscopic insights for rational design of redox-based memristive devices," *Nat. Commun.* **6**, 9610 (2015).

<sup>85</sup>S. U. Sharath, S. Vogel, L. Molina-Luna, E. Hildebrandt, C. Wenger, J. Kurian, M. Duerrschnabel, T. Niermann, G. Niu, P. Calka, M. Lehmann, H. J. Kleebe,

T. Schroeder, and L. Alff, "Control of switching modes and conductance quantization in oxygen engineered  $\text{HfO}_x$  based memristive devices," *Adv. Funct. Mater.* **27**, 1700432-1-1700432-13 (2017).

<sup>86</sup>S. Clima, Y. Y. Chen, C. Y. Chen, L. Goux, B. Govoreanu, R. Degraeve, A. Fantini, M. Jurczak, and G. Pourtois, "First-principles thermodynamics and defect kinetics guidelines for engineering a tailored RRAM device," *J. Appl. Phys.* **119**, 225107 (2016).