Reduction of Charge Traps and Stability Enhancement in Solution-Processed Organic Field-Effect Transistors Based on a Blended n-type Semiconductor

Antonio Campos, [†] *Sergi Riera-Galindo,* [†] *Joaquim Puigdollers,* [‡] *and Marta Mas-Torrent* [†*]

† Institut de Ciència de Materials de Barcelona (ICMAB-CSIC) and Networking Research Center on Bioengineering, Biomaterials and Nanomedicine (CIBER-BBN), Campus UAB, Cerdanyola del Vallès, 08193 Barcelona, Spain

‡ Dept. Enginyeria Electrònica, Universitat Politècnica de Catalunya, Jordi Girona 1-3, 08034, Barcelona, Spain

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ABSTRACT: Solution-processed n-type organic field-effect transistors (OFETs) are essential elements for developing large-area, low-cost, and all organic logic/complementary circuits. Nonetheless, the development of air-stable n-type organic semiconductors (OSC) lags behind their p-type counterparts. The trapping of electrons at the semiconductor–dielectric interface leads to a lower performance and operational stability. Herein we report printed small molecule n-type OFETs based on a blend with a binder polymer, which enhances the device stability due to the improvement of the semiconductor–dielectric interface quality and a self-encapsulation. Both combined effects prevent the fast oxidation of the OSC. Additionally, a CMOS-like inverter is fabricated depositing a p-type and n-type OSCs simultaneously.

1. INTRODUCTION

In the last two decades, the field of organic electronics has been under intense research due to its high potential for developing a new generation of flexible and low-cost devices. With this goal in mind, a huge amount of small molecule organic semiconductors (OSCs), both p- and n-type, have been synthesized and integrated as active material in organic field-effect transistors (OFETs).[1–3] However, the progress achieved with p-type OSCs outperforms that realized with n-type materials.[4,5] This is mainly due to the lower stability of the radical anions formed upon injection of electrons into the OSC.[6] Oxygen or water molecules penetrating into the OSC layer can easily oxidize the radical anions. Hence, it has been postulated that to achieve air stable n-channel OSCs, materials designed with electronic affinities (EA) around 4.0 eV are required.[7] High EAs further help to inject efficiently electrons from conventional metal electrodes diminishing thus contact resistances. It should also be noticed that thin film crystallinity and morphology also play a crucial role on the device stability since the physisorption of oxygen and moisture occurs mainly at grain boundaries.[8,9] Another cause that hampers the progress of n-type devices is derived from the fact that the hydroxyl groups present in the commonly used SiO_2 dielectric act as electron trapping centers.[10] To avoid this, the passivation of the dielectric with hydrophobic self-assembled monolayers (SAMs) or with buffer polymeric layers has been pursued.[11] In the last years, synthetic chemists have tuned the properties of n-type OSCs by modifying the chemical structure to improve their performance, stability and processability.[12–14] However, further work is needed in this direction since p- and n-type OSCs with similar performance are needed for their integration in circuits based on the so-called complementary metal-oxide semiconductor (CMOS) technology, which exhibits an enhanced signal/noise ratio and a lower power consumption.

Another current challenge in the field is the processability of the small molecule OSCs employing solution-based techniques. The preparation of homogenous and reproducible thin films over large areas is highly demanding due to the low viscosity of the solutions that leads to dewetting issues. In order to facilitate the processing of these materials and achieve uniform films, a promising route is to blend the OSC with an insulating polymer matrix.[15–20] Further, this approach also often leads to films with an enhanced crystallinity, a higher environmental stability and a reduced number of interfacial traps at the semiconductor/dielectric interface.[15,21–24] Recently, many efforts have been devoted to the deposition of OSCs blends using different coating techniques, but mainly employing p-type OSCs as active material.[25] To our knowledge, only very few works report on the deposition by spin coating of blends of n-type or ambipolar small molecule OSCs.[26–28]

In this work, we fabricated OFETs based on thin films of the air-stable OSC N,N′-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI8CN2) deposited by a solution shearing technique and we explore the influence of adding polystyrene (PS) as polymer matrix on the resulting device electrical properties (Figure 1). It was observed that devices prepared with the formulation with PS exhibit a higher performance and, importantly, a significantly improved bias and environmental stability. In-depth characterization of the devices is in agreement with the vertical stratification that takes place during the thin film crystallization that results in a sandwich structure with a crystalline OSC film in between a PS layer close to the dielectric that reduces the charge trapping and a top PS encapsulation layer. Moreover, as a proof-of-concept, by depositing in parallel by solution shearing at high speed PDI8CN2/PS, and the p-type OSC dibenzotetrathiafulvalene (DB-TTF) also blended with PS,[22,29] a CMOS-like inverter with a gain of 35 was realized. This work brings new insights into the role of the insulating matrix in the

performance of OFETs based on blended OSCs and demonstrates that the use of blends combined with a roll-to-roll compatible deposition technique represents a promising path towards the improvement of the n-type OFETs stability.

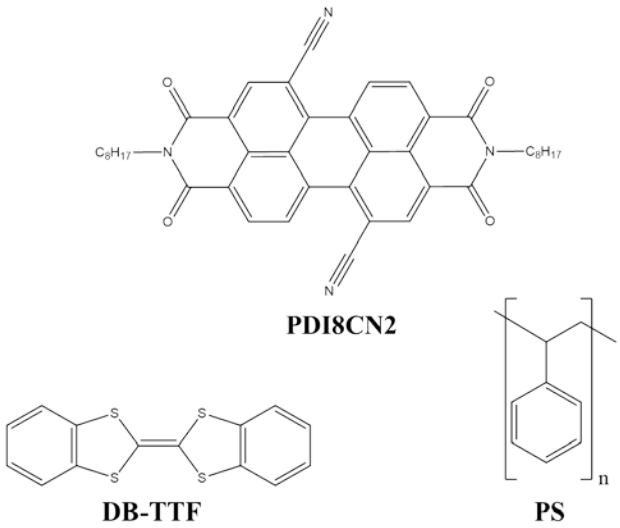

Figure 1. Chemical structures of the PDI8CN2, DB-TTF and PS.

2. EXPERIMENTAL SECTION

OFETs were fabricated on a bottom-gate bottom-contact (BGBC) configuration with interdigitated Cr/Au source and drain electrodes (channel width (W) = 5 mm and channel length (L) = 50 µm). Electrodes for OFETs were fabricated on highly n-doped Si wafers with 200 nm thermally grown SiO_2 purchased from SiMat. The source and drain electrodes were patterned by photolithography using a Micro-writer from Durham Magneto Optics LTD and a Cr/Au (5 nm / 40 nm) layer was deposited though thermal evaporation at $2 \cdot 10^{-6}$ mbar (System Auto 306 from Boc Edwards). The electrodes for the CMOS-like inverters were also fabricated following the

same process but the aspect ratio was modified to W/L = 50000 µm / 50 µm and W/L = 5000 µm / 50 µm for the n- and p-type OFETs, respectively, in order to achieve similar current values.

Ink formulations were made using PDI8CN2, purchased from Polyera Inc., and dibenzotetrathiafulvalene (DB-TTF) and polystyrene (PS) with M_W = 280 kg/mol (PS280k) and M_W = 3 kg/mol (PS3k), both purchased from Sigma-Aldrich. All the materials were used without further purification. All ink solutions used in this work were 2 % wt. in chlorobenzene. The formulations used were pure PDI8CN2, PDI8CN2:PS280k 1:2 and DB-TTF:PS3k 1:2.

The active layer fabrication was deposited on substrates by the bar-assisted meniscus shearing (BAMS) technique[22] using a home-designed equipment. This deposition technique consists in pouring an OSC solution in between a hot-plate and a bar separated ~500 µm apart forming a confined meniscus. Subsequently, the substrate is displaced in parallel to the bar at a constant speed. In these experiments, the hot-plate temperature was set at 105 ^{o}C and the coating speed was 1 cm/s. For the inverters fabrication, the n- and p- type inks were deposited simultaneously on separated parts of the bar.

The Cytop^{TM} CTL-809M (from Asahi Glass Co., Ltd.) encapsulating layer for the PDI8CN2 film was deposited by spin coating at 500 rpm the first 10 seconds and the speed was then increased to 2000 rpm for 45 seconds more.

X-ray diffraction (XRD) analysis of the thin films was carried out in a PANalytical X'PERT PRO diffractometer MRD. All measurements were carried out with monochromated Cu κ_α (λ = 1.5406 Å) radiation.

Atomic force microscopy (AFM) images were obtained using a 5100 SPM system from Agilent technologies in tapping mode and data was analyzed using Gwyddion 2.47 software.

Time of flight secondary ions mass spectrometry (ToF-SIMS) was used to determine the chemical compositional profile of the PDI8CN2/PS thin film, surface sputter etching was accomplished with Cs beam, over a 300 µm × 300 µm area using 1 keV energy settings raster. A pulsed beam of 25 keV Bi^+ ions scanned over a 50 µm × 50 µm region centered within the sputtered area was used. Analysis cycle time was 100 µs and sputtering cycle was 1.6 s and 0.5 s flood gun compensation. A high current beam of low energy (< 20 eV) electrons was employed for charge compensation, and negative ions were analyzed.

Electrical characterizations of the OFETs were carried out in air and dark conditions using an Agilent B1500A semiconductor device analyzer connected to the samples with a Karl SÜSS probe station. The samples for shelf stability were stored in ambient conditions in the dark. The electrical measurements at different temperatures were performed using a Keithley 2636A while the temperature was controlled with a MMR Technologies controller (model K–20).

OFET mobility, $\mu_{FE,sat}$, was extracted in saturation regime (V_{DS} = 20 V) using the following equation:

$$\mu_{FE,sat} = \frac{d\left(\sqrt{I_{DS}}\right)}{dV_{GS}} \frac{2\,L}{WC} \tag{1}$$

where W and L stand for channel width and length, respectively, C for capacitance per unit area, I_{DS} for drain-source current and V_{GS} for gate-source voltage. The mobility and threshold voltage

(V_{TH}) were extracted from a linear fit of the plot $(I_{DS})^{1/2}$ *vs*. V_{GS}. Finally, the sub-threshold swing (*SS*) was calculated using the following equation:

$$SS = \frac{d(\log(I_{DS}))}{dV_{GS}} \quad (2)$$

3. RESULTS AND DISCUSSION

Perylene bisimide (PDI) and naphthalene bisimide (NDI) derivatives have shown great potential as n-type OSCs.[30–32] Particularly, in the present work, we selected the derivative PDI8CN2 (Figure 1) since it exhibits a good solubility and air stability due to its low lying lowest unoccupied molecular orbital (LUMO), and has given rise to high performance OFETs.[14,33] Solutions based on PDI8CN2 in chlorobenzene 2% wt. were prepared. In order to explore the effect of a matrix insulator two formulations were employed, one containing only the OSC and another one blended with PS. After experimental optimization varying the polymer molecular weight and the OSC:PS ratio, the most optimum formulation was chosen to be PDI8CN2:PS280k in a ratio 1:2 (Table S1). Both solutions were deposited by bar-assisted meniscus shearing (BAMS) at 1 cm/s and 105 ºC, leading to continuous and homogenous crystalline films.

The thin film morphology of PDI8CN2 and PDI8CN2/PS films were characterized by AFM as shown in Figure 2. Both films are polycrystalline and their domain sizes are alike (Figure S1). However, AFM images show that grain boundaries are well defined in the PDI8CN2 film in contrast to the PDI8CN2/PS sample. This is due to the fact that in the latter sample a few nanometer thick (around 2.5 nm; average value estimated from the analysis of more than 10

pores from 3 different AFM images) of a non-continuous layer (Figure 2d) can be differentiated on the top of the crystallites. Such thin skin layer can be ascribed to a PS layer which covers the PDI8CN2 polycrystalline film, as previously observed with other p-type OSCs.[34] Also, X-ray diffraction confirms that the crystalline phase of the two films is the same (Figure S2), which matches the previously reported single crystal structure.[35]

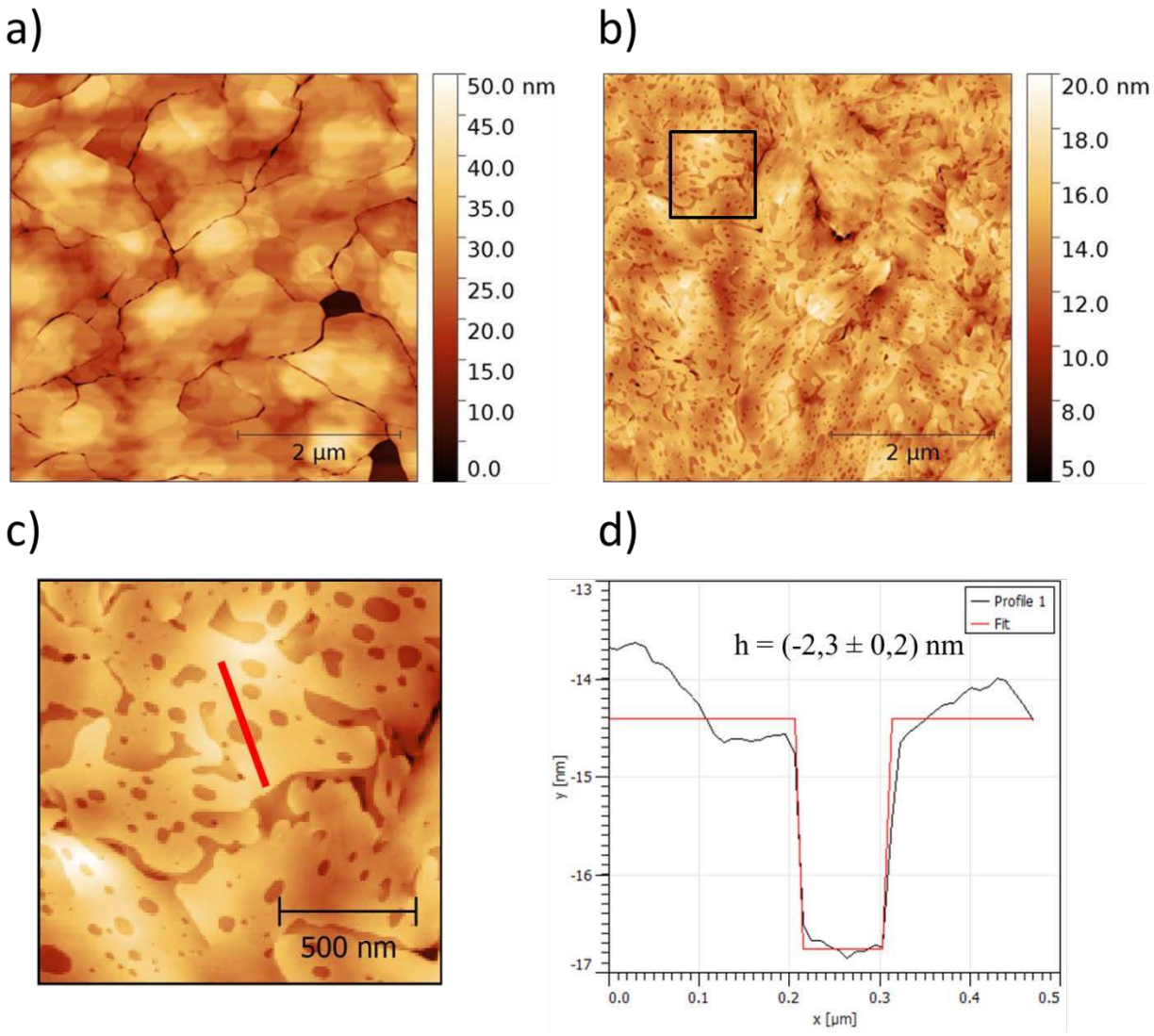

Figure 2. AFM topography images of **(a)** PDI8CN2 and **(b)** PDI8CN2/PS film. A zoom of the PDI8CN2/PS is shown in **(c)** to clarify where the height profile **(d)** was taken. A hole of approx.

2.3 nm can be appreciated in the height profile caused by a discontinuity in the PS skin layer covering the PDI8CN2 crystals.

The thickness of PDI8CN2 films were found to be (20 ± 10) nm with a roughness (R_{rms}) of 5.2 nm, while PDI8CN2/PS films were (35 ± 5) nm thick with a R_{rms} of 1.9 nm (Figure S3). Therefore, the addition of PS causes a thicker and smoother film. Furthermore, ToF-SIMS measurements indicate a major content of nitrogen on the top part of the film, which is in accordance with a vertical phase separation of the two materials, where the PS is in contact with the dielectric surface and the crystalline PDI8CN2 film lies on top (Figure S4). Such stratification during the OSC crystallization has been commonly observed in other blends.[16,21] From the ToF-SIMS data the thickness of the PDI8CN film sitting on top of the PS layer can also be roughly estimated to be around 10 nm.

Typical saturation transfer curves for PDI8CN2 and PDI8CN2/PS devices are shown in Figure 3a-b, and the corresponding output curves are collected in Figure S5-S6. The main parameters of the OFETs based on PDI8CN2 and PDI8CN2/PS are summarized in Table 1. Comparison of both transfer curves clearly shows an improvement in the performance of PDI8CN2/PS devices with an increase of the field effect mobility ($\mu_{FE,sat}$), a decrease of the threshold voltage (V_{TH} closer to 0 V), a higher on/off ratio, a steeper sub-threshold swing (*SS*) and a reduced hysteresis. Particularly, the significant improvement in *SS* and V_{TH} can be attributed to a decreased interfacial charge trap density (N_T), which is directly proportional to *SS* and has been estimated using the following equation[36] (Table 1):

$$N_T \approx \left[\frac{q\ SS\ \log(e)}{k_B\ T} - 1\right]\frac{C}{q} \quad (3)$$

Where q is the electronic charge, k_B is the Boltzmann constant and T is the absolute temperature.

It is observed that the introduction of PS reduces about one order of magnitude the N_T (from $1.51 \cdot 10^{12}$ $eV^{-1}cm^{-2}$ to $1.63 \cdot 10^{11}$ $eV^{-1}cm^{-2}$). The lower interfacial charge trap density is also reflected in the reduced hysteresis in the transfer characteristics (Figure 3). Further, it should be noticed that the clear increase in the field-effect mobility found in the PDI8CN2/PS devices could be due to the lower interfacial traps present, although dielectric depolarization effects caused by the lower permittivity PS layer might have also an impact reducing the polaronic disorder.[37,38]

Table 1. Main OFET parameters extracted from PDI8CN2 and PDI8CN2/PS based devices. The data shown are an average of 50 devices in both cases.

	$\mu_{FE,sat}$ [$cm^2/V \cdot s$]	V_{TH} [V]	$I_{ON/OFF}$	SS [V/decade]	N_T [$eV^{-1}cm^{-2}$]	τ (s)	β
PDI8CN2	$(5.5 \pm 0.5) \cdot 10^{-3}$	-8.4 ± 1.2	~ 10^5	0.90 ± 0.30	$1.51 \cdot 10^{12}$	$3.4 \cdot 10^3$	0.80
PDI8CN2/PS	$(2.8 \pm 0.3) \cdot 10^{-2}$	-0.9 ± 0.1	~ 10^5	0.15 ± 0,03	$1.63 \cdot 10^{11}$	$6.6 \cdot 10^5$	0.25

At equilibrium, source and drain contacts and the semiconductor have the same electrochemical potential. In the particular case of an n-type OSC, the application of positive V_{DS} shifts the electrochemical potential at the contacts ($\mu_2 - \mu_1 = qV_{DS}$), so then electrons can flow from source to drain contacts in order to equilibrate the electrochemical potential of the whole

system. Electron transport from source to drain contacts is realized through electronic states located on the semiconductor close to the interface with the dielectric material. The distribution of the density-of-states (DoS) on the proximity of the LUMO level determines hence the overall electronic performance of the device. The application of V_{GS} shifts the DoS to lower (for a positive V_{GS} values) or higher (negative V_{GS} values) energy values. Positive V_{GS} increases the number of available electronic states between source-drain contacts, *i.e.* higher I_{DS} current, whereas the application of a negative V_{GS} voltage decreases the number of available states, decreasing I_{DS}. Considering this, a careful analysis of the transfer characteristics of an OFET provide a qualitative picture of the distribution of electronic states in the vicinity of the mobility edge, near the LUMO energy level in an n-type OSC.

Figure 3c-d shows a schematic view of a plausible distribution of the DoS near the LUMO level according to the transfer characteristics showed in Figure 3a-b. Without the addition of PS (Figure 3c) the shape of the DoS could be described with two regions: a region with a high density of electronic states plus a region with a band-tail distribution of states extending within the band-gap of the semiconductor. The exact distribution of the region with a high density of electronic states is an open question. Whereas some authors describe this region as a Gaussian distribution of electronic states,[39] others consider that an exponential distribution would be more accurate.[40] For the sake of clarity, we consider here an exponential distribution. When PS is added (Figure 3d), the distribution of electronic states is modified. The slope of the exponential region is increased ($\varphi > \psi$ in Figure 3), whereas the band-tail distribution is reduced. Increase in the slope of the exponential region accounts for the higher *SS* value,[41] whereas the reduction of the band-tail distribution is responsible for the lower value of the I_{DS} current in the off state of the OFET when PS is added.

The V_{TH} reduction found in devices where PDI8CN2 was blended with PS shown (*i.e.*, V_{TH} closer to 0 V (Table 1)) can be explained by the DoS shift to lower energetic levels. The PDI8CN2 devices are normally ON (when V_{GS} = 0 V) because there are energetic sites in the semiconductor between the energies of the electrochemical potentials of the source and drain, which are slightly separated due to the application of V_{DS}.

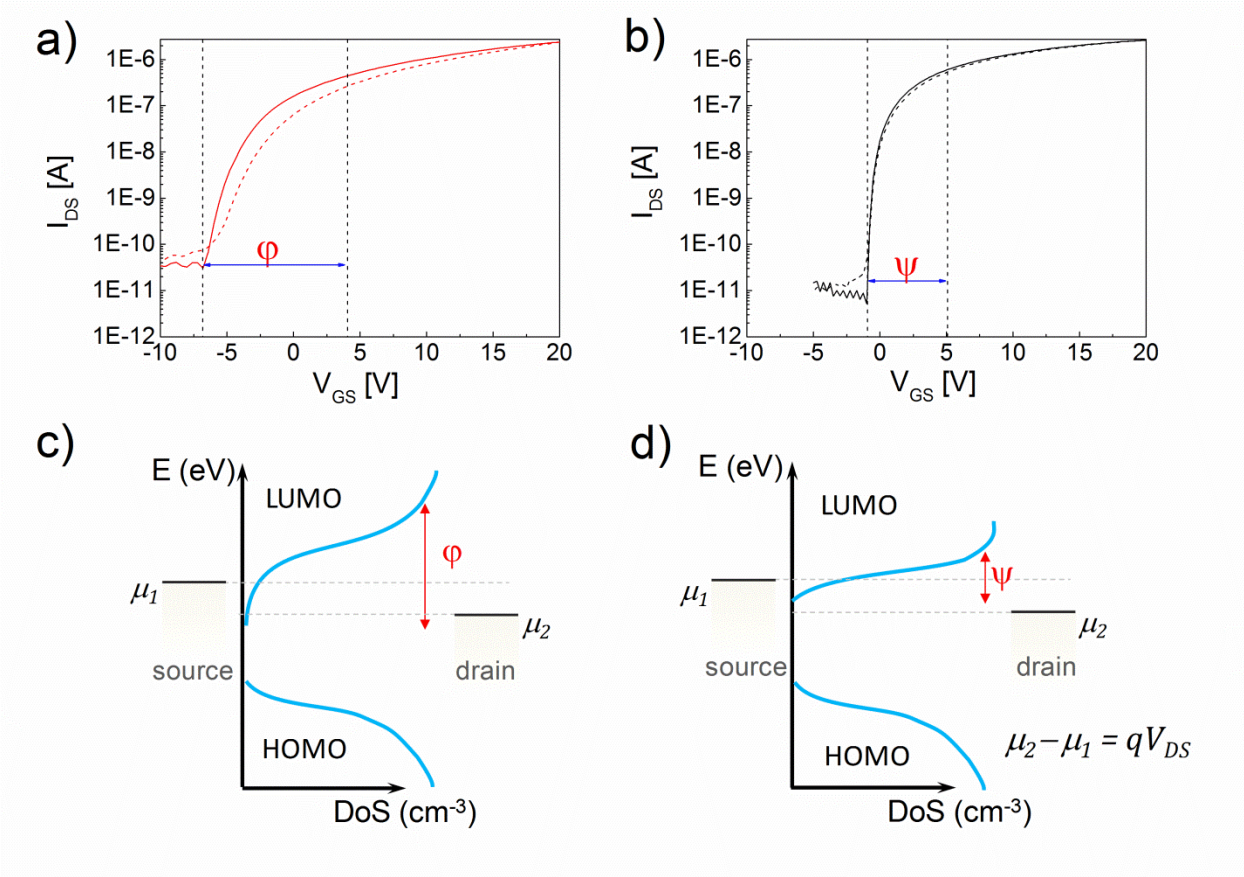

Figure 3. Top curves show the transfer characteristics of OFETs based on **(a)** PDI8CN2 and **(b)** PDI8CN2/PS. All transfer characteristics shown had a V_{DS} = 20 V. Continuous/dashed lines correspond to the forward/backward sweep of V_{GS} voltages. Bottom curves show a representation of the density of states (DoS) in a logarithmic scale of the active region of the OFET **(c)** without and **(d)** with PS.

Bias stress measurements, that is, the study of the stability of OFETs under operation, provide useful information about the reliability of the devices. Typically, under bias stress a threshold voltage shift is observed, which has been attributed to the entrapment of mobile charge carriers in localized electronic states at the OSC/dielectric interface.[42] The generation of such states in OFETs can arise from extrinsic factors such as oxidation or moisture, or intrinsic factors such as the electronic and structural disorder of the OSC films.[2] Hence, bias stress is very sensitive to the OSC/dielectric interface quality.[42] Most of the studies related to bias stress have been carried out on p-type OFETs rather than n-type ones.[43–46]

The bias stress measurements of PDI8CN2 and PDI8CN2/PS OFETs were carried out in ambient conditions at constant bias voltage V_{GS} of 20 V and V_{DS} = 0V between transfer measurements. V_{GS} was chosen in order to switch on the transistor (V_{GS} >> V_{TH}). Transfer characteristics were measured for 12 hours, every 15 minutes in the first 4 hours and every hour afterwards (Figure 4a-b). The V_{TH} variation in time is shown in Figure 4c. Remarkably, PDI8CN2/PS OFET undergoes a much lower shift (ΔV_{TH} = 7 V) than that observed for PDI8CN2, which saturates at 25 V only after 5 hours of measurements (detailed information of the mobility and threshold voltage shift with time for the bias stress experiment can be found in Table S2). The ΔV_{TH} in OFETs due to bias stress has been correlated in the literature with $N_{T,}$ since the trapped charges create an electric field that has to be compensated by the gate bias before an accumulation layer can be formed.[47] Our results are in agreement to the lower N_T found in PDI8CN2/PS films compared to the PDI8CN2 ones (Table 1). Importantly, PDI8CN2/PS devices recovered fully their initial parameters (i.e., V_{TH} and mobility) 12 hours after the bias stress measurements had been performed (Figure 4d), which could indicate that the charges are

trapped in more shallow trap states.[48] On the contrary, PDI8CN2 OFETs did not reveal an OFET behavior anymore after the bias stress test, pointing the presence of deeper traps and a deterioration of the material.

The observed threshold voltage shift was fitted with the following equation:[2,47,49,50]

$$\Delta V_{TH}(t) = (\Delta V_{TH}(\infty) - \Delta V_{TH}(0))\left(1 - e^{\left(\frac{t}{\tau}\right)^{\beta}}\right) \quad (4)$$

where t is the stress time, τ is the relaxation time for charge trapping and β is the dispersion parameter related to the characteristic width of the band tail of the semiconductor,[51,52] In other words, β is responsible for the dispersivity or spread of barrier states.[53] The values of these fitting parameters are shown in Table 1.

For the PDI8CN2/PS devices a β value of 0.25 and a relaxation time of the order of 10^5 was found. These values are on the same order than the ones found for many previous bias stress experiments performed on p-channel devices.[44] On the contrary, the PDI8CN2 devices showed a larger β value (0.80) and τ was two orders of magnitude lower (Figure 4c). Considering all this, we believe that the improved device stability under bias stress achieved with the blended OSC is mainly caused by a better quality of the OSC/dielectric interface. As previously mentioned, in the PDI8CN2/PS film a PS layer is covering the SiO_2 dielectric preventing charge trapping in the silanol groups of the oxide dielectric.[54] In fact, a reduction of the β value has been previously reported when the SiO_2 dielectric was coated with a SAM[42,44,55] or a polymer dielectric layer.[56] However, other factors that can affect the bias stress stability are the grain sizes and the penetration of oxygen and moisture into the films. It has been reported that devices based on films with a smaller grain size exhibit a higher threshold instability since the charges are trapped

at the grain boundaries.[43] Both PDI8CN2-based films prepared here exhibit similar crystalline domains. However, the films prepared with the blends are encapsulated by a skin PS layer which might protect them from external agents.[57] In order to disentangle the role of the bottom and top PS layer in the blended films, a cross-check experiment was performed. A bare PDI8CN2 film was encapsulated with Cytop^{TM} shortly after its deposition and, subsequently, it was measured under bias stress. These devices exhibited a significantly lower bias stress stability compared to the PDI8CN2/PS films, although they showed a better performance with respect to the devices without the encapsulation layer and they could recover their performance after the bias stress test (Figure S7). Accordingly, the extracted β value was 0.61 and τ was of the order of 10^4. This implies that, although to a lesser extent, the top PS layer has also some effect on the bias stress stability. Thus, the significant improvement in the operational electrical stability reached by blending PDI8CN2 with PS can be attributed to two-fold reasons: i) the passivation of the polar OH groups from the dielectric, and ii) the self-encapsulation of the OSC.

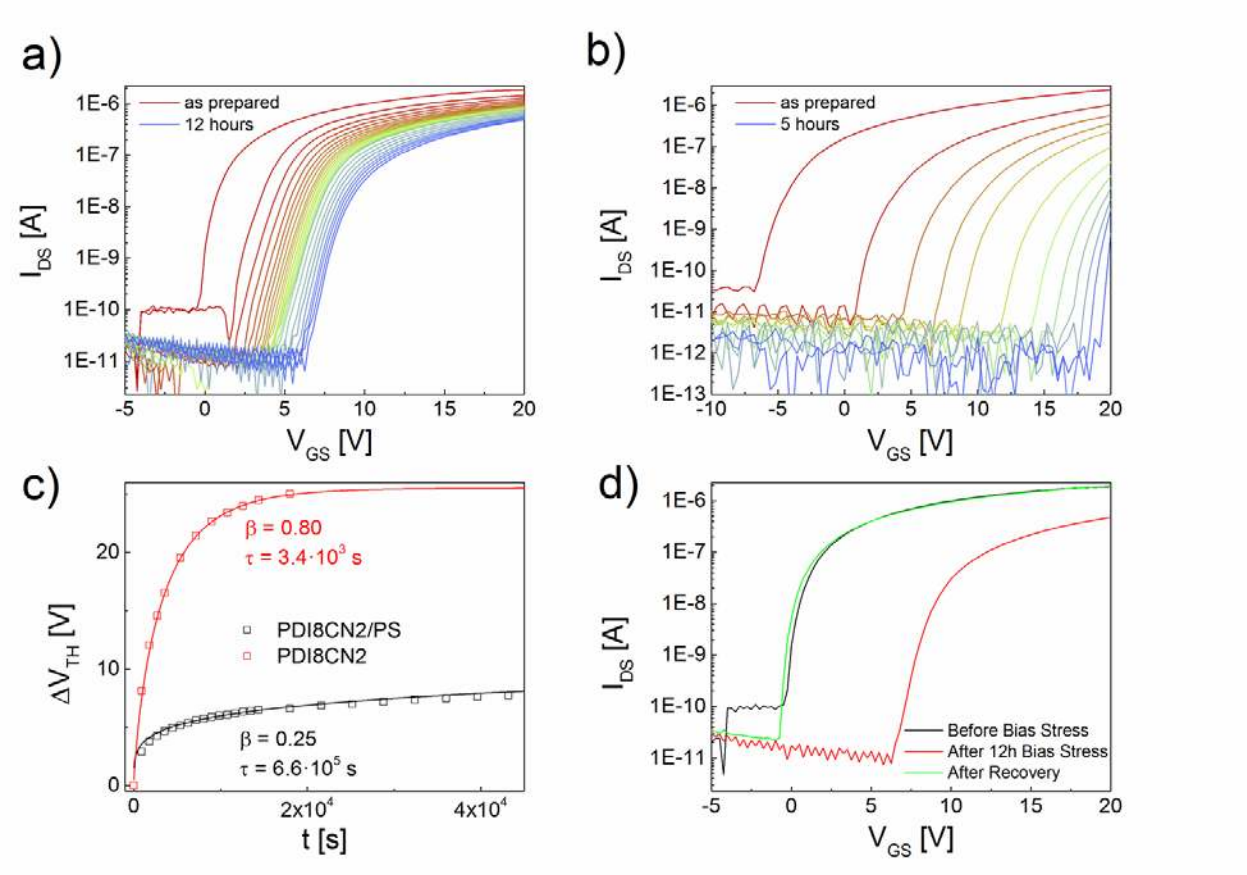

Figure 4. Bias stress stability measurements of **(a)** PDI8CN2/PS OFET and **(b)** PDI8CN2 (V_{GS} = 20 V and V_{DS} = 0 V). **(c)** Threshold voltage shift *vs.* time and fitting curves following equation 4. **(d)** Comparison of the transfer characteristics of the sample with PS just before the bias stress measurements, after the bias stress experiments and after the recovery. All transfer characteristics shown had a V_{DS} = 20 V.

The estimation of DoS calculations were performed following the method developed by Lang *et al.*,[58] in which the transfer characteristics are measured at different temperatures (from 300 K to 390 K for PDI8CN2 and from 305 to 350 for PDI8CN2/PS, that is, below the polymer glass transition). Since the transfer characteristics were measured at a fixed V_{DS}, I_{DS} is

proportional to the channel conductance for each V_{GS}. The activation energy (E_{ACT}) extracted from the Arrhenius plots of the channel conductance for each V_{GS} is shown in Figure S8 and Figure S9 for PDI8CN2 and PDI8CN2/PS devices, respectively. The E_{ACT} of PDI8CN2 OFET varies exponentially from 0.7 eV to 0.1 eV, however in the case of PDI8CN2/PS OFET E_{ACT} only varies in a much smaller range, from 0.3 eV to 0.05 eV. The rate at which E_{ACT} varies with V_{GS} indicates how easily the DoS distribution shifts to lower energies. Hence, a lower range of E_{ACT} means a lower energy required to turn the device on. The DoS in the gap of the semiconductor can be estimated from the derivative of E_{ACT} with respect to V_{GS}:[58]

$$DoS(E) = \frac{C}{q}\left(\frac{1}{d_{acc}\frac{dE_{ACT}}{dV_{GS}}}\right) \quad (5)$$

where d_{acc} is the thickness of the charge accumulation layer, here estimated with a value of 7.5 nm.[58] Figure 5 shows the DoS distribution of PDI8CN2 and PDI8CN2/PS active layers. PDI8CN2/PS has a sharp distribution of states with up to ~10^{21} $cm^{-3}eV^{-1}$ close the LUMO in contrast to the a more progressive distribution of PDI8CN2 (~10^{20} $cm^{-3}eV^{-1}$). In addition, the band tail of PDI8CN2 extends deeper into the band gap compared to PDI8CN2/PS. All these results are in agreement with a sharper *SS* observed from the transfer characteristics of Figure 3 and the β values found. Indeed, a lower β value implies lower defects in the channel of the transistor. Hence, the addition of PS reduces the trap density, weakening the sub-band gap tail, called Urbach tail, and in consequence reducing the density of sub-gap defect states in the transistor channel, being sharper the band tail of the DoS.

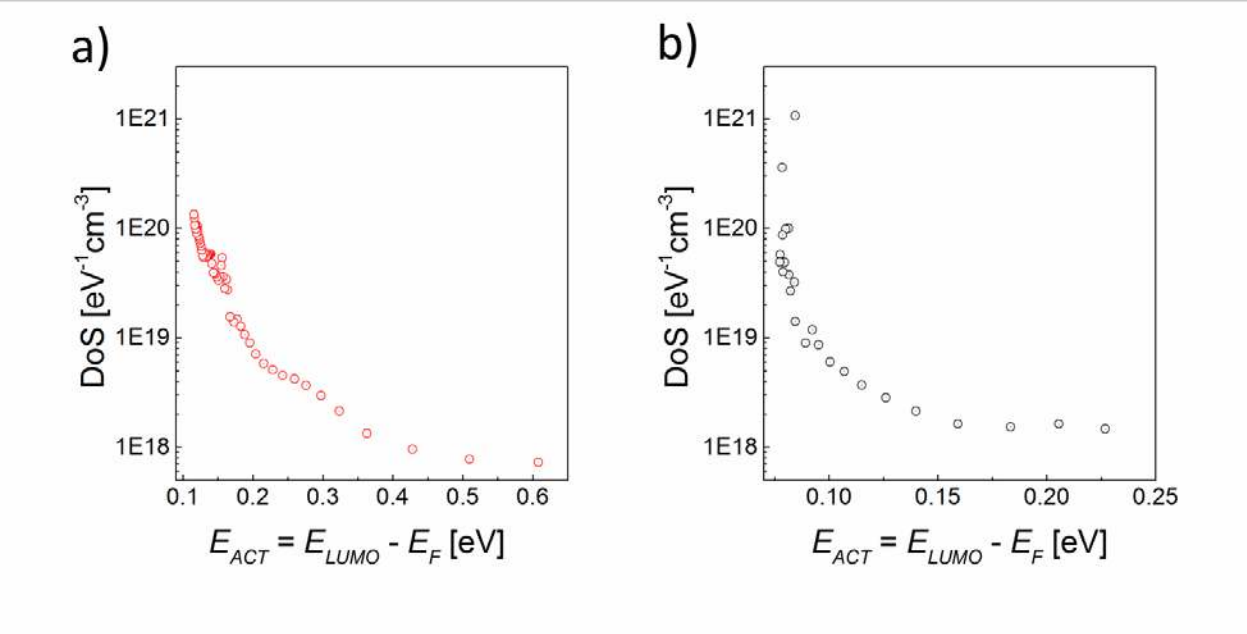

Figure 5. Distribution of DoS of **(a)** PDI8CN2 and **(b)** PDI8CN2/PS devices.

The shelf stability of the transistors was also studied by measuring the devices for several days storing them under dark and ambient conditions. The variation of the V_{TH} of the devices measured for 150 days after fabrication are depicted in Figure 6. Remarkably, not significant changes in the V_{TH} of PDI8CN2/PS OFETs are observed. In sharp contrast, the V_{TH} shifts more than 10 V in PDI8CN2 based OFETs during the same period of time. The air stability enhancement found in the blends is again indicative of the self-encapsulation of the active material by the top insulating PS layer, which acts as a barrier against the penetration of water or oxygen molecules.

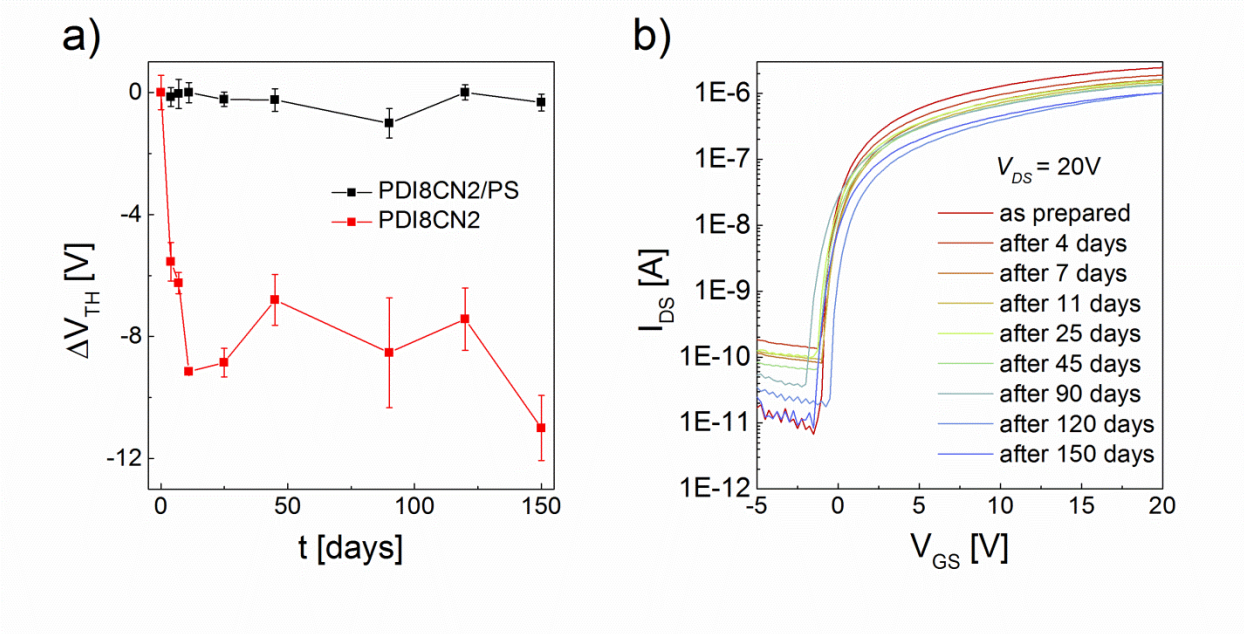

Figure 6. Shelf stability data of the PDI8CN2 and PDI8CN2/PS based OFETs. **(a)** Threshold voltage shift (ΔV_{TH}) and **(b)** Transfer characteristics of an OFET fabricated with PDI8CN2/PS as prepared and after different storage times.

Finally, a CMOS-like inverter with the structure shown in Figure 7a and in Figure S10 was fabricated using PDI8CN2/PS for fabricating the n-type OFET and DB-TTF/PS for the p-type (transfer characteristics in Figure S11). The formulation used for the p-type material was the one previously reported as described in the experimental section.[22,29] Ink solutions were deposited simultaneously by BAMS technique separating the two solution meniscus with a teflon ring (Figure 7a). Since DB-TTF/PS OFETs exhibit a mobility of one order of magnitude higher,[7] we used a n-channel 10 times wider to balance the current of both transistors. The voltage transfer characteristics of the inverter are shown in Figure 7b. The inverter reveals a good performance with a gain of 35, which is a comparable value to what it can be found in the literature for similar systems (Figure 7c).[59]

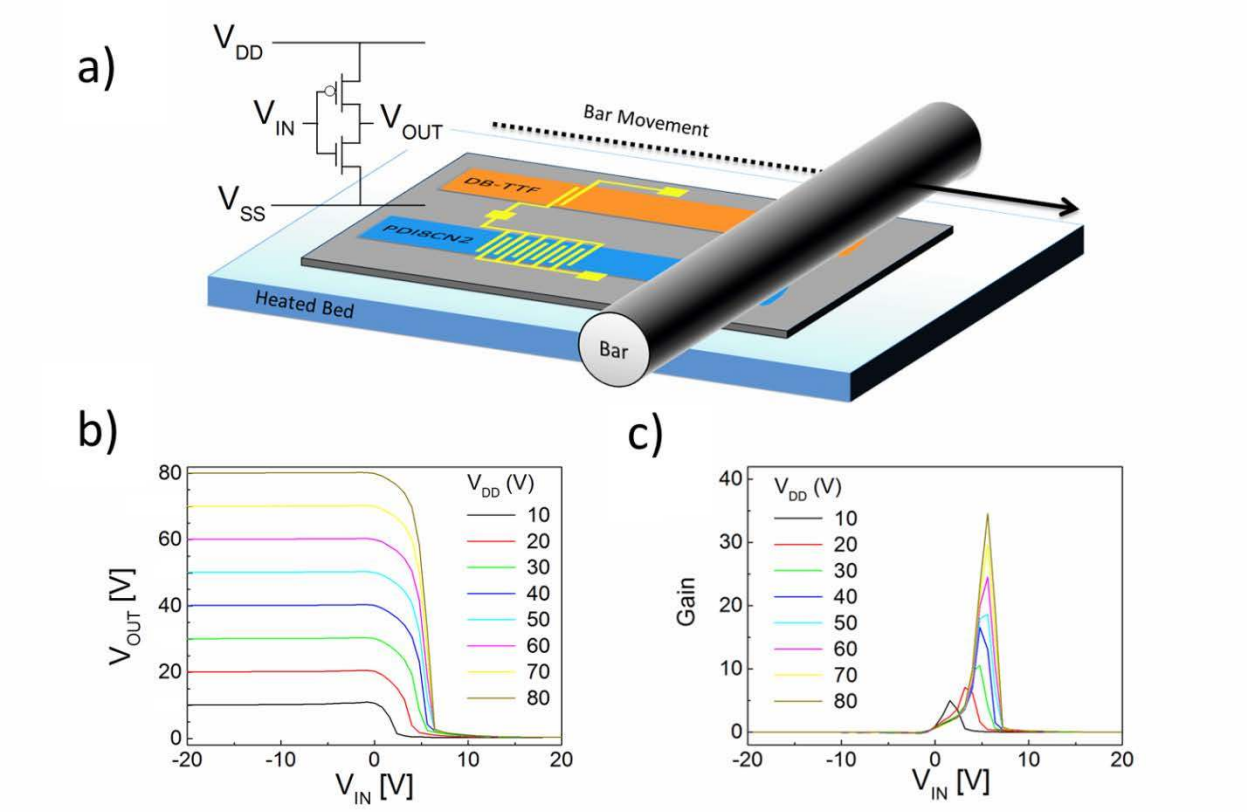

Figure 7. (a) Schematic representation of a CMOS inverter and scheme showing how the active layers of the inverter is fabricated using BAMS. **(b)** Transfer characteristics and **(c)** Gain at different V_{DD} of the CMOS-like inverter made with PDI8CN2/PS as n-type OSC and DB-TTF/PS as p-type OSC.

4. CONCLUSIONS

OFET devices based on the n-type OSC PDI8CN2 have been prepared using the solution-shearing technique BAMS. Solutions of the pure OSC and also of the OSC blended with PS were employed with the aim of gaining insights into the role of the insulating matrix. Both films

showed similar crystallinity and morphology. However, in the blended films a vertical phase separation occurred leading to the formation of a bottom PS layer close to the dielectric and, on the top, a crystalline layer of the OSC seated but self-encapsulated by a thin skin PS layer. The OFET electrical characteristics of PDI8CN2/PS revealed an optimized performance displaying improved device parameters ($\mu_{FE,sat}$, V_{TH}, $I_{ON/OFF}$ and SS). More importantly, the OFETs based on blends were dramatically more robust in terms of bias stress and environmental stability, which is crucial for the reliability of the devices. This was ascribed to the dual role of the PS matrix: i) passivation of the OSC/dielectric interface serving as a non-polar dielectric medium and ensuring a low level of charge traps and ii) protection of the OSC from the diffusion of oxygen and moisture which are highly detrimental for electron transport. Finally, the PDI8CN2/PS blends were combined with a blend of a p-type OSC to realize a CMOS-like inverter. This works advocates that by blending n-type OSCs with insulating polymeric matrixes n-channel OFETs with improved performance can be achieved even when processed with fast-deposition techniques compatible with up-scaling, of great importance for the development of this CMOS-like technology using OSCs.

ASSOCIATED CONTENT

Supporting information

Crossed-polarized optical microscope images; x-ray powder diffractograms; AFM images used to extract film thickness'; ToF-SIMS graph of PDI8CN2/PS; main transistor parameters of the tested formulations; Output characteristics of a PDI8CN2/PS film; Output characteristics of a PDI8CN2 film; Main transistor parameters extracted from the bias stress stability measurement;

Activation energy PDI8CN2 OFET; Activation energy PDI8CN2/PS OFET; Inverter scheme and optical microscope images; DB-TTF/PS OFET transfer characteristic.

AUTHOR INFORMATION

Corresponding Author

* e-mail: mmas@icmab.es

Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no conflict of interest.

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