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De Oliveira Thomas, Mandray Sylvain, Guichon Jean-Michel, Jean-Luc Schanen ...+1 more authors

Institutions: Centre national de la recherche scientifique, Thales Group

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De Oliveira Thomas[1], Mandray Sylvain[1,2], Guichon Jean-Michel[1], Jean-Luc Schanen[1], Adrian Perregaux[3]

[1]G2ELab (UMR 5269 INPG-UJF-CNRS),
Bat Ense[3], B.P. 46
38402 St Martin d'Hères CEDEX, France

[2]Thales Avionics El Syst,
41 Boulevard de la République BP 53
78400 Chatou

[3]Magsoft
20 Prospect St. Ballston Spa,
New York 12020

Abstract— Busbar structures must first achieve the principal function of a low inductive, multiport interconnection. Therefore, large sheets, very close to each other are used. An interesting issue is to use the inherent capacitive effects of busbars for achieving an integrated EMI filter function. However, this may not cause any inductance degradation. Busbar topology including the ground potential brings some EMC filtering capability. A multilayer topology is proposed to both increase the capacitances of interest and decrease the stray inductance. This has been validated using simulations and experimental results. Finally, multipurpose busbars (Electrical link, Mechanical support, thermal dissipator, EMC filter) may be one of the future key points of Power Electronics integration.

I. INTRODUCTION

Power Electronics converters are very attractive for high efficiency, low volume energy conversion. Therefore, it is generally used in many systems, such as More Electrical Aircraft, Automotive industry, or many industrial applications. However, one main drawback of such switched mode power conversion is the generation of unintended high frequency currents, known as Electromagnetic Compatibility (EMC) phenomenon. [1]

One of the main problems is due to common mode currents. These currents originate from high voltage variation inside the converter, and then flow through the metallic chassis and ground. These unintended high frequency currents must be mitigated since they can generate disturbances for other electric equipments, and even destroy some low level electronics.

One possible solution is to use EMI (Electromagnetic Interferences) filters, which are composed of passive components (inductors and capacitors). Fig. 1. shows a basic topology of an EMI Filter. However, at high frequencies, these components suffer from stray behavior: inductive effects for capacitors, and capacitive for inductors. Therefore, high frequency EMI reduction is rarely effective for high frequencies. [2]

This paper proposes the use of the inherent capacitive behavior of the electrical DC link at the converter input, in order to provide high quality high frequency capacitances Cx and Cy for EMI filtering. However, the electrical link for power electronics is restricted by high constraints regarding the stray inductance: due to the large current commutation speed, low inductance interconnects must be provided. Therefore, busbar topologies are very often used [3]. This laminated structure exhibits high capacitive effects, which can be used for EMI filtering. This has already been used in [4] and [5], to provide a large Cx. However, in this paper, the idea is to use additional layers, for ground potential, in order to also provide the Cy capacitors (Fig. 2.). This solution adds limited additional costs and will be shown as effective. Furthermore, a detailed electromagnetic analysis of this "integrated EMC filter busbar" will be provided, including an investigation on the various possible topologies: different location of a single ground layer, or using several ground layers… (sections II and III). Additionally, the stray inductance constraint on the busbar will be accounted for during the design. The various geometries will be modeled and tested using temporal simulations (section IV), and experimental validation will be proposed in section V.

II. EMC ANALYSIS OF A POWER INTERCONNECTION

A power link will be modelled starting from the equivalent circuit of Fig. 2.

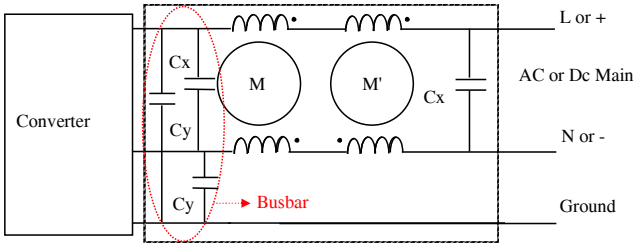

Fig. 1. Basic EMI Filter topology. Cx capacitor is connected on the power bus, Cy between bus and ground.

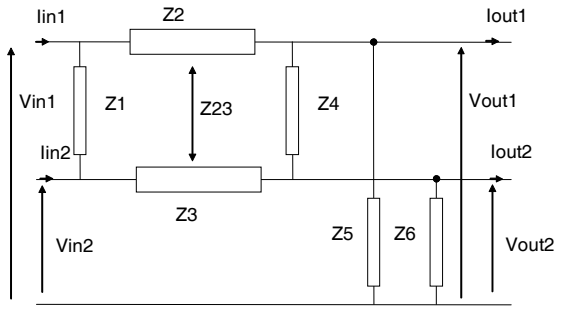

Fig. 2. Basic scheme of an electrical link.

From this electrical representation, it is easy to express the output voltage and currents as a function of the ones at the input.

$$\begin{bmatrix} V_1 \\ V_2 \\ I_1 \\ I_2 \end{bmatrix}_{in} = [Mat] \cdot \begin{bmatrix} V_1 \\ V_2 \\ I_1 \\ I_2 \end{bmatrix}_{out} \quad (1)$$

where Mat is a function of all impedances representing the electrical link

For EMC Analysis, it is common to change referential to Common Mode and Differential Mode as follows

$$\begin{bmatrix} V_{md} \\ I_{md} \\ V_{mc} \\ I_{mc} \end{bmatrix}_{in/out} = [P] \cdot \begin{bmatrix} V_1 \\ V_2 \\ I_1 \\ I_2 \end{bmatrix}_{in/out} \text{ with } [P] = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & \frac{1}{2} & \frac{-1}{2} \\ \frac{1}{2} & \frac{1}{2} & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \quad (2)$$

Therefore, in this new referential, one can obtain:

$$\begin{bmatrix} V_{md} \\ I_{md} \\ V_{mc} \\ I_{mc} \end{bmatrix}_{in} = [P] \cdot [Mat] \cdot [P]^{-1} \cdot \begin{bmatrix} V_{md} \\ I_{md} \\ V_{mc} \\ I_{mc} \end{bmatrix}_{out} \quad (3)$$

The expression of the matrix [P].[Mat].[P]$^{-1}$ is somewhat complex, but part of its elements are interesting to be studied (the x represent complex terms, not detailed here). They are detailed in eq. (4).

$$\begin{bmatrix} x & Z2+Z3-2.Z23 & \frac{Z6.Z2-Z5.Z3+Z23.(Z5-Z6)}{Z5.Z6} & \frac{Z2-Z3}{2} \\ x & x & \frac{2.Z6.Z2-2.Z5.Z3+(Z6-Z5)\cdot(Z1-2.Z23)}{2.Z5.Z6.Z1} & \frac{Z2-Z3}{2.Z1} \\ \frac{2.Z5.Z6.(Z2-Z3)+Z4.Z23.(Z6-Z5)+Z4.(Z6.Z2-Z5.Z3)}{4.Z4.Z5.Z6} & \frac{Z2-Z3}{2} & x & \frac{1}{2}\cdot\left(Z23+\frac{Z2+Z3}{2}\right) \\ \frac{Z6-Z5}{2.Z5.Z6} & 0 & \frac{Z5+Z6}{Z5.Z6} & 1 \end{bmatrix} \quad (4)$$

If the link is symmetrical, i.e. Z5 = Z6 and Z2 = Z3, the matrix is reduced to

$$\begin{bmatrix} x & 2.(Z2-Z23) & 0 & 0 \\ x & x & 0 & 0 \\ 0 & 0 & x & \frac{1}{2}\cdot(Z23+Z2) \\ 0 & 0 & \frac{2}{Z5} & 1 \end{bmatrix} \quad (5)$$

In this case, it is clear that differential mode and common mode are completely decoupled. This is very interesting for EMC analysis and reduction, since differential mode and common mode generators don't mix together.

This symmetry is thus an advantage and will be kept in the busbar design

III. BUSBAR GEOMETRY

The proposed busbar aims at linking the DC bus capacitor with a power module (Fig.3). Therefore, its stray inductance must be kept low. Usually, large copper foils are used, close to each other, in order to take advantage of the large mutual coupling and to decrease the stray inductance [3]. Therefore, a busbar is highly capacitive. The idea is to use this capacitive behaviour to provide EMC filtering capability. Classically, an EMC filter implies Cx (for differential mode) and Cy for common mode, as illustrated in Fig. 2. The high frequency quality of these capacitors is of great importance, and using the stray behaviour of the busbar seems attractive, since the parasitic capacitance will exhibit a very low esl (equivalent series inductance).

Including the Cy capacitance in the busbar configuration requires the inclusion of a ground potential sheet, in addition to plus and minus sheets.

Several geometries can be proposed. If only three layers are proposed (plus, minus and ground), three solutions are possible. To preserve the desired symmetry, in order to avoid common mode/ differential mode coupling (section II), a layout with the ground inserted between plus and minus will be selected. Adding further layers and keeping the geometrical symmetry leads to the solution of a sandwich mixing power and ground tacks. This increases the capacitive coupling and therefore the filtering effect. Examples are illustrated in Fig.4. However, further investigation is needed to check the impact of the ground layer on the switching loop inductance, as well as on the capacitive matrix.

For this purpose, due to simple geometry, parallel plate capacitor formula can be used. For inductive modelling, to account for all couplings, frequency and proximity effects, a complete modelling in a PEEC software [6] has been used.

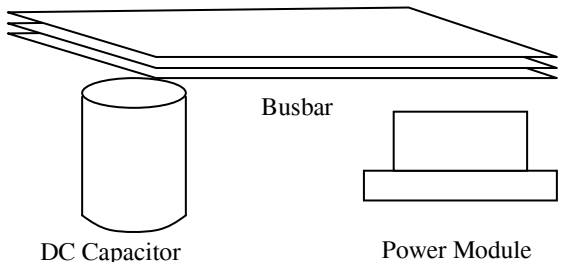

Fig. 3. Converter topology including DC bus capacitor, busbar, power module.

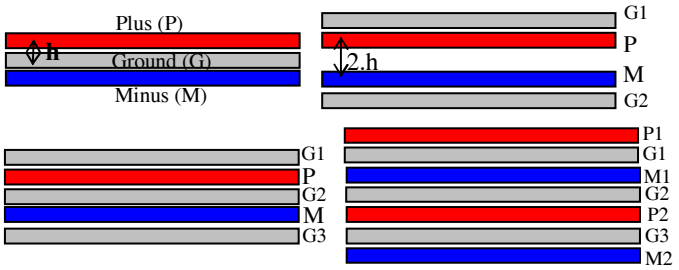

Fig. 4. Example of multi layers busbars arrangement (cross view, not to scale). 3-layers, 4-layers, 5-layers and 7-layers.

IV. ELECTROMAGNETIC MODELING

The investigation of the various geometries on both inductive and capacitive aspects has been achieved using simulation [6].

A. *Capacitive modeling*

The complete capacitive model starts from the number N of conductors (copper sheets). For a set of N conductors, N-1 voltages can be defined, leading to a (N-1)*(N-1) symmetrical matrix. The number of capacitors to represent is thus N*(N-1)/2. However, since all ground sheets are at the same potential, the final representations accounts only for 3 different potentials and thus 2 voltages, which leads to only 3 capacitors (Cx, Cy and Cy). The computation of all three capacitors however accounts for all N*(N-1)/2 capacitors between all conductors, taking into account the fact that several grounds are connected together, what shorts some capacitors. If M is the number of ground conductors, the remaining number of capacitor is:

$$N*(N-1)/2 - M*(M-1)/2 \qquad (6)$$

The computation of Cx and Cy capacitors results from the association of all elementary capacitors. The complete process is illustrated for the 5-layers structure in Fig. 5.

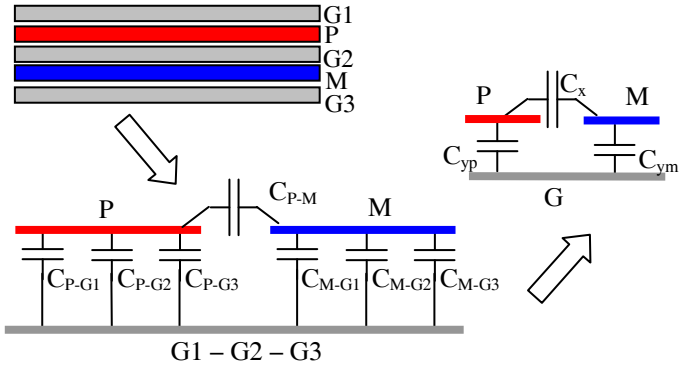

Fig. 5. Capacitive model and reduction for the 5-layers example. Conductors G1, G2 and G3 are connected together.

As mentioned before, based on the simple parallel plate capacitor formula, the capacitance will be considered proportional to the inverse of the dielectric thickness.

Table 1 sums up for each configuration of Fig. 4 the number of capacitors, and the values of Cx and Cy obtained, with respect to a reference value of C, corresponding to a base dielectric thickness h separating two consecutive copper layers.

Table 1. Capacitive behavior investigation for symmetrical geometries (11 cm long and 5 cm wide busbar)

Geometry	3 layers	4 layers	5 layers	7 layers
N	3	4	5	6
M	1	2	3	3 for G, 2 for P&M
Number of capacitors	3	5	7	16
Elementary capacitor values	C_{PG}=C C_{MG}=C C_{PM}=C/2	C_{PG1}=C C_{MG2}=C C_{PM}=C/2 C_{PG2}=C/3 C_{MG1}=C/3	C_{PG1}=C C_{PG2}=C C_{PG3}=C/3 C_{MG1}=C/3 C_{MG2}=C C_{MG3}=C C_{PM}=C/2	C_{P1G1}=C C_{P1M1}=C/2 C_{P1G2}=C/3 C_{P1G3}=C/5 C_{P1M2}=C/6 C_{M1G1}=C C_{M1G2}=C C_{M1P2}=C/2 C_{M1G3}=C/3 C_{P2G1}=C/3 C_{P2G2}=C C_{P2G3}=C C_{P2M2}=C/2 C_{M2G3}=C C_{M2G2}=C/3 C_{M2G1}=C/5
Cx	C/2	C/2	C/2	5.C/3
Cyp=Cym	C	4.C/3	7.C/3	64.C/15
Cyp=Cym	C	1.33.C	2.33.C	4.27C

As clearly shown in Table 1, 3-, 4- and 5-layers have been built in order to have a fair comparison: the distance between plus and minus sheets is kept constant at a 2.h value; this brings a constant Cx. The multiplication of layers in the 7-layers topology leads to an increase in Cx.

Equivalent Cy capacitors, always equal for intentional symmetry reasons also increase with the number of layers (ground or P&M), from 1/3 to more than 4 times.

B. *Inductive modeling*

Since the distance between the plus and minus sheets has been kept constant (except for the 7-layers case), one could imagine that the inductance should not be affected by the presence of ground layers. However, since switching currents during commutations exhibit high frequency components, eddy currents in the ground sheets may be encountered, which

may modify the inductive behavior. Supposing an infinite ground sheet disposed between the two P and M layers, and using the image method [2] would lead to a decrease in inductance and also mutual coupling. Since the loop inductance of the busbar accounts for both parameters, the final result is not obvious. In addition, the ground foil is not infinite at all. Therefore, precise simulations using PEEC method have been carried out to investigate the stray inductance of the busbar, depending on the chosen topology. The reference case will be a 2-layers busbar, without any integrated ground, with a 2.h distance between P and M sheets.

Table 2 gives the simulation results, where it is shown that it has been possible to keep a reasonable stray inductance when inserting the ground sheets inside the busbar. The degradation is about 6% only. The multiplication of ground foils does not change this effect significantly, which induces an increase in the common mode capacitances without changing the differential mode inductive behaviour.

Even more, a 7-layers busbar configuration reduces the stray inductance dramatically, by taking advantage of P and M sheets division.

Obviously, further improvement may be obtained by reducing the value of the dielectric thickness (h), which would result in a further decrease in stray inductance and an increase of the capacitive matrix, as proposed in [4-5] and [7]. Additionally, a change in the dielectric material properties may also increase the capacitive behaviour.

Table 2. Stray inductance investigation for symmetrical topologies (11 cm long and 5 cm wide busbar)

2 layer	3 layer	4 layer	5 layer	7 layer
6.85 nH	7.29 nH	7.26 nH	7.26 nH	2.57 nH

All these issues are linked to other necessary capabilities of the busbar, regarding insulation (between Plus and Minus, but also with respect to the Ground) and partial discharge behaviour. Therefore, a complete design must account for these constraints.

C. Circuit Model

After modelling, an automatic link to a time simulator is proposed, allowing the validation of the busbar effect on the EMC behaviour [8]. The automatic coupling between the PEEC model and the circuit simulator has been used and completed by adding all capacitors corresponding to the busbar model. Fig. 6 illustrates the simulated schematics, in the example of the 5-layers structure. A Line Impedance Stabilization Network (LISN [2]) has been inserted between the power supply and the DC bus capacitor, to provide a known path for common mode current.

D. Simulation Results

Since the 4-layers topology was not so different in comparison with the 3-layers one, its results will not be displayed. In addition, it has been preferred to illustrate the effect of non symmetrical geometries, which generate stray couplings between differential mode and common mode. Therefore, an additional geometry has been added, replacing G and M in the 3-layers geometry of Fig. 4. It will be called 3-layers-non symmetrical. Its stray inductance is lower, the Cx value is higher (Cx=C), but Cyp and Cym are different: Cyp=C/2 and Cym=C.

Results obtained on common mode current (Fig. 7) show the effective reduction, when comparing a conventional busbar and multilayer ones. As expected, the higher capacitive structures allow a better common mode reduction. Obviously, most of the gain is achieved in the high frequency domain, since these capacitors cannot be as high as discrete Cy capacitors. However, their quality is better.

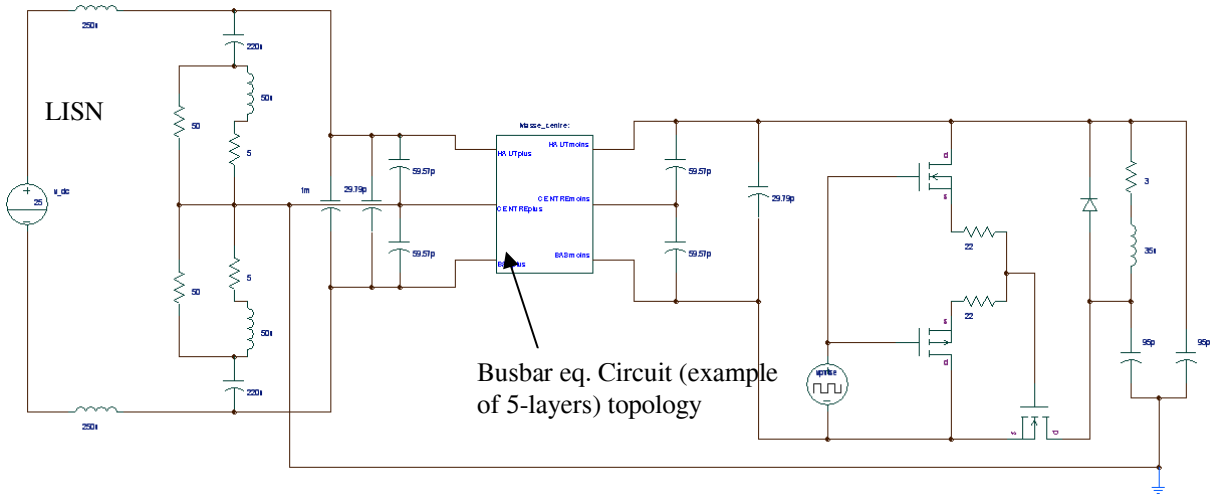

Fig. 6. Simulation scheme (the converter is composed of a single leg – chopper cell).

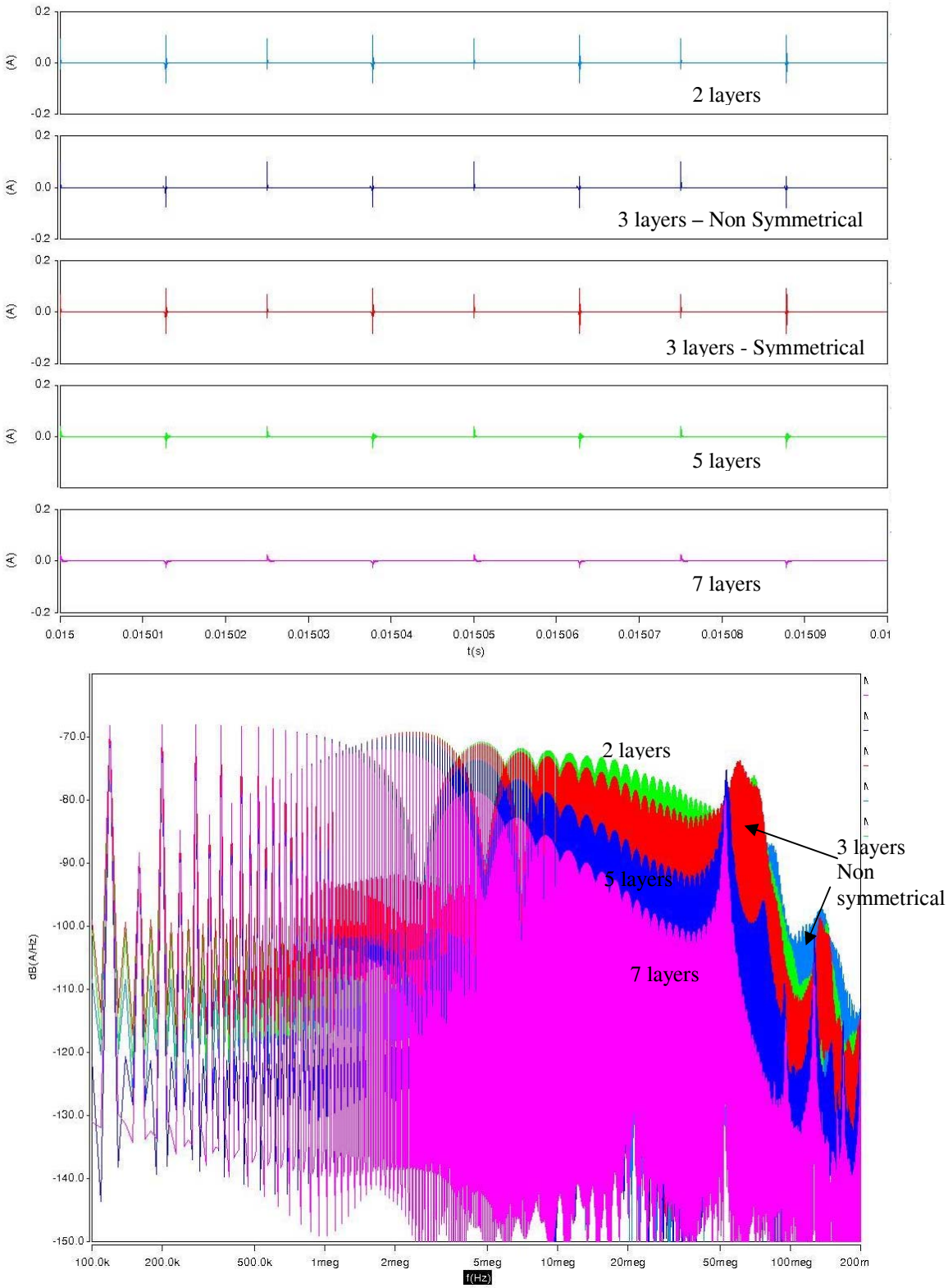

Fig. 7. Common mode current reduction for the multilayer busbars in comparison with the conventional one. top: common mode current temporal waveforms – Bottom frequency analysis.

An additional remark is that the 3-layers non symmetrical structure does not filter the common mode current as well as the symmetrical one, as expected from the results of section II.

V. Experimental Validation

A first set of prototypes using simple PCB has been proposed to validate the concept. A simple chopper has been built and a conventional two layer busbar has been compared to a three layer busbar, with the ground between plus and minus sheet (Fig. 8). The ground sheet has been designed to collect the maximum common mode current: it is a complete metal plane under the power components and driver. For an actual power converter with power module, it should be directly connected to the heatsink.

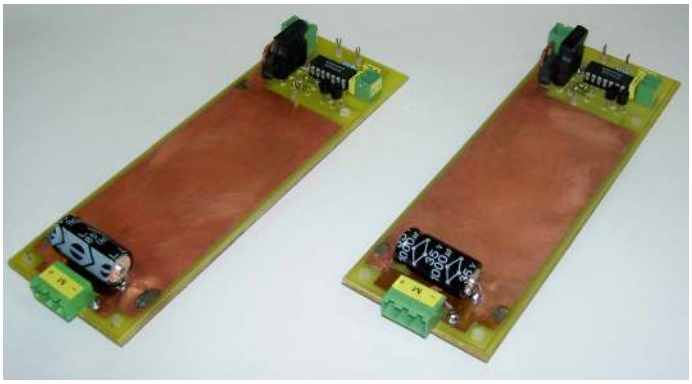

Fig. 8. Experimental setup for two and three layer busbar: same converter and different busbar layout.

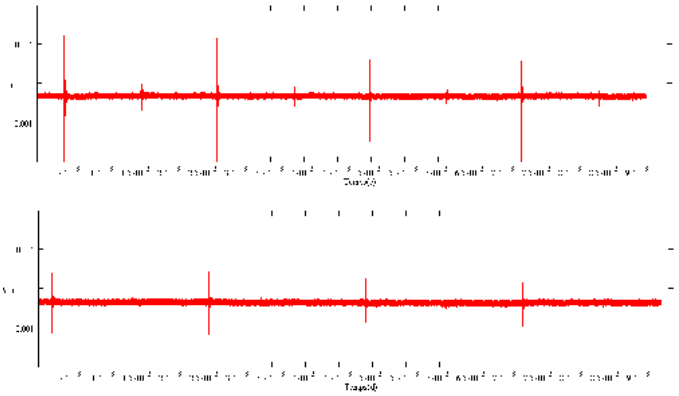

Fig. 9. Experimental results on Common mode current, top: 2layers – bottom: 3 layers.

Results show a very important common mode reduction, which validates the proposed idea (Fig. 9.). The common mode current has been classically measured using a current probe on both feeding wires.

VI. Conclusion

This paper starts from the basic idea in power integration to use the stray capacitive effects of a multilayer laminated busbar to reduce conducted EMI. The electrical link realized by the busbar must achieve several functions: low inductive link, high Cx and high Cy. Therefore, the ground potential is accounted for in the design. A complete electromagnetic analysis has been carried out in order to check the electromagnetic behavior of the busbar. Geometrical symmetry results in the electrical symmetry allowing for the de-coupling between common mode and differential mode. Simulation is used to check the influence of busbar geometry on its electrical parameters. The effective EMI reduction has been validated using both simulation and measurement. In the proposed examples, the frequency range is quite high, and thus especially interesting for radiated emission reduction. However, for bigger structures, higher capacitance can be expected, and therefore, the EMI reduction will be effective even for lower frequencies. Furthermore, for low frequencies active solutions have been shown to be good candidates in conjunction with integrated solutions [9].

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