# Reduction of DC-Bus Capacitor Ripple Current With PAM/PWM Converter

Frederick D. Kieferndorf, *Member, IEEE*, Matthias Förster, and Thomas A. Lipo, *Fellow, IEEE*

***Abstract*—Electrolytic capacitors are used in nearly all adjustable-speed drives, and they are one of the components most prone to failure. The main failure mechanisms include loss of electrolyte through outgassing and chemical changes to the electrolyte and oxide layer. All the degradation mechanisms are exacerbated by ripple current heating. Since the equivalent series resistance of electrolytic capacitors is a very strong function of frequency it must be properly modeled to accurately calculate the power loss. In this paper, a method to reduce the ripple current in a constant Volts/Hertz pulse-amplitude-modulation (PAM)/pulsewidth-modulation (PWM) converter driving an induction motor is investigated. The dc-bus voltage amplitude is reduced in proportion to speed by a buck or current stiff rectifier and the PWM modulation index is maintained at a high level to achieve a reduced ripple current below base speed. By comparison with a diode-bridge-fed PWM voltage stiff inverter, it is shown that the PAM/PWM mode of operation can lead to a significant reduction in capacitor power loss leading to increased capacitor lifetime or decreased capacitor size. The capacitor heating is analyzed using numerical and analytical techniques. Experimental results are provided to verify the analytical results.**

***Index Terms*—Adjustable-speed drive (ASD), buck rectifier, current ripple, current stiff rectifiers (CSRs), electrolytic capacitor modeling, equivalent series resistance (ESR), industrial drives, pulse amplitude modulation (PAM), pulsewidth modulation (PWM), voltage stiff inverter (VSI).**

## I. Introduction

NEARLY all modern adjustable-speed drives (ASDs) use electrolytic capacitors to supply the stiff dc-bus voltage for pulsewidth-modulation (PWM) voltage stiff inverters (VSIs). The capacitors also decouple the rectifier from the inverter part of the drive by providing a low-impedance path for the high-frequency PWM ripple current. The main sizing considerations for bus capacitors are ripple current rating and voltage holdup time during power failure. Voltage ripple specifications will typically be met when the previous two specifications are satisfied, thus, it is not normally a primary concern for sizing.

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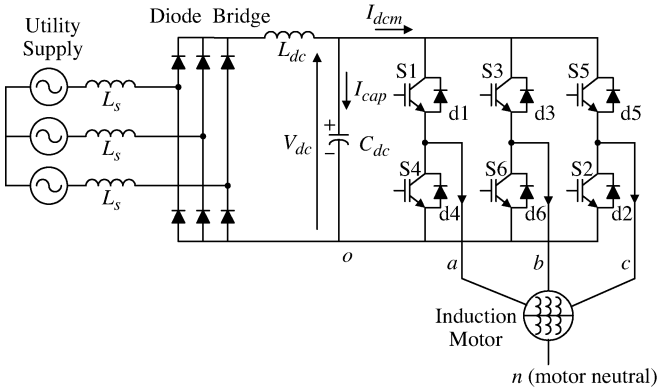


Fig. 1. Standard diode-bridge-fed PWM VSI induction motor drive.

Electrolytic capacitors have a relatively high equivalent series resistance (ESR) and must endure high current ripple from the inverter and often the rectifier as well. The focus of this paper is the inverter contribution, since with proper design the rectifier contribution to the ripple current can be made negligible (i.e., by adding a large enough ac- or dc-side reactor) [1], [2]. Operating temperature is the main factor causing degradation of the capacitor parameters, especially the ESR. The ripple current and ambient temperature are the main contributors to the temperature rise of the capacitor. Two significant degradation mechanisms accelerated by heating are chemical changes in the oxide layer and the electrolyte [3] and electrolyte vapor leakage through the capacitor end seal. Both factors lead to an increase in ESR over the operating life of a capacitor. At some point the ESR will exceed the maximum recommended value (termed parameter drift failure [3]). This is considered the end of life for the capacitor at which time it should be replaced [2].

The rms ripple current in the electrolytic capacitor from the inverter side switching is primarily a function of the load phase angle $(\phi)$ and the modulation index $M_i$. It is assumed that the machine transient inductance $(L_\sigma)$ is large enough so that the output switching frequency current ripple is negligible. The capacitor rms ripple can then be considered to be entirely composed of segments of the three sinusoidal output currents chopped up at the switching frequency [4], [5]. To examine the power loss in the capacitor an estimate of all significant current harmonics is needed. The frequency-dependent ESR model value is then multiplied at each harmonic frequency by the square of the current component and the resulting terms summed.

The standard mode of operation of an ASD is to maintain the link voltage $(V_{\rm dc})$ at a constant value and adjust the modulation index to control the output voltage magnitude. As shown in Fig. 1, three-phase diode bridge rectifiers produce the link

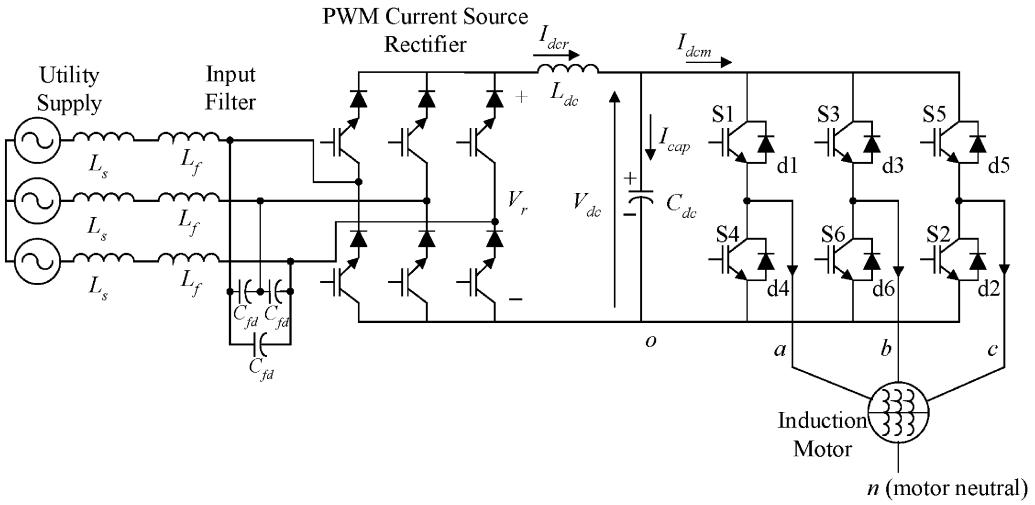


Fig. 2. PAM/PWM converter with CSR and VSI.

voltage in the majority of drives. Increasingly, due to power quality considerations, voltage stiff rectifiers (VSRs) are used to provide a near-unity power-factor (PF) utility interface.

If the VSR is replaced with a current stiff rectifier (CSR), $V_{\rm dc}$ can be reduced below base speed and unity PF can still be achieved. It is important to note that there are many alternative rectifier topologies that could have been chosen and cost is always a major consideration. For the purposes of this paper the CSR was not necessarily the lowest cost option, but it provided adjustable dc-link voltage, flexibility and is a well-known topology. The reduction of $V_{\rm dc}$ below the motor base speed is also known as pulse amplitude modulation (PAM) [6] and the combined mode of operation will be denoted as PAM/PWM. The PAM/PWM topology is shown in Fig. 2.

The effects of this additional degree of freedom, with respect to the standard drive of Fig. 1, can be explored in the overall ASD in terms of efficiency, lifetime, dynamic response, etc. This paper examines the benefits of varying $V_{\rm dc}$ and $M_i$ on the electrolytic capacitor ripple current with an induction motor load. The reduced current ripple results in a reduction of power losses in the capacitor over most ranges of loading and speed. This in turn can lead to a reduction in the necessary bus capacitance or to an increase in capacitor lifetime. A 7.5-kVA prototype inverter driving a 10-hp induction motor was used to obtain experimental results.

## II. ESR Model for Electrolytic Capacitor

In order to reasonably estimate the power loss in an electrolytic capacitor bank a good model is needed. The electrolytic capacitor model used in this analysis was introduced in [2] where it was shown to match well with experimental results, including lifetime prediction. The circuit diagram of the model is shown in Fig. 3. The physical meaning of each component is indicated in the figure. The complete equation for the real part of the impedance, which is the ESR, is shown by

$$\text{ESR} = \frac{R_2}{1+\omega^2 \text{C}_2^2 R_2^2} + R_{1b}\text{e}^{\frac{(T_{base}-T_{\rm core})}{E}} + R_0. \qquad (1)$$

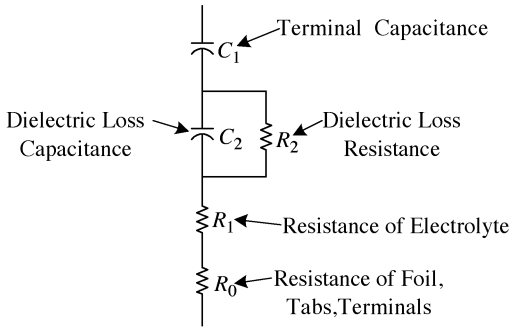


Fig. 3. Electrolytic capacitor model.

The frequency dependence of the ESR is due to the dielectric and is provided in the model by the parallel combination of $R_2$ and $C_2$. The temperature dependent nature of the electrolyte resistance, $R_1$ is modeled with a base resistance, $R_{1b}$ and an exponential temperature variation controlled by a temperature sensitivity factor $E$. $T_{base}$ is the temperature at which the $ESR$ was measured while $T_{\rm core}$ is the temperature of interest for the ESR calculation.

The ripple current heating losses in the capacitor are estimated based on this model. The parameters for the capacitors used in the experimental setup have been determined by impedance measurements of the capacitor bank. The measured variation of ESR with frequency is shown in Fig. 4. A curve fit to the model, done in MATLAB, is also shown in the figure. More series parallel *RC* segments can be added to produce a better fit [2], but a single pair results in sufficient accuracy to judge the relative change in losses. The resulting parameter values are shown in Table I. The ESR change with temperature is shown in Fig. 5 for several frequencies of interest.

## III. Determination of Capacitor Current Spectrum of VSI Drive

The capacitor current spectrum can be estimated by chopping up the sinusoidal output currents going to the induction motor. The modulation method used to create the PWM device gate signals in the VSI was the regular sampled space-vector

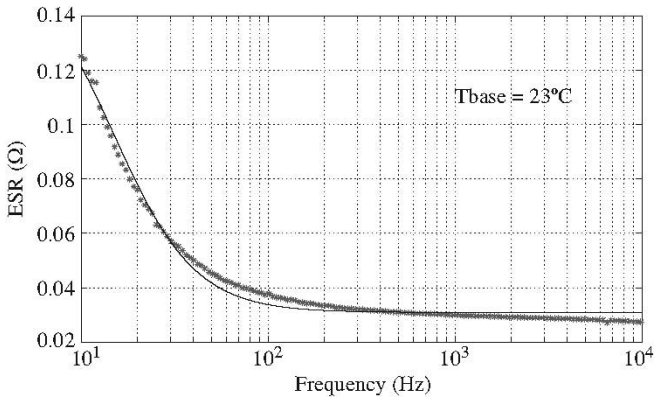


Fig. 4. ESR versus frequency of electrolytic capacitor bank: experimental data points ($^*$), model with curve fit parameters (—).

TABLE I
ELECTROLYTIC CAPACITOR PARAMETERS

| | | |
|---|---|---|
| $R_0$ | 22.9 | mΩ |
| $R_{1b}$ | 8.0 | mΩ |
| $E$ | 16.1 | °K$^{-1}$ |
| $R_2$ | 131 | mΩ |
| $C_1$ | 2530 | μF |
| $C_2$ | 81000 | μF |

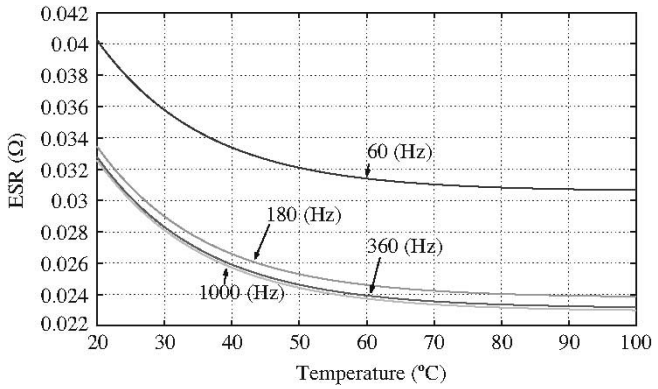


Fig. 5. ESR versus temperature of electrolytic capacitor bank for several frequencies of interest.

PWM (SVPWM) ramp comparison method. This is equivalent to the direct digital method used in (SVPWM) [7]. The experimental setup uses a TI TMS320F240 DSP to produce the gate signals with an identical modulation method. The modulation index used in the calculations is defined by

$$V_1 = M_i \frac{V_{\rm dc}}{2} \sin(\omega\, t) \tag{2}$$

where $V_1$ is the fundamental output voltage and $M_i$ is the inverter modulation index [8]. Defined this way the ideal limit of the linear modulation region for SVPWM is when $M_i = 1.15$. The capacitor current harmonics are calculated numerically in MATLAB as will be outlined below.

The following voltage and current variables follow the standard notation based on the nodes labeled in Fig. 2. First, the

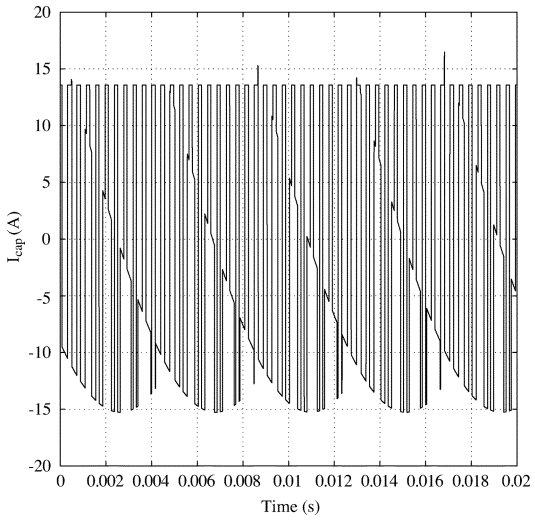


Fig. 6. Calculated capacitor ripple current waveform: diode-fed inverter, 40-Hz fundamental, 75% rated motor torque load.

PWM pole voltage waveforms ($v_{ao}$, $v_{bo}$, and $v_{co}$) are determined. A speed/frequency command is given and the modulation index is determined based on the dc-bus voltage and the required induction motor terminal voltage. The three regular sampled voltage references are formed and then the intersections with the triangle carrier are computed. The resulting output voltage as well as the given load torque (as slip frequency) are fed into an induction machine model. This determines the output current magnitude and phase for all three phases assuming a balanced three-phase set.

The capacitor current is then calculated by first determining the pole currents in the upper diodes and switches of the inverter from the pole voltage switching instants and the phase currents

$$I_{pa} = I_{s1} - I_{d1} \quad I_{pb} = I_{s3} - I_{d3} \quad I_{pc} = I_{s5} - I_{d5}. \tag{3}$$

The sum of the three upper pole currents than determine the dc-link current to the motor as

$$I_{\rm dcm} = I_{pa} + I_{pb} + I_{pc}. \tag{4}$$

Assuming the rectifier current is constant with negligible harmonic content (i.e., $I_{\rm dcr} = I_{\rm dcm(ave)}$), as mentioned previously [1] the capacitor current is

$$I_{\rm cap} = I_{\rm dcm(ave)} - I_{\rm dcm}. \tag{5}$$

The calculated and experimental waveforms of $I_{\rm cap}$ for the same motor speed and rms fundamental output current for full $V_{\rm dc}$ (diode-bridge-fed ASD) are shown in Figs. 6 and 8 and for reduced $V_{\rm dc}$ (CSR-fed ASD) are shown in Figs. 7 and 9. It can be seen that sinusoidal segments match up reasonable well in the sets of waveforms. The measured waveform for $I_{\rm cap}$ was captured with a low insertion impedance coaxial current transformer put in the output dc-link current path [9]. The inverted ac coupled waveform is shown on the oscilloscope trace after digital filtering (80-kHz bandwidth) to remove the high frequency current spikes. This accurately represents the capacitor current as long as the rectifier contribution is negligible. The difference in magnitude can be attributed to the output ac current ripple

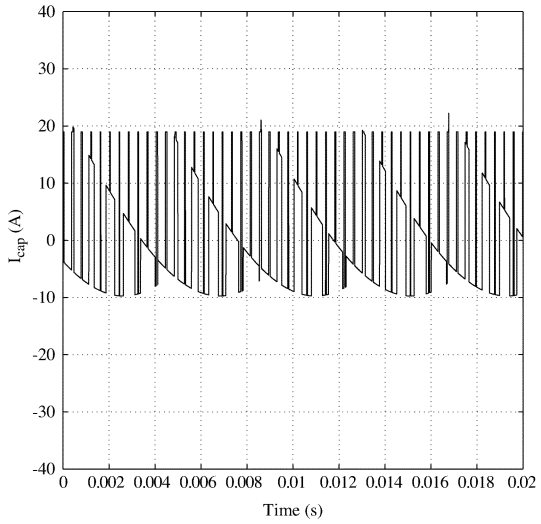


Fig. 7. Calculated capacitor ripple current waveform: CSR-fed inverter, $V_{\rm dc} = 228$ V, 40-Hz fundamental, 75% rated motor torque load.

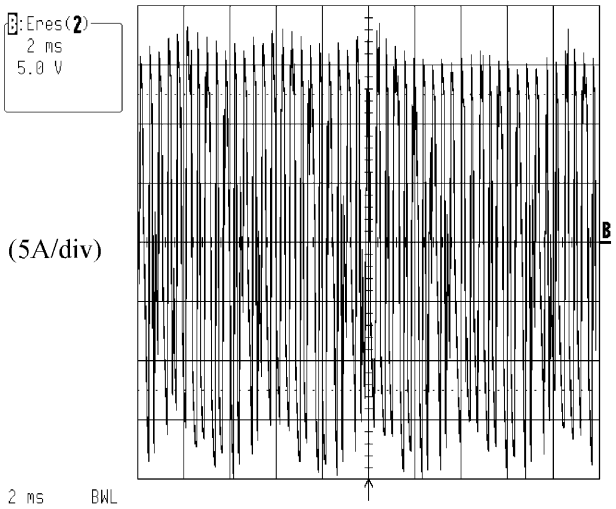


Fig. 8. Experimental capacitor ripple current waveform: diode-fed inverter, 40-Hz fundamental, 75% rated motor torque load, 3-bit enhanced resolution.

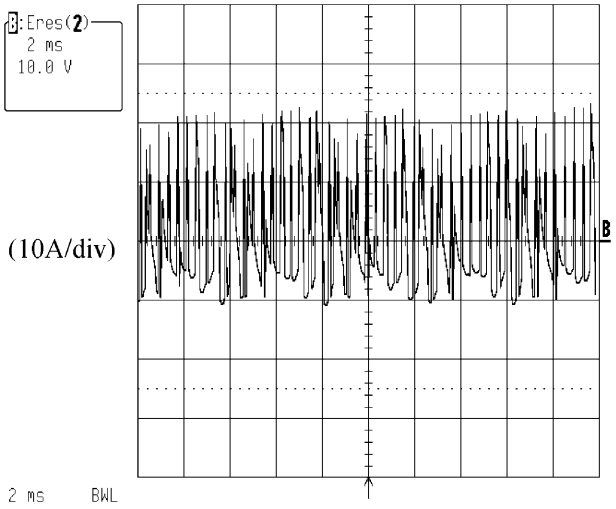


Fig. 9. Experimental capacitor ripple current waveform: CSR-fed inverter, $V_{\rm dc} = 228$ V, 40-Hz fundamental, 75% rated motor torque load, 3-bit enhanced resolution.

due to the $L_\sigma\ di/dt$ of the induction motor coupled to the low switching frequency (1225 Hz).

From the time-domain capacitor current calculated above the vectors of rms harmonic components are calculated using the MATLAB $fft()$ function as

$$I_{{\rm cap}h} = \frac{|fft(I_{\rm cap})|}{\sqrt{2}\cdot\frac{N}{2}} \tag{6}$$

where $N$ is the number of points in the time vector $I_{\rm cap}$. The total ripple current rms value can then be determined from the $N_h$ frequency components in the harmonic spectrum as

$$I_{\rm cap,rms} = \sqrt{\sum_{n=1}^{N_h} I_{{\rm cap}h,n}^2}. \tag{7}$$

This was then compared with the following per-unit equation [4], [5] as a further verification of the calculations:

$$\begin{aligned} I_{\rm cap,rms,pu}^2 &= \frac{I_{\rm cap,rms}^2}{I_{1rms}^2} \\ &= \frac{M_i}{4\pi}\left[2\sqrt{3} + \left(8\sqrt{3} - \frac{9\pi}{2}M_i\right)\cdot\cos^2(\phi)\right] \end{aligned} \tag{8}$$

where $I_{1rms}$ is the fundamental induction motor current. The maximum error between the two calculations was approximately 4% at full speed and load for both the constant $V_{\rm dc}$ and adjustable $V_{\rm dc}$ cases.

The rms capacitor currents are calculated for loads from zero to rated torque and excitation frequencies from 5 to 55 Hz. The minimum excitation frequency for each load condition was determined from the induction machine parameter calculated torque/speed curves by the torque at maximum slip. Since no voltage boosting was applied at low frequency the peak torque was reduced at lower speeds due to the increased relative effect of the rotor resistance.

The resulting current ripple from calculation and experimental measurements are shown in Figs. 10–13. The experimental and calculated results match quite well for both the constant $V_{\rm dc}$ case fed by a diode bridge rectifier and the varying $V_{\rm dc}$ case fed by a CSR. Most importantly they match for the high load condition. In Figs. 11 and 13 it can be seen that when $M_i$ was held constant in the PAM/PWM drive the ripple current becomes nearly flat over the entire speed range. This is important from the perspective of capacitor sizing, since now one need only consider the ripple current at the rated speed and load. The maximum value was also reduced by about 29%.

It can be seen that reducing $V_{\rm dc}$ and increasing $M_i$ to a high value results in much lower ripple current for the mid-range of frequencies. Experimentally, the maximum modulation index was limited to about $M_i = 1.07$ due to dead time and minimum allowed pulse width considerations for the insulated gate bipolar transistors (IGBTs) in the VSI.

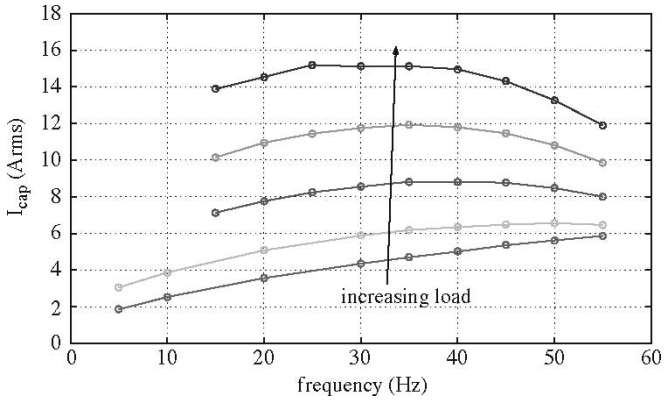


Fig. 10. Calculated rms electrolytic capacitor current with constant $V_{\rm dc} = 323$ V (diode-bridge fed) and varying modulation index.

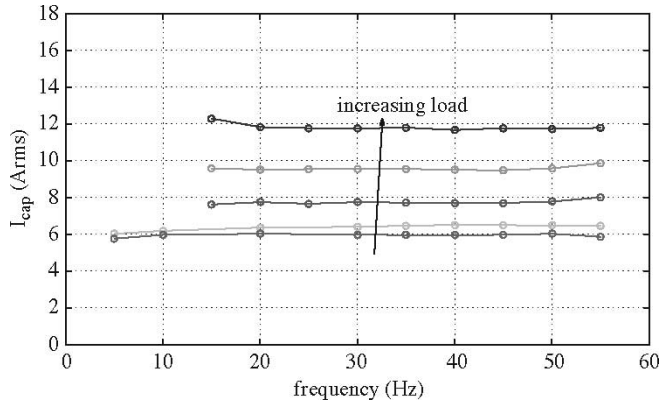


Fig. 11. Calculated rms capacitor current with varying $V_{\rm dc}$ (CSR fed) and constant modulation index $M_i = 1.07$.

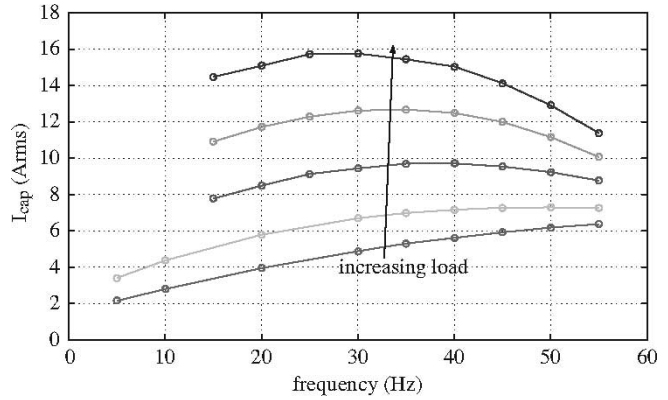


Fig. 12. Experimental rms capacitor ripple current with constant $V_{\rm dc} = 323$ V (diode-bridge fed) and varying modulation index.

## IV. Capacitor Loss Calculations

Using the capacitor current harmonic components from (6) the power loss is calculated by

$$P_{\rm loss} = \sum_{n=1}^{N_h} I_{{\rm cap}h,n}^2 \cdot ESR(f_n). \tag{9}$$

The dissipative losses were calculated for each set of harmonics produced from the ripple current calculation. Thus the full rated range of speed and load for the 10-hp induction machine was covered. In the standard ASD of Fig. 1 the dc-bus voltage was fixed at approximately 323 V with a variac so that at full speed the modulation index would be the maximum of 1.07. During variable dc-bus operation in the PAM/PWM ASD of Fig. 2 the modulation index was fixed at 1.07 while $V_{\rm dc}$ was varied from 30 to about 290 V.

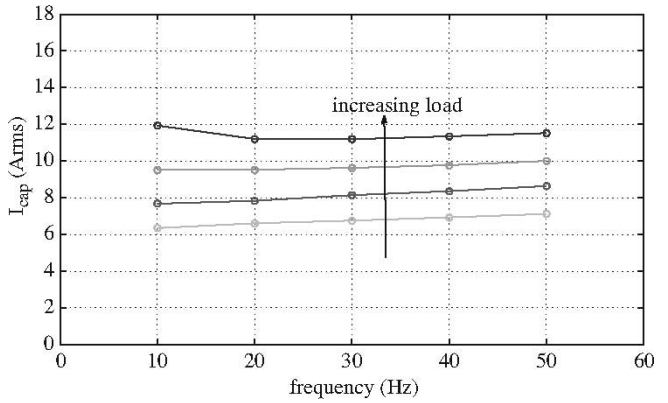


Fig. 13. Experimental rms capacitor ripple current with varying $V_{\rm dc}$ (CSR fed) and constant modulation index $M_i = 1.07$.

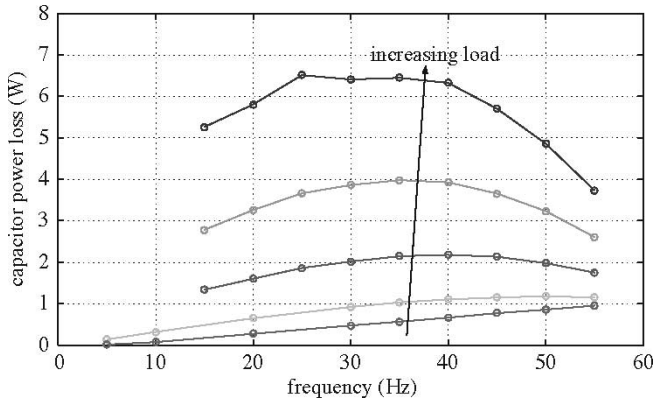


Fig. 14. Calculated capacitor power loss with constant $V_{\rm dc} = 323$ V (diode-bridge fed) and varying modulation index.

The experimental capacitor loss calculation was done using a LeCroy oscilloscope with mathematical functions to multiply the capacitor current and the ac part of the dc-link voltage. The mean value of the instantaneous power was than averaged over 20–30 sweeps. The dc-link voltage was measured using a precision high voltage differential amplifier ac coupled to the scope.

The calculated and experimental loss results are shown in Figs. 14–17. The standard ASD results match quite well in shape since the peak values occur at nearly the same frequency. The calculated results can be taken as a conservative estimate since they are slightly higher. For the varying dc-bus results all the curves are flat across the range of frequencies. The measured results are all lower than the calculated results due mainly to the temperature dependence of the electrolyte resistance, $R_1$, since it decreases with increasing temperature as shown in Fig. 5. The calculations were all done assuming one temperature. In the experimental setup the temperature increased under larger load decreasing the ESR and reducing the losses while under less load the temperature decreased increasing the ESR and increasing

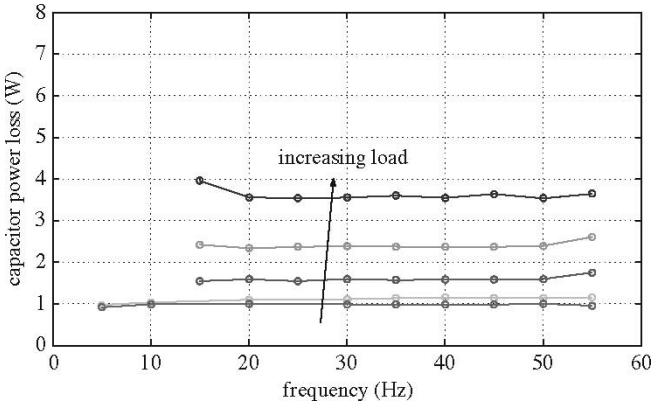


Fig. 15. Calculated capacitor power loss with varying $V_{\rm dc}$ (CSR fed) and constant modulation index $M_i = 1.07$.

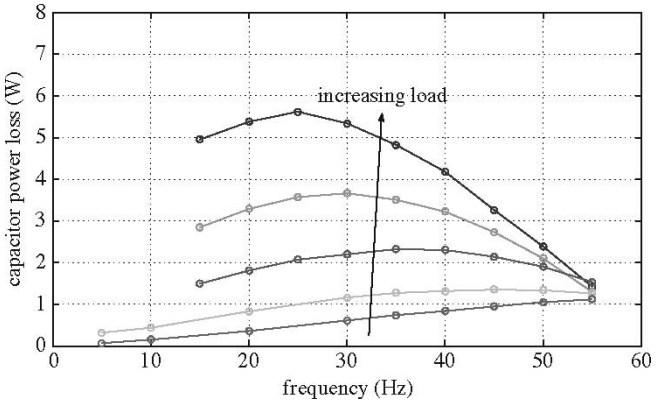


Fig. 16. Experimental capacitor power loss with constant $V_{\rm dc} = 323$ V (diode-bridge fed) and varying modulation index.

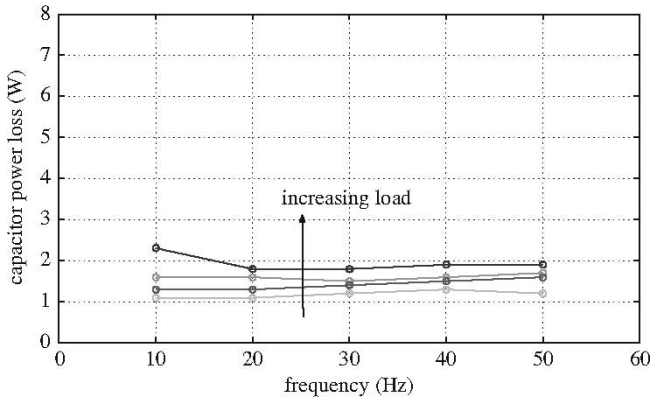


Fig. 17. Experimental capacitor power loss with varying $V_{\rm dc}$ (CSR fed) and constant modulation index $M_i = 1.07$.

the losses. This effect is especially noticeable in the PAM/PWM ASD power loss measurements where the range of losses with load is much less than for the calculated values.

As discussed earlier with the ripple current results it can be seen that in the mid-speed range the losses can be significantly reduced. The peak reduction for the calculated losses is about 55% and the peak reduction for the experimental results is about 70%. The ripple current rating of electrolytic capacitors is really a way of getting at the capacitor heating effect. Thus the power loss results give a better picture of the stresses on the capacitor.

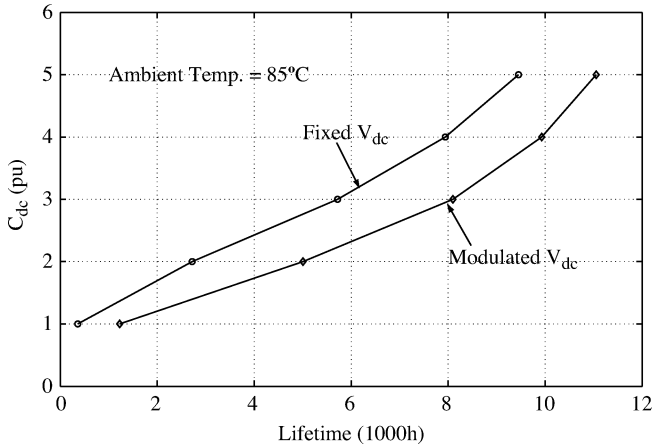


Fig. 18. Lifetime prediction of capacitor bank with $T_{\rm load} = 1.0$ pu and fundamental frequency = 30 Hz.

From the capacitor power loss results it can be seen that operation by varying the dc-bus voltage with speed can be advantageous for the electrolytic capacitor lifetime or sizing requirements. The increase in lifetime will depend on the typical drive duty cycle and whether it requires operation below base speed for a significant fraction of time. In terms of sizing considerations the reduction in peak capacitor losses depends on the range of modulation indices the drive will command.

To give an idea of the tradeoff involved in capacitor sizing a numerical calculation based on [2], [12] was performed. A per-unit dc-bus capacitance value of 470 $\mu$F was chosen based on the value of a single capacitor in the experimental setup capacitor bank. The induction machine load conditions were 50% speed and 100% load. The resulting curves of estimated lifetime versus amount of capacitance for the diode-bridge-fed ASD and the PAM/PWM ASD are shown in Fig. 18. To illustrate the meaning of this figure an example capacitor bank with four electrolytic capacitors (i.e., 4 pu in the figure) is considered. In a standard drive with fixed $V_{\rm dc}$ the estimated lifetime would be about 8000 hours of continuous use. In the PAM/PWM drive with modulated $V_{\rm dc}$ the lifetime would be improved by about 25%. On the other hand you could remove one capacitor (or 25% of the bank) from the PAM/PWM drive and still have a lifetime of about 8000 h.

## V. PAM/PWM Controller

In this section the controller used in the analysis of the preceding sections for the PAM/PWM drive of Fig. 2 is developed. The controller is partitioned in two sections with each section implemented on a separate digital signal processor (DSP) board. As seen in Fig. 19 DSP1 is comprised of the VSI controller and the DSP2 contains the CSR controller.

The dc-link voltage command for the CSR controller is essentially linearly proportional to commanded speed. To ensure a minimum reasonable dc-bus voltage based on minimum startup torque requirements the commanded bus voltage $(V_{\rm dc}^*)$ had a lower limit of about 30 V. The upper limit is determined by the utility line voltage magnitude and the need to operate the CSR in the linear modulation region. Power quality requirements for unity power factor and minimal current distortion will decide

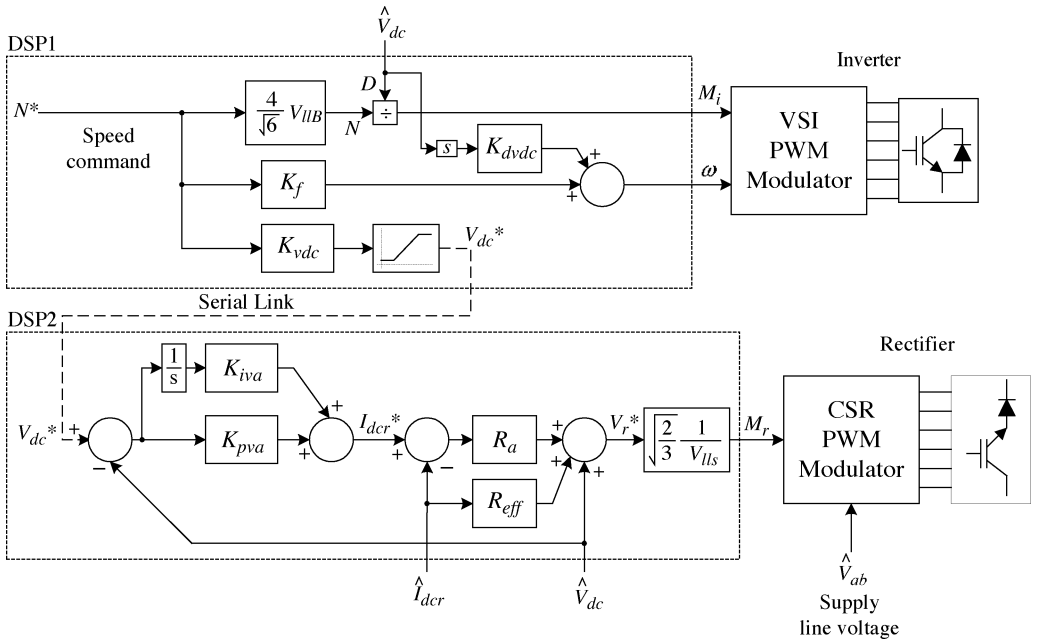


Fig. 19. Implemented two-DSP controller for PAM/PWM motor drive: VSI with $V_{\rm dc}$ compensation of modulation index for open-loop V/f control and $V_{\rm dc}^*$ generation, CSR with closed-loop PI voltage regulator.

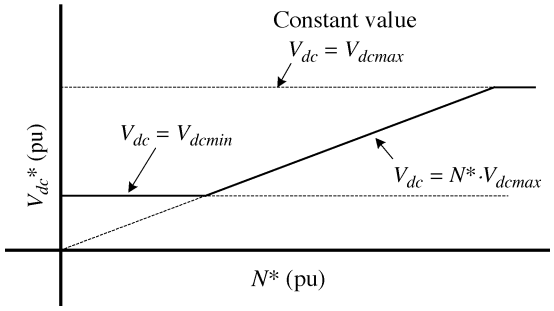


Fig. 20. Per-unit dc-bus voltage command $(V_{\rm dc}^*)$ versus speed $(N^*)$ generated in VSI controller and sent serially to CSR controller.

the importance of the second condition. The general form of the voltage command is shown in Fig. 20.

The hardware controller is based on two TI DSP boards, one for the rectifier and one for the inverter. The inverter determines the dc-link voltage command for the rectifier based on the commanded speed. In order to minimize the amount of communication between the two controllers the modulation index for the VSI is adjusted automatically based on the desired output voltage and the measured bus voltage $\hat{V}_{\rm dc}$ according to

$$M_i = N^* \cdot \frac{4}{\sqrt{6}} \cdot \frac{V_{llB}}{\hat{V}_{\rm dc}} \tag{10}$$

where $V_{llB}$ is the base line to line machine voltage and $N^*$ is the per-unit speed command.

The voltage command $V_{\rm dc}^*$ received from the inverter drives the controller in the rectifier. An outer loop proportional $(K_{pva})$/integral $(K_{iva})$ regulator is used to control the dc-link voltage. The inner loop consists of an active resistance proportional $(R_a)$ controller on the rectifier current $I_{\rm dcr}$. The parasitic resistance of the dc-bus inductor $R_{\rm dc}$ and the link voltage $V_{\rm dc}$ are also decoupled from the command voltage $V_r^*$ so the PI voltage controller only responds to voltage errors [10]. The "^" indicates a measured or estimated value. Finally, the modulation index $M_r$ is produced from the rectifier voltage command $V_r^*$ by the equation [11]

$$M_r = V_r^* \cdot \sqrt{\frac{2}{3}} \cdot \frac{1}{V_{lls}} \tag{11}$$

where $V_{lls}$ is the line to line supply voltage.

The maximum value of $M_r$ depends on how much distortion is acceptable to the utility. To have the least distortion $M_r$ should be limited to 1.0. This also limits the maximum dc-bus voltage to around 280 V with a line-to-line utility supply voltage of 230 Vrms. This can be increased by going into overmodulation as with a VSI, but at the price of input current distortion.

## VI. Conclusion

Investigations have been made into the effect of varying the link voltage $V_{\rm dc}$ with speed and holding the modulation index $M_i$ constant in an induction motor V/f drive. Comparisons were made between a standard diode-bridge-fed ASD with a fixed link voltage and a CSR-fed ASD with an adjustable link voltage. It has been shown through numerical calculations that the peak ripple current in the dc-bus electrolytic capacitor can be significantly reduced in the PAM/PWM drive. Further it has been shown that the effective heating due to the power loss in the ESR can be reduced even further because of the strong frequency dependence of the ESR. These results were verified by measurements made on a 7.5-kW motor drive.

The reduced heating stresses on the electrolytic capacitor bank can lead to increased lifetime. Depending on the driving factors for a particular drive the capacitance of the electrolytic capacitor bank can instead be reduced. A numerical calculation was made based on a method reported in the literature to concretely demonstrate the tradeoff.

Finally a topology for realizing the varying dc-bus voltage has been described. A controller has been implemented for the overall PAM/PWM converter and demonstrated driving an induction machine. The type of applications where this mode of operation could be useful would involve operation below base speed at high load levels for a significant portion of their load profile. Some examples include: electric cranes, electric vehicles, off-road electric construction equipment, and compressor pumps.

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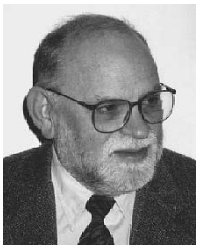

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