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Reduction of parasitic capacitance in 10 kV SiC MOSFET power modules using 3D FEM

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Keywords

≪Packaging≫, ≪Simulation≫, ≪Wide bandgap devices≫, ≪Silicon Carbide (SiC)≫

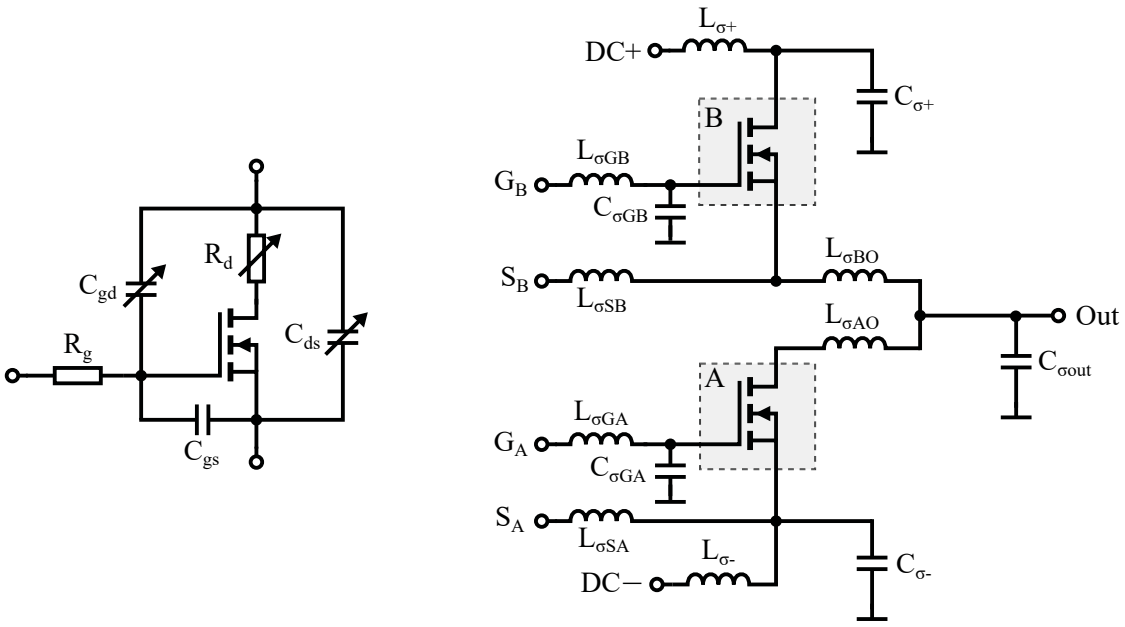
Abstract

The benefits of emerging wide-band gap semiconductors can only be utilized if the semiconductor is properly packaged. Capacitive coupling in the package causes electromagnetic interference during high dv/dt switching. This paper investigates the current flowing in the parasitic capacitance between the output node and the grounded heat sink for a custom silicon carbide power module. A circuit model of the capacitive coupling path is presented, using parasitic capacitances extracted from ANSYS Q3D. Simulated values are compared with experimental results. A new iteration of the silicon carbide power module is designed, having reduced capacitive coupling without penalizing other parameters. The new module is tested experimentally, which verifies the reduced capacitive coupling to the heat sink.

Introduction

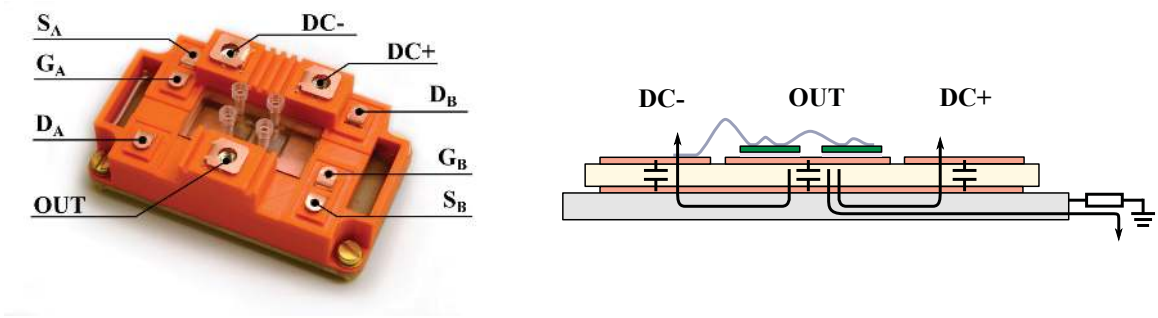
Emerging wide-band gap semiconductors, such as silicon carbide (SiC) MOSFETs, offer higher breakdown voltage, faster switching speeds and increased operating temperatures, when compared to their silicon counterparts [1], [2]. The capability of a semiconductor to switch fast is influenced by both parasitic inductances and capacitances, introduced by the semiconductor die itself and the package. Fig. 1a shows parasitic capacitances and main resistances of the semiconductor die. A more detailed model is obtained when considering the parasitic inductances of the package, i.e. copper tracks, terminal pins and bond-wires. Furthermore, direct bonded copper (DBC) planes are only separated from the grounded heat sink by a 0.63 mm aluminium nitride (AlN) substrate layer, causing the Cu-AlN-Cu layers to act as capacitors. Including these parasitic capacitances and inductances, a circuit model of a half-bridge module is shown in Fig. 1b, in which the semiconductor die parasitics are included in the MOSFET symbols. This model describes the power module during switching transients.

A half-bridge power module with 1st generation 10 kV / 10 A SiC MOSFETs from Wolfspeed is designed and packaged at the Department of Energy Technology, Aalborg University. The module, with baseplate dimensions 104 mm x 59 mm, is shown in Fig. 2a. Package design for low inductance has been studied extensively in literature by the use of Finite Element Method (FEM) software [3]-[7]. During double



(a) (b)

Fig. 1: (a) Parasitics of the SiC MOSFET die and (b) parasitics added by the packaging.



(a) (b)

Fig. 2: (a) Photograph of designed module and (b) principle diagram of capacitive coupling paths.

pulse testing of the module, large current flowing from the output node to the heat sink is observed, as indicated in Fig. 2b. The high voltage potential and fast switching of the output node, is coupled to the grounded heat sink through parasitic capacitances $C_{\sigma out}$ and $C_{\sigma GB}$. This displacement current does not flow laterally through the copper tracks and bond wires, and thereby bypasses main inductances of the switching circuit model in Fig. 1b. The currents conduct to both the DC-link and through gate drive circuitry [8], and causes electromagnetic interference (EMI) issues which limits the switching speed of the circuit [9], [10]. O. Kreutzer et. al. [11] suggests the use of a Y-capacitor to suppress this EMI, but in this paper efforts are on mitigating the root cause.

The aim of this paper is to design a power module with low capacitive coupling between the output node and the heat sink. Circuit diagrams and simulation tools are used and verified to aid the design of a new module. The new power module should be designed without penalizing other parameters. After packaging, the module is tested experimentally to evaluate the effect of the proposed changes.

Design of simulation model and experimental platform

The parasitic capacitances, of the module shown in Fig 2a, are evaluated in ANSYS Q3D and listed in Table I. In order to evaluate the simulation, a double pulse test is used to compare simulated parasitic capacitances and experimental results. In this test the voltage on the heat sink is measured, as a direct measure of the capacitive coupling between top and bottom side DBC planes.

Table I: Simulated parasitic capacitances of the SiC power module on 0.63mm ceramic

Parasitic	$C_{\sigma+}$	$C_{\sigma out}$	$C_{\sigma-}$	$C_{\sigma GB}$	$C_{\sigma GA}$
Value	101 pF	149 pF	45 pF	19 pF	22 pF

In addition to the calculated values of the module, contributions from the experimental setup are included. A cooling fan is mounted on the heatsink and the voltage is measured with a high voltage Lecroy PPE probe. The capacitive coupling to the fan is measured as 80 pF using a Keysight E4990A impedance analyzer. The datasheet of the voltage probe states 6 pF of coupling to ground. Thus a total auxiliary contribution of 86 pF is added to the model. When currents flow as in Fig. 2b, the main parasitic inductances, i.e. copper tracks and bond wires, of Fig. 1b must be ignored. Neglecting inductances, the simplified model of the system based only on capacitive values evaluated in ANSYS Q3D is shown in Fig. 3. Currents through capacitances $C_{\sigma GB}$ and $C_{\sigma GA}$ are critical, as they may influence vulnerable gate

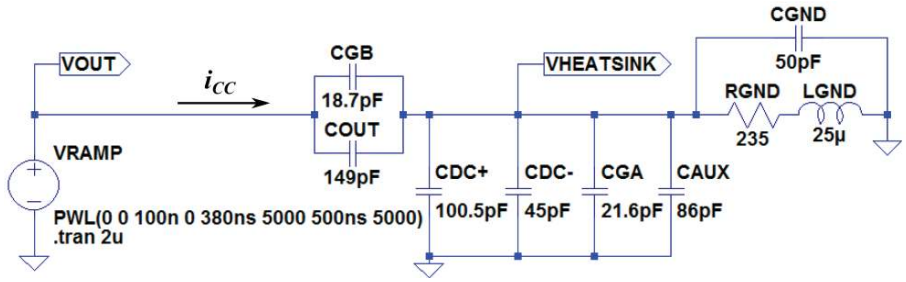


Fig. 3: LTSpice model to simulate heatsink voltage and current.

driver circuitry and control signals. From (1), mitigating the coupling current is done by reducing the capacitive coupling and ensuring slow transients of voltage to the heat sink, but it is not desirable to slow the switching speed of the MOSFETs.

$$i_{CC}(t) = (C_{\sigma GB} + C_{\sigma out}) \cdot \frac{\mathrm{d}(V_{out} - V_{heatsink})}{\mathrm{d}t} \tag{1}$$

The heat sink is grounded using a power resistor to provide damping, and is modelled by a resistance R_{gnd} = 235 Ω, in series with an inductance of L_{gnd} = 25 µH and has a parallel parasitic capacitance of C_{gnd} = 50 pF. Alternatively, grounding with a short wire, modelled by a series RL-circuit of 0.1 mΩ and 200 nH, could be used. LTSpice simulations of heat sink voltage and combined capacitive coupling current, i_{CC}, for the chosen grounding resistor and the case of undamped short wire is shown in Fig. 4.

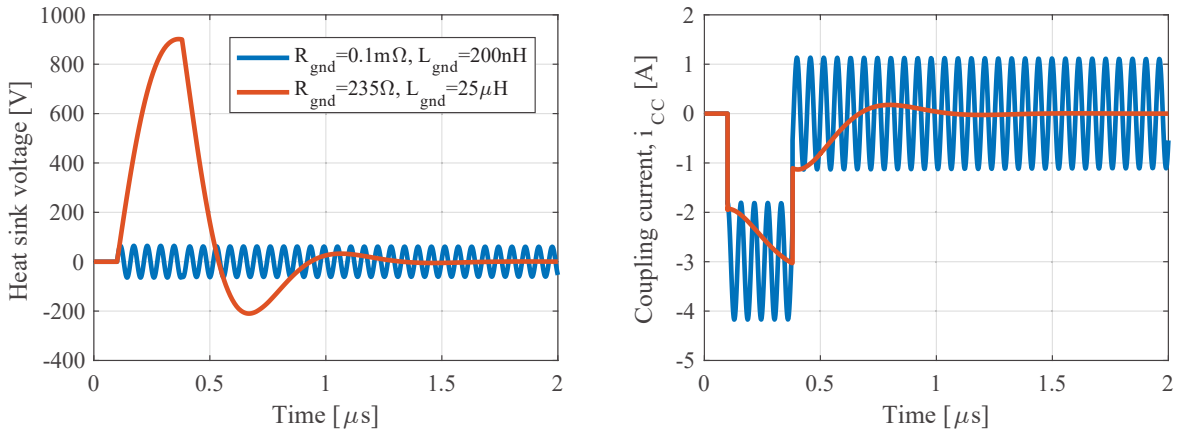


Fig. 4: LTSpice simulation results of heatsink voltage (left) and current (right) for damped and undamped grounding impedance, during a double pulse test at 5 kV switching in 280 ns (18.2 kV/µs)

The results show that the amplitude of the current flowing through the baseplate is driven by (1). This current passes through gate drive and control circuitry, resulting in reduced signal integrity and undesirable noise in grounding planes. The simulation also shows that the higher resistance causes damped transients but increases the amplitude of the heat sink voltage. On the other hand the low resistance reduces heat sink voltage amplitude, but causes undamped ringing which in turn causes current to continuously flow. Since the latter way leads to system instability, the 235 Ω high voltage resistor is chosen for further experiments.

Experimental validation of FEM

The LTSpice model based on capacitances evaluated in ANSYS Q3D is verified using a double pulse test at a DC-link voltage of 5 kV. An experimental test bench was designed to ensure robust operation during high voltage switching [12]. The SiC power modules are powered from custom designed gate driver supplies [13], due to high coupling capacitance in commercially available medium voltage DC-DC supplies [14]. Voltages of the half-bridge output and heat sink are measured as depicted in Fig. 5. The LTSpice simulation results are also shown with and without the influence of the auxiliary voltage probe and heat sink fan. There is very good agreement between the experimental results and the LTSpice

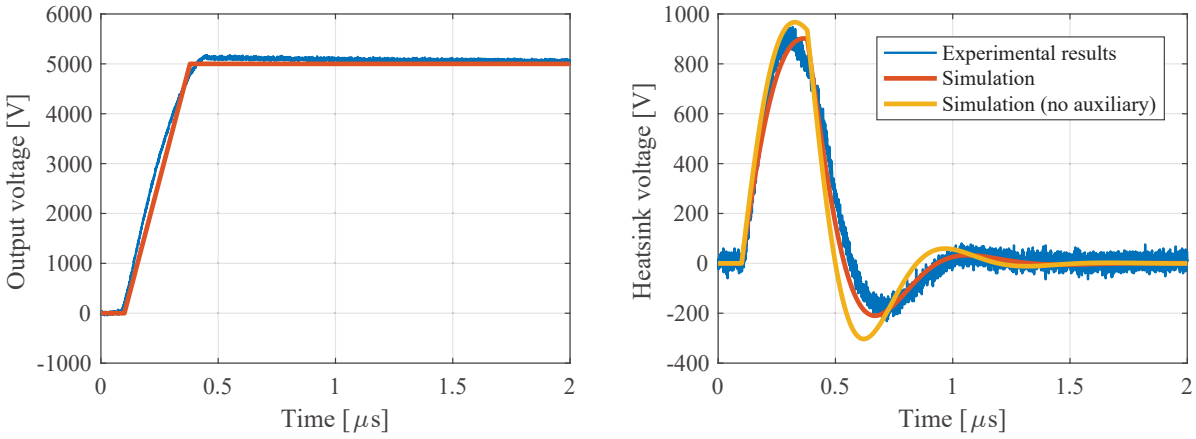


Fig. 5: Half-bridge output voltage (left) and heat sink voltage (right) during 18.2 kV/μs switching measured experimentally and from LTSpice simulation (with and without influence of auxiliary equipment).

simulation, which is based on the capacitances obtained in ANSYS Q3D. This result verifies the quantitative accuracy of using ANSYS Q3D in the further design of the power modules. The results also prove the importance of a proper experimental test setup, and that the influence of auxiliary equipment, such as the probe and fan, is taken into consideration.

Developing new design by FEM

The power module design is modified to reduce the parasitic coupling capacitance, without penalizing other parameters excessively. The design is improved by reducing the outer dimensions of the DBC, and by making an overall more compact layout. A total parasitic capacitance of 98 pF is achieved ($C_{\sigma out}$ of 86 pF and $C_{\sigma GB}$ of 12 pF), which is a reduction of 41 % compared to the initial 168 pF. Still a relatively large part of the surface area of the output plane is used to connect to the source terminal S_B of the module. This track was initially kept wide to ensure low parasitic inductance in the gate-source loop. It is desirable to reduce the width of the plane, to reduce the parasitic capacitance, but without increasing the parasitic inductance considerably. The portion of the plane to be removed is marked as the pink area in Fig. 6. A parametric sweep for the width of the cutout is performed from 0 mm to 7 mm. The parasitic resistance and inductance of three critical paths are monitored. The three paths are: from DC+ to the output terminal, from DC- to the output terminal and the affected gate-source loop of MOSFET B. In this calculation die parameters are excluded i.e. for evaluating the DC+ to output loop the drain and source pads of the MOSFET die are shorted. The results for output capacitance and parasitic inductance and

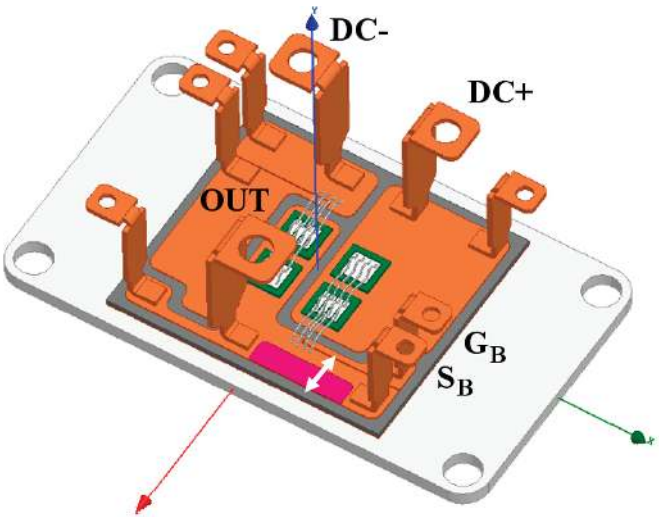


Fig. 6: ANSYS Q3D model for parametric analysis of reduced Cu track width.

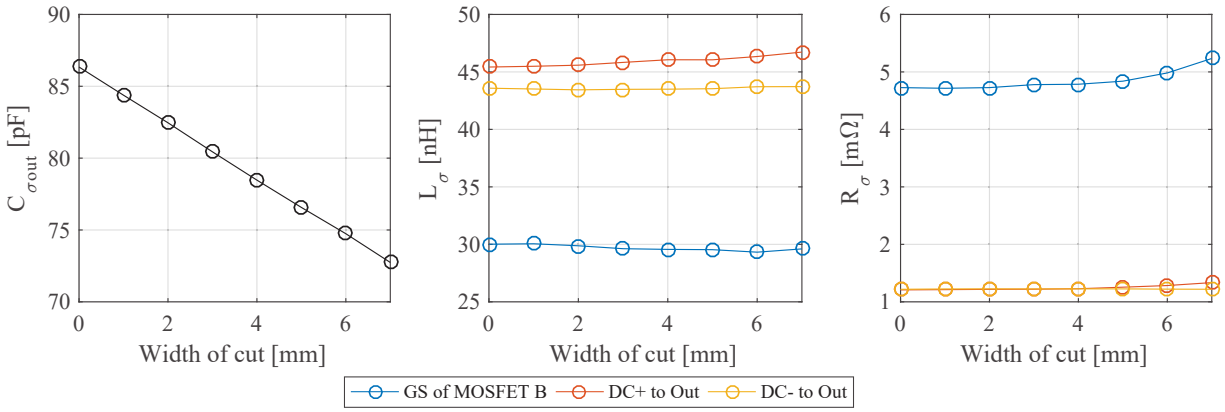


Fig. 7: $C_{\sigma out}$, L_σ and R_σ as a function of the reduced plane width for three critical paths

resistance in the three paths considered are shown in Fig. 7. In ANSYS Q3D low frequency inductances and resistances are evaluated by assuming uniformly distributed current thus neglecting skin effect.

The capacitance is linearly decreasing as the width of the cut is increased, but the parasitic inductance and resistance for all considered current paths are almost constant. Gate-source resistance is mostly affected, but the magnitude is small compared with the gate resistance of the die. At the width of 7 mm to be removed, the remaining track to the source terminal is only 1 mm wide. For manufacturing purposes this is considered the minimum track width for etching of the DBC. At this width the total parasitic capacitive coupling from the output to the heat sink is 85 pF ($C_{\sigma out}$ of 73 pF and $C_{\sigma GB}$ of 12 pF). This is a further reduction of 13 %, without penalizing other parameters. Capacitive couplings from power module planes to the heat sink for the new design are listed in Table II. This is the design which is manufactured.

Table II: Simulated parasitic capacitances of the new SiC power module on 0.63mm ceramic

Parasitic	$C_{\sigma+}$	$C_{\sigma out}$	$C_{\sigma-}$	$C_{\sigma GB}$	$C_{\sigma GA}$
Value	65 pF	73 pF	32 pF	12 pF	33 pF

In case the design changes proves not to be sufficient to ensure robust operation, modifications to the materials is proposed. The DBC master cards used for the power modules are commercially available with AlN ceramic substrate thickness of 0.63 mm and 1 mm. The increased thickness decreases the capacitive coupling. In an ANSYS Q3D simulation, using a 1 mm substrate layer instead of 0.63 mm reduces the total parasitic capacitance ($C_{\sigma out}$ + $C_{\sigma GB}$) from 85 pF to 57 pF. However, the increased

thickness of AlN substrate layer also impacts the thermal resistance. A model of the structure from SiC MOSFET die to heat sink is simulated in COMSOL to evaluate the thermal resistance. FEM is used to account for changing thermal spread angles, caused by the difference in thermal conductivity of each layer [15]. Fig. 8 shows the temperature distribution throughout the layers at a heat sink temperature of 45 °C, and an average power dissipation level of 55 W per die (estimated from a double pulse test at 5 kV, 5 A). The thermal resistance from junction to heatsink for a thickness of 0.63 mm is evaluated to 0.30 $\frac{K}{W}$, and increases to 0.32 $\frac{K}{W}$ for a thickness of 1.0 mm ceramic. The penalty of increasing the thickness of the ceramic is only 6 %, due to the relatively high thermal conductivity of 150 $\frac{W}{m \cdot K}$ for AlN ceramic [16]. The increased thickness of the ceramic was not implemented, as the main scope is to document the influence of modified DBC layout.

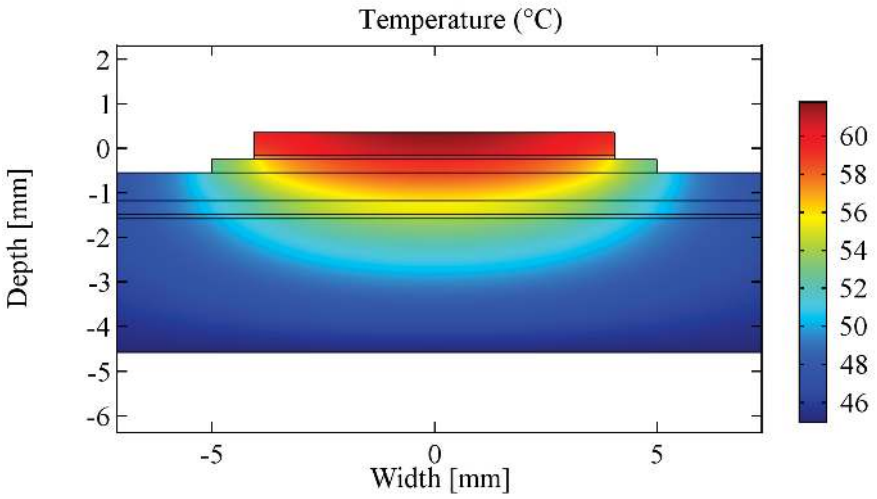


Fig. 8: Thermal distribution throughout power module layers simulated in COMSOL.

Experimental results

The new improved power module with 0.63mm ceramic thickness was manufactured and packaged, and is shown in Fig. 9. The power module is populated with 3rd generation Wolfspeed 10 kV / 17 A SiC MOSFET dies. An important improvement in the new generation die is that it has higher gate-source threshold voltage. This change makes it less vulnerable to noise and parasitic turn on. The improved

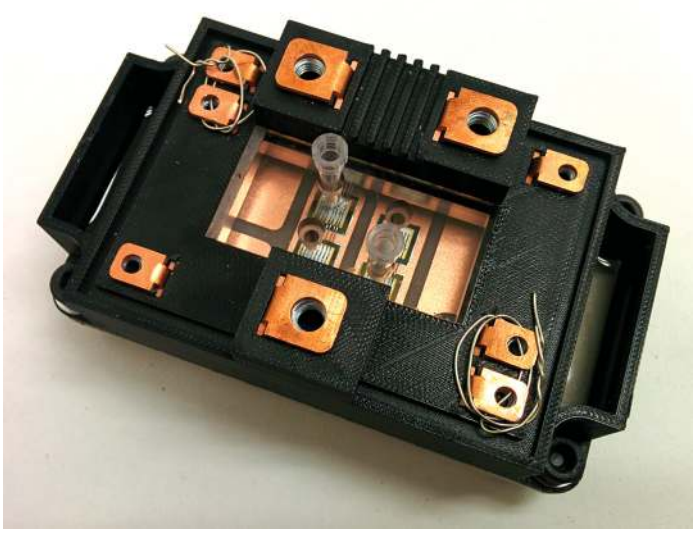


Fig. 9: Photograph of the new improved power module.

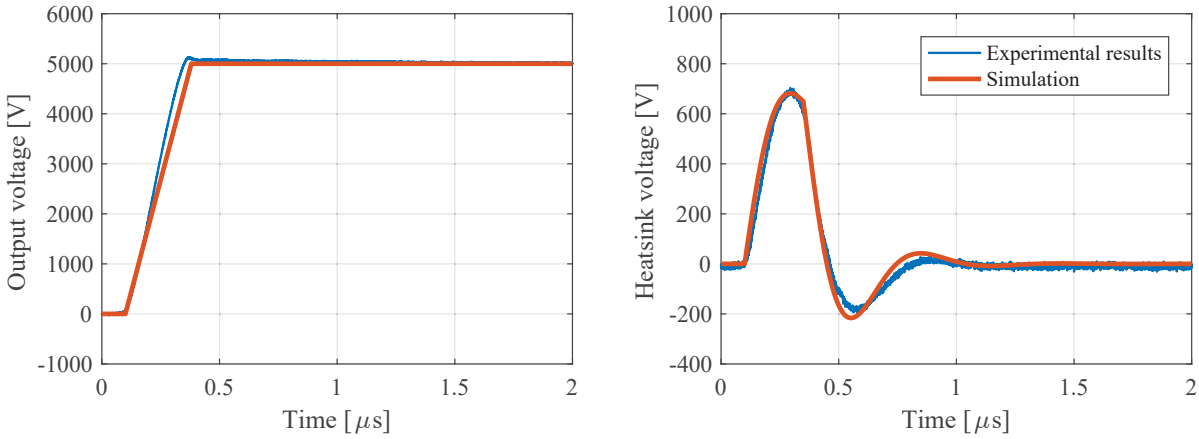


Fig. 10: Experimentally measured half-bridge output voltage (left) and heat sink voltage (right) during 21.0 kV/μs switching of new module.

DBC layout and higher robustness of the MOSFET die allows the new test to be done at a switching speed of 21.0 kV/μs. The output voltage and the heat sink voltage during the test are shown in Fig. 10. As in Fig. 5 an excellent quantitative agreement between simulation and experiment is observed. The new module is switching 15 % faster, while the amplitude of the heat sink voltage is reduced by 26 %, when compared to the old module in Fig. 2a.

Conclusion

The high voltage breakdown and fast switching speed of SiC MOSFETs put further demand on low capacitive coupling in power module packaging. A model of parasitic coupling capacitances was evaluated for a SiC MOSFET power module using ANSYS Q3D. A double pulse test verifies the agreement between experimental tests and simulation. The result justifies the use of ANSYS Q3D for further design improvements.

The paper proposes design modifications which reduces the parasitic capacitive coupling. Smaller DBC dimensions and reduced track widths reduces the total output coupling capacitance from 167 pF to 85 pF, which is experimentally verified. A further reduction from 85 pF to 57 pF is proposed by increasing ceramic thickness, at the expense of slightly increased thermal resistance. The results also show that coupling between power module and heat sink can be directly observed through measurement of the heat sink voltage.

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