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Reduction of Short-Channel Effects in FinFET

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Abstract*— An application of FinFET Technology has opened new development in Nano-technology. Simulations show that FinFET structure should be scalable down to 10 nm. Formation of ultra thin fin enables suppressed short channel effects. It is an attractive successor to the single gate MOSFET by merit of its superior electrostatic properties and comparative case of manufacturability process. Inventing new device is always essential to improve the circuit performance; the total steps are more than usual MOSFET process, but the cost of material is smaller. Since it is more compact, using FinFET is economical. The leakage current due to DIBL was well suppressed and the roll-off of a FinFET is well controlled.

***Index Terms*— DG-FET, DIBL, etches, FinFET, GIDL, hysteretic threshold, parasitic bipolar effect, roll-off, short channel effects, Threshold Voltage.**

I. INTRODUCTION

As the fabrication techniques developed day by day, the channel length has been shrinking continuously to its minimum in MOSFET. The smaller channel length results high speed of operation and increases the components per chip. The sustained scaling of conventional bulk device requires innovative methods to avoid the barriers of fundamental physics constraining the conventional MOSFET device structure. The most often cited limitations are location of dopants providing high I_{on}/I_{off} ratio and control of the density, quantum-mechanical tunneling of carriers through thin gate from drain to source and from drain to body and finite sub-threshold slope [1]. The channel depletion width must scale with the channel length to contain the off-state leakage I_{off}. This leads to high doping concentration, which reduces the carrier mobility and causes junction edge leakage due to tunneling. The gate oxide thickness t_{ox} must also scale with the channel length to maintain gate control, proper threshold voltage V_T and performance. The thinning of the gate dielectric results in gate tunneling leakage, degrading the circuit performance, power and noise margin. The short channel effects arise due to drift of electron characteristics in the channel and change in the threshold voltage due to shrinking in the channel length. The short-channel effect is controlled by geometry and the off-state leakage is limited by the thin silicon film in these SOI devices. For an effective suppression of the off-state leakage, the thickness of the Si film must be less than one quarter of the channel length [2]. The desired V_T is achieved by manipulating the gate work function, such as the use of mid gap material or poly-SiGe. Concurrently, material enhancements, such as the use of i) high-k gate material and ii) strained silicon channel for mobility and current drive improvement, have been actively performed [3]. As scaling changes it directly affects its physic, performance and new circuit design issues continue to be presented. Design challenges of these emerging technologies with particular emphasis on the implications and impacts of individual device scaling elements and unique device structures on the circuit design [4]. We implemented planar device structures from continuous scaling of PD SOI to ultra-thin-body fully depleted (FD) SOI and new materials such as strained Si channel and high-k gate dielectric and Gate Oxide Tunneling Leakage, Self heating, Soft Error Rate. The Partially depleted floating-body MOSFET was the first SOI transistor generically adopted for high-performance applications, primarily due to device and processing similarities to bulk CMOS device. Due to bulky structure of CMOS device short channel effects have been increased [5]. The PD SOI device is largely identical to the bulk device, except for the addition of a buried oxide ("BOX") layer. The active Si film thickness is larger than the channel depletion width, thus leaving a quasi-neutral "floating" body region underneath the channel. The V_T of the device is completely decoupled from the Si film thickness, and the doping profiles can be tailored for any desired V_T [6] . The device offers several merits in its performance improvement:

1) Decreased junction capacitance,

2) Lower average threshold due to positive V_{BS} during switching.

3) Dynamic loading effects, in which the load device tends to be in high $V_{T\ state}$ during switching

Such performance comes at the cost of some design complexity resulting in floating body of the device, such as

1) Parasitic bipolar effect and
2) Hysteretic V_T variation.

In this paper, we focus Section II on hysteretic V_T variation. In Section III, introduces the process flow of FinFET. Section IV, proposed non planar FinFET. In Section V explains that the conversion of planar to FinFET. The experimental results for short channel effects are shown in Section VI. Finally, the concluding remarks are given in Section VII.

II. HYSTERETIC VT VARIATION

The hysteretic V_T variation exists due to long time constants of various body charging/discharging mechanisms [7]. A generally used estimation for hysteretic V_T variation (or "history effect" as it is known in the SOI community) is the disparity in the body voltages and delay between them is called "first switch" and "second switch". The "first switch" refers to the case where a circuit (e.g., inverter) starts in an initial an operating state with input "low" and then undergoes an input-rising transition. In this case, the initial dc equilibrium body potential of the switching nMOSFET is

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determined primarily by the balance of the back-to-back drain-to-body and body-to-source diodes. The "second switch" refers to the case where the circuit is initially in a quiescent state with input "high." The input first falls and then rises (hence, the name "second switch"). For this case, the pre-switch body voltage is determined by capacitive coupling between the drain and the body.

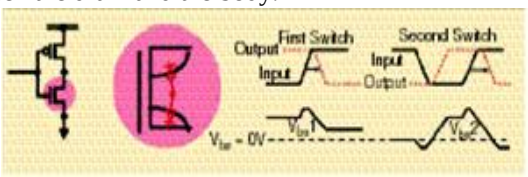
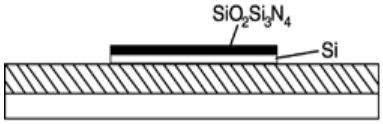


Fig.1. Input/Output Waveforms for Inverter.

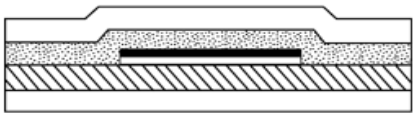
Fig. 1. Shows input/output waveforms and nMOS body voltage for a PD SOI CMOS inverter under "first switch" & "second switch" condition. The duty cycle, slew rate and output load all three affect the hysteretic behavior of the circuits. A much high duty cycle increases hysteretic behavior but a much faster switching activity causes loss of body charge and less time for the device to return/settle to its initial equilibrium state[8]. In order to reduce the short channel effects in the conventional MOS-FET, we used MOS-FET with double gate, which is known as FinFET. The main advantage of the FinFET is the ability to drastically reduce the short channel effect.

III. PROCESS FLOW OF FINFET

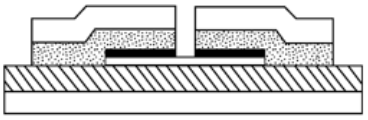
A conventional SOI wafer is taken as raw material (probably the best), except that the alignment notch of the wafer is rotated 45° about the axis of symmetry of the wafer. Because the conventional SOI is to provide {100} planes on silicon fins that are oriented along the conventional "x" and "y" directions on the wafer [9]. The process of defining fins source/drain silicon is very similar to that used to define trench isolation in modern CMOS. Patterns are defined and etched into the active top silicon layer in both processes. The conventional process requires additional processing to fill and planarize the isolation trenches; the FinFET process, on the other hand, it proceeds directly to channel processing, such as sacrificial oxidations, masked ion implantations for channels, or specialized passive elements, followed by the gate dielectric module. Gate deposition and etch are very similar, with less-severe demands on the selectivity of the gate-electrode etch to gate oxide, because the oxide surface is orthogonal to the etch direction [10]. An ion implantation of source/drain species and halos (or pockets) must differ for self-evident geometrical reason but otherwise are largely similar to conventional planar implantation steps. Conventional $CoSi_2$ or $NiSi_2$ processes are used to silicide the tops of the flat tableland with steep edges and the gate, for contacts to source/drain and gate, respectively. The short channel effects generally distinguished as Drain Induced barrier lowering (DIBL), punch through and surface scattering. Drain voltage (V_d) contributes to inverting the Channel, effectively reducing 'V_t' that in turns increasing current with increasing 'V_d'.



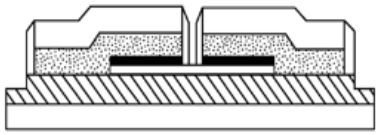
(1) After depositing Si_3N_4 and SiO_2 stacked layer. Si fin was formed.



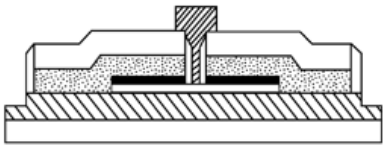
(2)Phosphorus-doped-poly Si and SiO_2 stacked layer deposited.



(3) Source and drain were etched while Si fin was covered by the mask layer.



(4) Spacer SiO_2 layer was etched down into buried oxide layer.



(5) After depositing B-doped SiGe, gate pattern was delineated.

IV. NON PLANNER FINFET

In the FinFET, silicon body is rotated on its edge into a vertical orientation so that only the source and drain regions are placed horizontally above the body, as in a conventional planar FET [11].

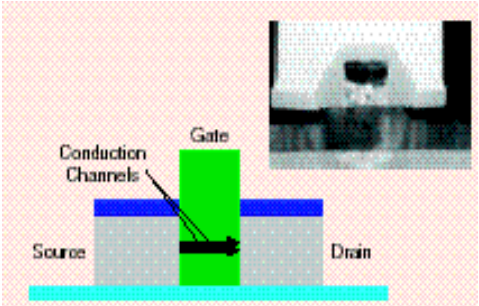


Fig.2. Cross Sectional View.

V. CONVERSION OF PLANER TO FINFET TECHNOLOGY

FinFET processing on SOI wafers uses standard manufacturing process modules. To etch the ultra thin

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(T_{SI}=15nm) fins, spacer lithography [side wall image transfer (SIT)] is used [12]. Since the SIT process always generates an even number of fins, an extra process step is needed for removal of fins to allow odd number of fins or otherwise break fin" "loops" where needed. That means, conversion of an existing design, two additional levels have to be introduced, namely the "fin" and the "Trim" level. All other design levels remain the same. Consider now a planar design which is to be converted for processing in the 90 nm FinFET technology node. The FinFET height H_{Fin} together with the fin pitch (determined by photolithography) defines the FinFET device width W_{Fin} within the given silicon width of the planar device, to get the same or better device strength [13]. For automatic Fin and Trim generation, Fin-GEN (software tool) has been developed, which takes the active area and poly gate levels, and, based on special FinFET ground rules, generates the additional levels. The circuit (as well as other β-ratio sensitive circuitry) may require manual adjustment on the number of fins in the N-devices and P-devices after automatic addition of fins in the N-devices and P- devices after automatic addition of the FinFET levels. Besides device width quantization, other factors like width, threshold variation, and self-heating must be taken into account when designing with FinFET. A process with multiple threshold voltages and multiple gate oxide thickness is required to take full advantage of this new device. The width quantization needs some restrictions on the device strength flexibility, but most of them can be absorbed easily when converting an existing design or starting a new design. Of course, as stated earlier, latches, dynamic circuit, and SRAM cells need careful optimization when designing with FinFET [14]. Discrete devices and circuits for analog applications require special attention. As an example, consider a driver/receiver circuit with an ESD protection diode. In a planar process the protection voltage is proportional to junction length of the diode [15]. In FinFET technology the same junction length per fin pitch may be nearly one-eighth of that of the planar device. Another example is that total output driver impedance matching, which is usually implemented with a planar resistor requiring a silicon block resistor, on a silicon island to adjust output impedance (including the wire to the pad) to 50 Ω[16]. For such applications, and analog circuits in general, special devices may be necessary for optimized designs using FinFETs.

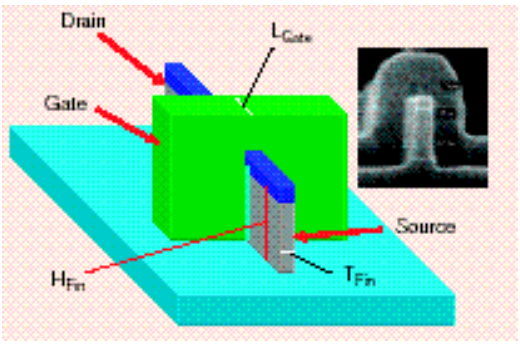

Fig.3. FinFET.

FinFET is designed to use multiple fins to achieve larger channel widths. Source/Drain pads connect the fins in parallel. As the numbers of fin are increased, the current through the device also increases. For example: A 3 fin device increases its current by 3 times to than single fin device. Planar DG-FETs have a most challenging thing is to deliver all of the first three requirements since the "second" gate is buried below a layer of active silicon. The fourth challenge is that planar DG-FET; a process module is required to define the additional contact to the buried gate if space is not to be lost for it specifically, and a low-resistance gate material must be introduced in the buried oxide so the challenge gets nearly removed [17]. Vertical DG-FETs typically address problems 1 and 4 quite successfully. In this case the gate length is usually defined by the thickness of a deposited gate-electrode material, which automatically makes both gates the same length and self-aligned to each other. Similarly, the source and drain junctions can be symmetrically defined to have the same alignment to both gates; however, unique challenges are presented to define both self-alignment of the bottom junction to the gates and to keep the parasitic series resistances associated with the bottom junction low. Furthermore, a space-efficient low-capacitance contact scheme to the lower junction requires a high-wire act in process integration. While high drive currents have been achieved with Type II structures, high performance (e.g., low capacitance) and CMOS integration have met with limited progress [18]. Vertical fin type DG-FET has the advantage to access both gates, and both sides of source and drain, from the front of the wafer. Gate length is conventionally defined since the direction of the current is in the wafer plane. Gate width, however, is no longer controlled by lithography [19]; rather, the width is given by twice the height of the silicon fin H_{Fin}. The Fig. 4 shows that the parts of FinFET in two-dimensional structure, which explains layout design with buried layer. This structure gives us best driving current in comparison to conventional MOSFET technology, and provides more compact in fabrication process [4],[5].

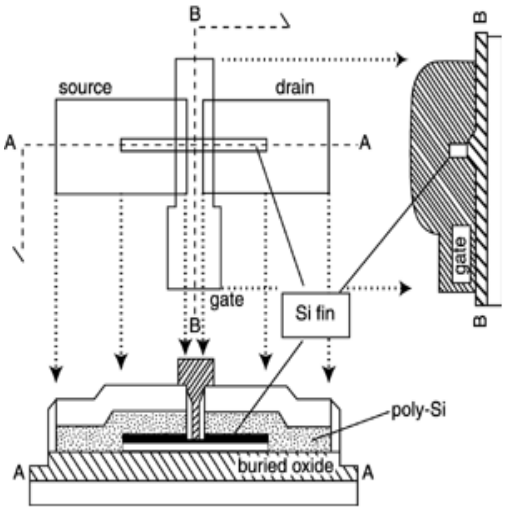

Fig. 4. Schematic Explaining the Parts of a Finfet.

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V. SIMULATION OF VERTICAL DOUBLE-GATE SOI MOSFETS USING DEVICE3D

The simulation methodology of a self-aligned double-gate MOSFET structure (FinFET) carried out by using SILVACO 3-D simulation suite. The MOSFET (double-gate) is one of the most attractive alternatives to classical MOSFET structure for gate length down to 20nm. In spite of his double-gate structure, the FinFET is closed to its root, the conventional MOSFET in layout and fabrication. 3-D numerical simulations of the FinFET are performed in this article, in order to validate the basic principles and to uncover several important aspects: evaluation of the length, width and quantum effects. The features of the structure are shown in Fig 6 are: (1) transistor is formed in a vertical ultra–thin Slicon fin and is controlled by a double-gate, which considerably reduced short channel effects, that we discussed previously; (2) the two gates are self aligned and are aligned to S/D; (3) S/D is raised to reduce the access resistance; (4) Up to date gate process: low temperature, high -k dielectrics can be used and (5) the structure is quasi-planar because Si Fin is relatively short. The basic characteristics of FinFET which we considered are T_{ox}=2nm length=50nm width=50nm and Fin height=50nm. Note that we have defined a parameterized structure for subsequent use in our automation tool, which make much easier any kind of variation (length, width) to perform large scale simulation. The main physical effects (mobility, carrier statistics and recombination) were expressed by a set of models universally used for simulating the MOS technology: mobility dependence of the electric field and doping level, Boltzmann statistics and Shockley-Read-Hall generation recombination mechanisms.

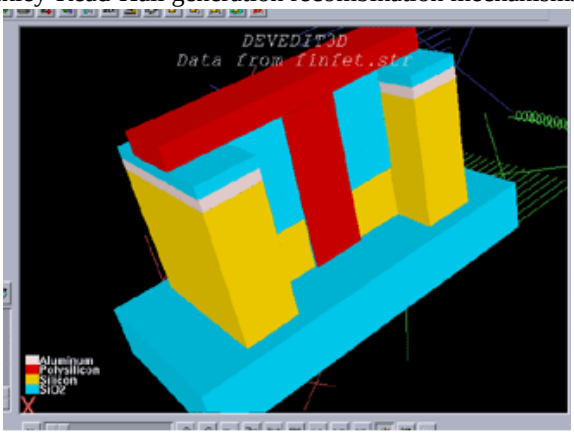

Fig.5. Plot of a 50-Nm Finfet 3-D Structure for a Width of 50nm.

Typical I-V characteristics of a 50-nm gate length are shown in Fig 6. The leakage current induced by DIBL was well suppressed. DIBL occurs when the depletion region of the drain interacts with the source near the channel surface to lower the source potential barrier. It happens when a high drain voltage is applied to a short-channel device, lowering the barrier height and resulting in further decrease of the threshold voltage. The source injects carriers into the channel surface without the gate playing a role. DIBL is increased at higher drain voltage and shorter effective channel length. Surface DIBL is happens before deep bulk punch-through. It decreases the threshold voltage. Hence the leakage current decreases.

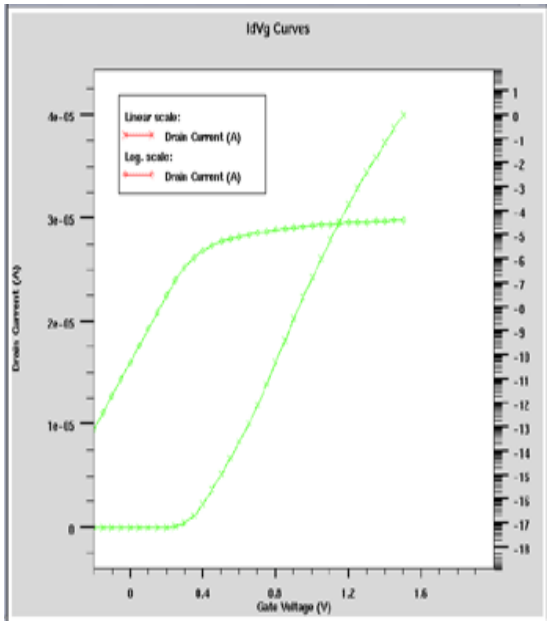

Fig.6. I_d Vs V_{gs} Curve With 50nm Technology.

The roll-off of a FinFET with a width of 50nm is well controlled as can be seen in Fig 7. This result can be correlated to the good control of the channel potential due to the double gate.

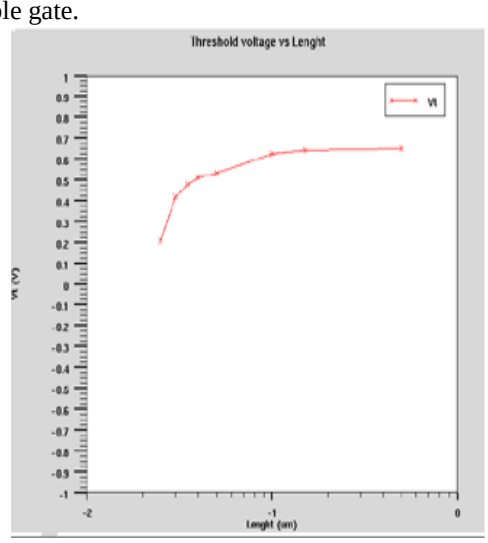

Fig.7. Threshold Voltage as A Function of Gate Length for A Width of 50-Nm.

The width of this FinFET is adjusted by the number of Si fins. If you want to double the width of your device then you have to put 2 Fins between sources and drain as shown in Fig. 5. As the channel length is reduced further, the threshold voltage of FinFET decreases. This reduction of threshold voltage with reduction of channel length is known as V_T roll-off the principal reason behind this effect is the presence of two-dimensional field patterns in short-channel devices, unlike the one dimensional field pattern in long-channel devices. This two-dimensional field pattern originates from

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the proximity of the source-drain region.

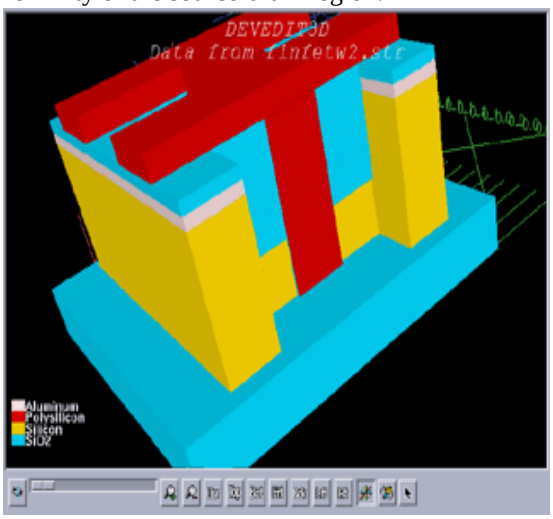


Fig. 8. Structure of a 2-parallel channel device. Gate length 50-nm.

This can be achieved very simply using the "mirror" feature in ***DevEdit3D***. The resulting I-V curve shown in Fig.9.

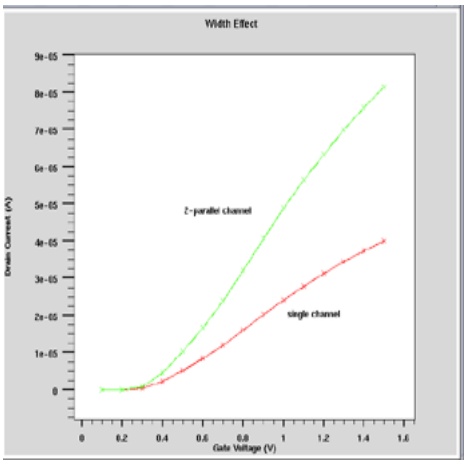
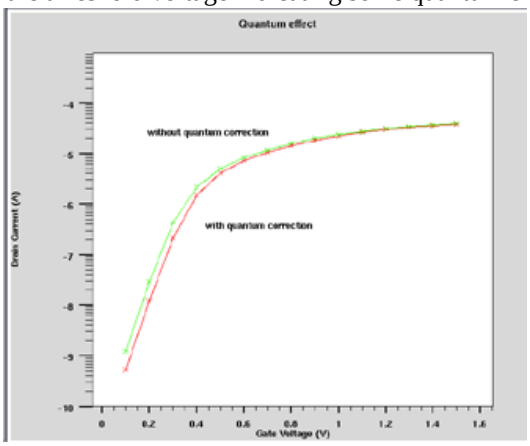


Fig.9. Drain Current Comparison between Single and 2-Parallel Channel Device, Gate Length 50-Nm.

Finally we simulated using our quantum module named *Quantum3D*. The result is plotted in Fig. 10. One can see a shift in the threshold voltage indicating some quantum effect.



Fig,10. Quantum effect in a 50-nm with a width of 50nm.

Sub 50-nm FinFETs were successfully simulated using 3-D SILVACO simulation tools. It is very easy to study the impact of the geometry and doping of this 3-D device using *Device3D*. Indeed more and more people take a look at this novel structure since it is an attractive successor to the single-gate MOSFET. In scaled devices, due to high electric field at the surface and high substrate doping, the quantization of inversion –layer electron energy modulates V_T. A DG device like FinFET offers unique opportunities for microprocessor design. Compared to a planar process in the same technology node, FinFET have reduced channel and gate leakage currents. This can lead to considerable power reduction when converting a planar design to FinFET technology. Utilizing FinFET would lead to reduction in total power by a factor of two, without compromising performance. Another possibility to save power occurs when both gates can be controlled separately. The second gate can be used to control the threshold voltage of the device, thereby allowing fast switching on one side and reduced leakage currents when circuits are idle.

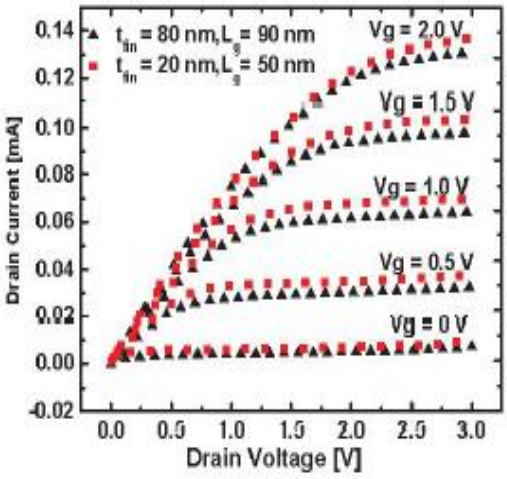


Fig.11. Drain Characteristics for Gate Length 50-Nm & 90-Nm.

Finally, separate access to both gates could also be used to design simplified logic gates. This would also reduce power, and save chip area, leading to smaller, more cost-efficient designs. However chip designs using FinFET must cope with quantization of device width, since every single transistor consists of an integral number of fins, each fin having the same height.

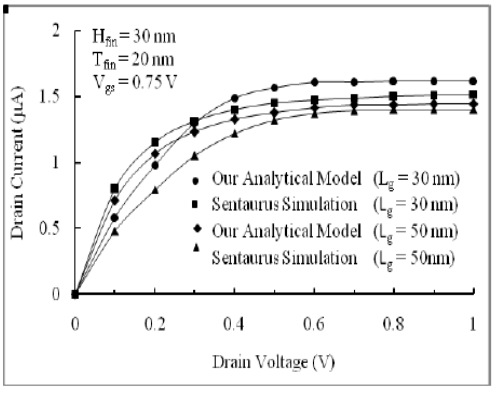


Fig. 12. Drain Characteristics for Finfet with Gate Length 30-Nm &50-Nm.

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Comparison of our analytical quantum mechanical model with Sentaurus simulation results for I_d-V_d characteristics for for gate lengths of 30 nm and 50 nm.

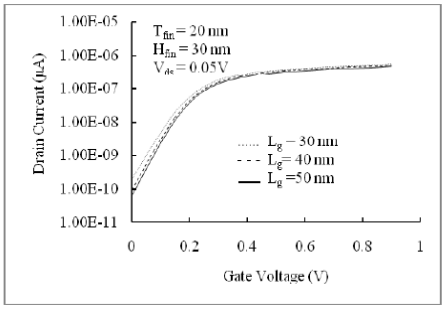

Fig .13. Variation of drain current with applied gate voltage for varying channel length of 30 nm, 40 nm and 50 nm using Sentaurus.

Table.I : Cost of SOI-based FinFET vs. junction-isolated bulk FinFET.

SOI-based FinFET				**Junction-isolated bulk FinFET**			
	L.S	P	C	L. S	P	C	C.D.
Substrate			500			120	-380
FEOL Process	7	56	561	9	91	805	244
Net cost difference							-136

L.S.-Litho steps; P- process; C-Cost ($);C.D-Cost Difference;

FinFET technology is economic, and the process involved made it is not costlier than conventional MOSFET fabrication.

VI. CONCLUSION

Simulations show that the FinFET structure should be scalable down to 10 nm technology. Formation of ultra thin fin (0.7 L_g, for a lightly doped body) is difficult for subduing short channel effects. This structure is fabricated by forming the S\D before the gate; This technique may be needed for future high-k dielectric and metal-gate technologies that cannot bear the high temperatures required for S\D formation. Further performance improvement is possible by using only ultra-thin gate dielectric and thinner spacers. Despite of its double gate structure, the FinFET is similar to the conventional MOSFET with regard to layout and fabrication. This is an attractive successor to the single gate MOSFET by advantages of its superior electrostatic properties and comparative ease of manufacturability. Research groups and also Industry running companies such as Intel, IBM and AMD have shown interests in developing similar devices, as well as mechanisms to migrate mask layouts from Bulk-MOSFET to FinFET. Some more issues such as gate work function engineering, high quality ultra thin fin lithography and source\drain resistance need to be resolved and a high-k yield process flow needs to be established by process researchers before FinFET can be used in commercial integrated circuits. Device researchers need to understand and model quantum effects, and circuit design researchers need to exploit the packing density afforded by the quasi-planar device to design efficient architectures.

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