

Relation between substrate surface morphology and microcrystalline silicon solar cell performance

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Abstract

In the present paper, the structural and electrical performances of microcrystalline silicon ($\mu\text{c-Si:H}$) single junction solar cells co-deposited on a series of substrates having different surface morphologies varying from V-shaped to U-shaped valleys, are analyzed. Transmission electron microscopy (TEM) is used to quantify the density of cracks within the cells deposited on the various substrates. Standard 1 sun, variable illumination measurements (VIM) and Dark $J(V)$ measurements are performed to evaluate the electrical performances of the devices. A marked increase of the reverse saturation current density (J_0) is observed for increasing crack densities. By introducing a novel equivalent circuit taking into account such cracks as non-linear shunts, the authors are able to relate the magnitude of the decrease of V_{oc} and FF to the increasing density of cracks.

Keywords: Silicon; Solar cells; Photovoltaics; TEM/STEM; Microcrystallinity; Porosity

1. Introduction

Thin film microcrystalline silicon ($\mu\text{c-Si:H}$) is a promising material for large-area thin film solar cells. Single junction $\mu\text{c-Si:H}$ cells already reached efficiency in the order of 10% [1–3]. Moreover, it can be combined with amorphous silicon to form tandem (micromorph) cells that reach initial efficiencies up to 13–14.5% [4,5]. It is already well known that the substrate morphology strongly influences the growth and performances of $\mu\text{c-Si:H}$ solar cells: a rougher substrate generally allows for enhanced light scattering within the device and thus, for a gain in photocurrent; however, open-circuit voltage (V_{oc}) and fill factor (FF) are usually both reduced [6,7]. The microscopic origin for this effect has so far not been fully clarified. This effect is

particularly pronounced when using glass substrates with a ZnO layer deposited by low-pressure chemical vapor deposition (LP-CVD). Such substrates have deep valleys with sharp angles (pinches). However, when LP-CVD ZnO substrates are subject to a plasma treatment in order to obtain a surface morphology without pinches, the values of V_{oc} and FF can again be markedly increased [8]. In this study, we look at a series of cells co-deposited on LP-CVD ZnO substrates treated during varying times, transforming the substrate's morphology from V-shape (initial) to U-shape (long treatment time). TEM observations indicate that the cells deposited on U-shape substrates have less cracks than on V-shape substrates. A good correlation can be established between the presence of cracks and poor solar cell performances (low V_{oc} and FF). Finally, by introducing a new equivalent electrical circuit, where an additional parallel diode renders the effect of cracks, we are able to take into account properly the effect of cracks on the $J(V)$ characteristics of $\mu\text{c-Si:H}$ single junction solar cells.

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2. Experimental procedures

The substrates were prepared by depositing a 5 μm thick LP-CVD-ZnO layer, from a vapor-gas mixture of water, diethyl-zinc and diborane, on AF45 glass substrates from Schott. The surface morphology was subsequently modified by applying a plasma treatment on the ZnO layers (see Fig. 1) [8]. This treatment allows for morphology modifications ranging from V-shape (initial) morphology to U-shape one (with treatment). For longer treatment time, LP-CVD-ZnO becomes almost flat with decreasing light scattering capabilities. p-i-n $\mu\text{c-Si:H}$ single junction solar cells were co-deposited on these substrates in a small area plasma-enhanced chemical vapor deposition (PECVD) reactor, working at very-high excitation frequency (VHF) [8]. The thickness of the $\mu\text{c-Si:H}$ intrinsic layer is approximately 1.8 μm .

Standard $J(V)$ curves are measured under WACOM solar simulator, and variable illumination measurements (VIM) are performed on the same set-up by using metallic mesh grey filters. Dark $J(V)$ curves are measured with voltages comprised between -1 and 1 V at 25°C . Finally, the cells are prepared for TEM cross-sectional examination by using the tripod method [9]. TEM bright-field medium-resolution, micrographs are obtained with a Philips CM200 microscope operated at 200 kV. The estimation of number of cracks has been done by averaging over a cross section length of 20 μm , which is considered to be representative of the whole sample.

3. Model and simulation procedure

In 1998, Merten et al. [10] proposed an equivalent electrical circuit for amorphous silicon solar cells modified to take into account the recombination current within the i-layer. The circuit is composed as usual of a diode, a photo-generation source, a series resistance and a shunt resistance. To this a recombination current sink is added. The recombination current represents losses due to defects (recombination centers) in the bulk material, whereas, the series resistance accounts for contact resistance and the shunt resistance describe linear leakage current, such as cell patterning shunts at the edges or pinholes within the i-layer. The $J(V)$ curve of the a-Si:H pin solar cell can then be expressed as the sum of the different contributions (principle of superposition). At first sight, cracks can be thought of being some kind of linear shunts between the front and back contact. By using the equivalent circuit of Merten et al., one can quantify the loss in FF due to the respective increased recombination losses (decrease in V_{coll}) and decreasing shunt resistance R_{sh} ; this approach was studied in [11]. However, when applying this approach to analyze the data of our VIM-measurements, the loss in FF observed for cells with a high crack density is much greater than the loss that would be predicted due to the measured decrease of R_{sh} and of V_{coll} .

In our new equivalent circuit for $\mu\text{c-Si:H}$ solar cells (see right part of Fig. 2), the effect of cracks in the material is taken into account by adding a second parallel diode to

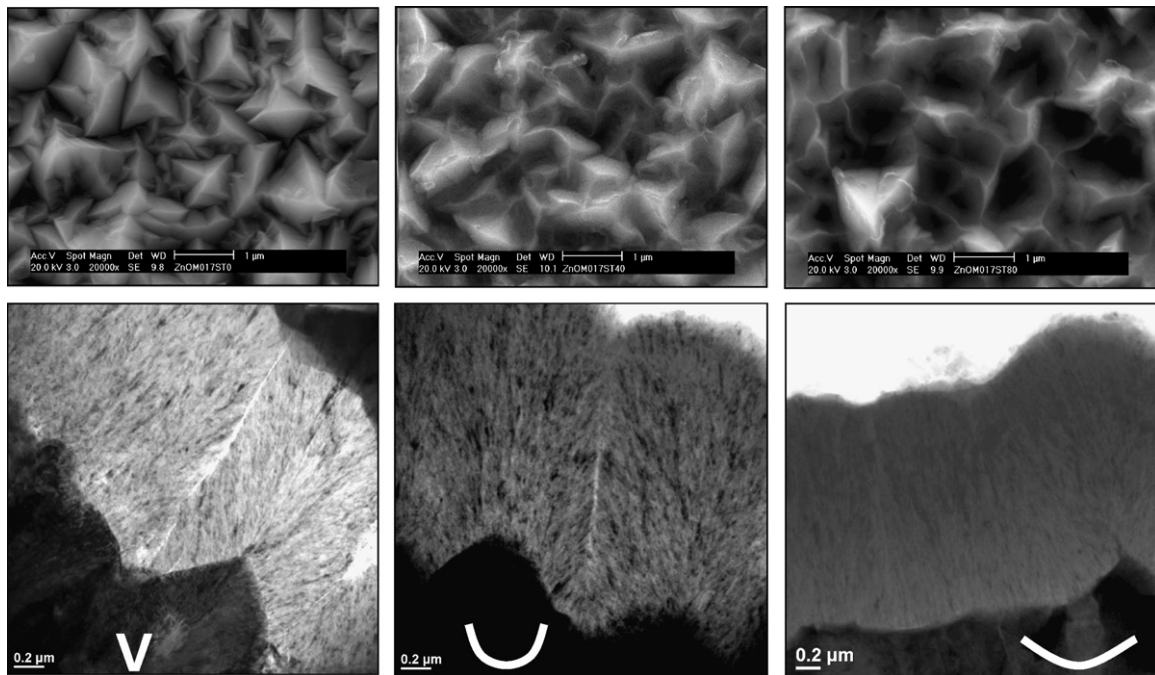


Fig. 1. Up: SEM micrographs of ZnO surface. Down: bright field TEM cross-section micrographs of $\mu\text{c-Si:H}$ pin on substrates treated with increasing plasma treatment time (left 0 min/middle 40 min/right 80 min). For 40 min of treatment, the cracks do not cross completely through the p-i-n device (compare with sample $t = 0$ min), but only begin after the first third of the i-layer.

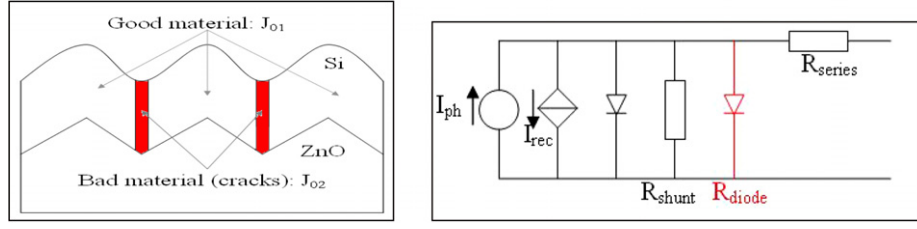


Fig. 2. Left: sketch of silicon growth on rough ZnO: cracks are located above the valleys between the substrate's pyramids. Right: corresponding equivalent electrical circuit for $\mu\text{c-Si:H}$ solar cells. R_{diode} is a non-linear resistance related to cracks and form by diode₂.

the equivalent electrical circuit (see left part of Fig. 2). The $J(V)$ curve of the $\mu\text{c-Si:H}$ pin solar cell is then expressed by:

$$J_{\text{tot}}(V) = J_{\text{diode}_1} + J_{\text{diode}_2} + J_{\text{rec}} + J_{\text{sh}} - J_{\text{L}}$$

$$= J_{01} \left(\exp \left(\frac{qV'}{n_1 kT} \right) - 1 \right) + J_{02} \left(\exp \left(\frac{qV'}{n_2 kT} \right) - 1 \right)$$

$$+ J_{\text{L}} \cdot \frac{\varphi(V') \cdot d_i^2}{(\mu\tau)_{\text{eff}} \cdot (V_{\text{bi}} - V')} - J_{\text{L}}, \quad (1)$$

$$V' = V - J_{\text{tot}} \cdot R_s, \quad (2)$$

with V the voltage, n_1 and n_2 the ideality factors, V_{bi} the built-in voltage, $(\mu\tau)_{\text{eff}}$ the effective mobility-lifetime product, d_i the thickness of intrinsic layer, $\varphi(V)$ the electric field deformation factor, considered constant, R_p the parallel resistance, R_s the series resistance and J_{L} the photogenerated current density.

J_{diode_1} corresponds to the dark current of the reference cell and all values are fixed with a good solar cell (without cracks). J_{diode_2} corresponds to the dark current arising from cracks in the solar cell (bad material). The value of n_2 is fixed equal to 2 in order to represent a recombination-limited device. J_{02} is, thus, the model parameter, which will depend on the density of cracks in the i-layer. J_{rec} can be rewritten as

$$J_{\text{rec}} = J_{\text{L}} \cdot \frac{\varphi(V') \cdot d_i^2}{(\mu\tau)_{\text{eff}} \cdot (V_{\text{bi}} - V')} = J_{\text{L}} \cdot \frac{V_{\text{bi}}^2}{V_{\text{coll}} \cdot (V_{\text{bi}} - V')}, \quad (3)$$

with $V_{\text{coll}} = \frac{(\mu\tau)_{\text{eff}} \cdot V_{\text{bi}}^2}{\varphi(V') \cdot d_i^2}$ the collection voltage (obtained by VIM measurements).

A simulation program (developed with LabView) allows fitting dark and illuminated $J(V)$ curves based on Eq. (1). The parameters that can be fitted by simulation are: R_p , R_s , n_1 , n_2 , J_{01} , J_{02} , J_{sc} and V_{coll} . The procedure employed to obtain the characteristics of the shunt diode was as follows: first, the parameters (R_p , n_1 , J_{01}) of an 'ideal' $\mu\text{c-Si:H}$ diode were obtained by measuring and fitting the dark $J(V)$ curve of a good reference cell (deposited on the almost flat, treated ZnO), without any shunt diode. Then, the V_{coll} value of the 'ideal' cell is obtained from VIM measurements by taking the slope between (0;0) and $(1/J_{\text{sc}}; R_{\text{sc}})$ at 1 sun. The values of these parameters were then fixed in the simulation software. Finally, the standard $J(V)$ curves at 1 sun for all other cells were fitted with n_2 fixed at 2 (value for recombination-limited diode) and the other

parameters (R_s , J_{02} , J_{sc}) were obtained with the 2 diode simulation (see Fig. 2).

4. Results

In the previous study of Bailat et al. [8], a relationship between the electrical parameters (V_{oc} and FF) and ZnO surface time treatment was established. The V_{oc} , FF and efficiency values all increased as a function of treatment time. Here, the magnitude of the device's electrical performances amelioration is explained by considering cracks as diode-like shunts in the equivalent electrical circuit of the solar cells. As seen in Fig. 3, the 1 sun $J(V)$ curves are very well fitted by the simulation program by using the fixed parameters obtained with the reference cell (diode1) and by adjusting only the value of J_{02} for the second diode.

Fig. 4 shows how the increasing crack density within the i-layer leads to an increasing value of J_{02} . The 2 points close to the origin are measured for very good solar cells: cracks have almost disappeared from the i-layer. The largest value of J_{02} is measured in the device on untreated ZnO, in which cracks cross through the whole i-layer. Finally, the intermediate point is observed for a device in which cracks extend only up to one third of the i-layer thickness. If we consider that $J_{02} = n \times I_{\text{crack}}$ with n the density of cracks per cm^2 and I_{crack} the inverse current of an individual crack, then from the slope of the linear fit of the data in

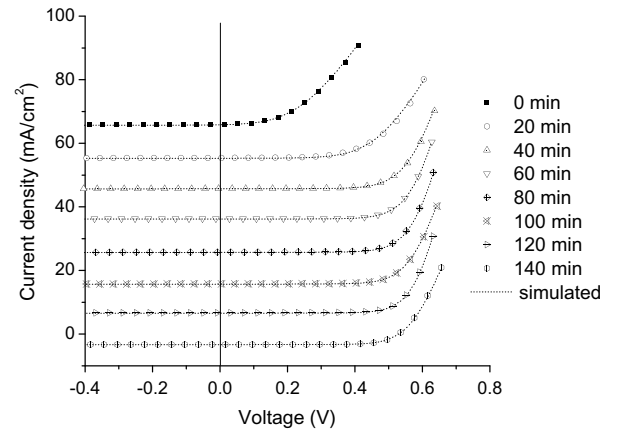


Fig. 3. Experimental illuminated $J(V)$ curves (1 sun) for each treatment (each one is shifted by 10 mA). Excellent fits are obtained with the 2-diode model (black dots) varying only J_{02} .

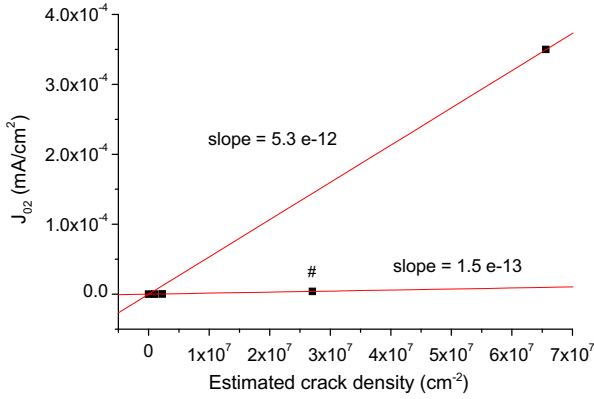


Fig. 4. Relationship between the value of J_{02} and the crack surface density, estimated by TEM micrographs, in co-deposited $\mu\text{c-Si:H}$ cells on varying substrates. Low J_{02} and low crack density is observed in ‘good’ solar cells. The point marked with the symbol # corresponds to a device where the cracks do not cross the whole pin structure, whereas the highest J_{02} value is observed for the device deposited on untreated ZnO and exhibits cracks running all the way through the device.

Fig. 4, we obtain that the inverse current for each crack is between 10^{-13} and 5×10^{-12} mA, depending on the length of the cracks relative to the i-layer thickness. These values are consistent with ZnO grain size in the range of $1 \mu\text{m}$.

Fig. 5 gives the variation of electrical parameters in function of the estimated density of cracks. High values of V_{oc} and FF are related to a low density of cracks in the i-layer of the solar cells.

5. Discussion

The present paper illustrates the negative effect of the occurrence of cracks in $\mu\text{c-Si:H}$ pin single junction solar cells on the electrical performance of the devices. In particular, V_{oc} and FF values decrease with increasing crack densities. The effect of the substrate’s surface geometry on the occurrence of cracks is related to the occurrence of pinches on the substrate; these can be avoided by the modification of the substrate’s geometry from V-shape to U-shape. Here, the modelization of the cracks on the solar cell $J(V)$ curves by a resistor-like element in the equivalent cir-

cuit does not allow one to fit the observed decrease in V_{oc} and FF. One needs to add a second parallel diode to the usual equivalent electrical circuit. In this work, the unshunted part of the device is considered as a ‘good’ diode (diode 1: $n_1 = 1.45$, $J_{01} = 1.1 \times 10^{-8} \text{ mA/cm}^2$) whereas the cracks are modeled by a ‘bad’ diode (diode 2: $n_2 = 2$, $J_{02} = n \times J_{\text{crack}}$). With this novel equivalent circuit, we are able to fit very well the experimental ‘1 sun’ and dark $J(V)$ curves. Furthermore, the relationship between J_{02} and the estimated density of cracks seems to depend on whether or not the cracks cross through the whole device thickness. Cracks that cross all layers (p-i-n) seem to be more destructive ($I_{\text{crack}} = 5 \times 10^{-12} \text{ mA}$) than cracks that end within the i-layer ($I_{\text{crack}} = 10^{-13} \text{ mA}$). Therefore, further work has to be done in order to identify more precisely the nature and the type of cracks existing in $\mu\text{c-Si:H}$ solar cells deposited on rough substrates. Also, the role of the opening angle of the substrate structure [6] and of the radius of curvature of the pinches [2,8] on the creation or suppression of cracks have to be understood more in detail.

6. Conclusions

In this paper, the origin and the effect of cracks in thin film microcrystalline solar cells is studied. With TEM observations, we show that a V-shaped substrate morphology results in a large density of cracks crossing the whole pin solar cell, whereas U-shaped substrates lead to the growth of dense $\mu\text{c-Si:H}$. Characterization of the electrical performance of these devices by VIM and dark $J(V)$ measurements indicates that cracks do not act simply as resistive-like shunts in $\mu\text{c-Si:H}$ devices. We have to modelize the cracks as diode-like shunts in the equivalent circuit of the device in order to be able to fit our experimental data. It seems that FF and V_{oc} losses induced by cracks depend on the length and origin of the latter. For our ZnO grain size, when cracks cross the whole pin device, their individual reverse saturation current is about $5 \times 10^{-12} \text{ mA}$ whereas if the crack is not completely crossing the device, it is about 10^{-13} mA . Even if this observation needs further confirmation, our study demonstrates that growth of

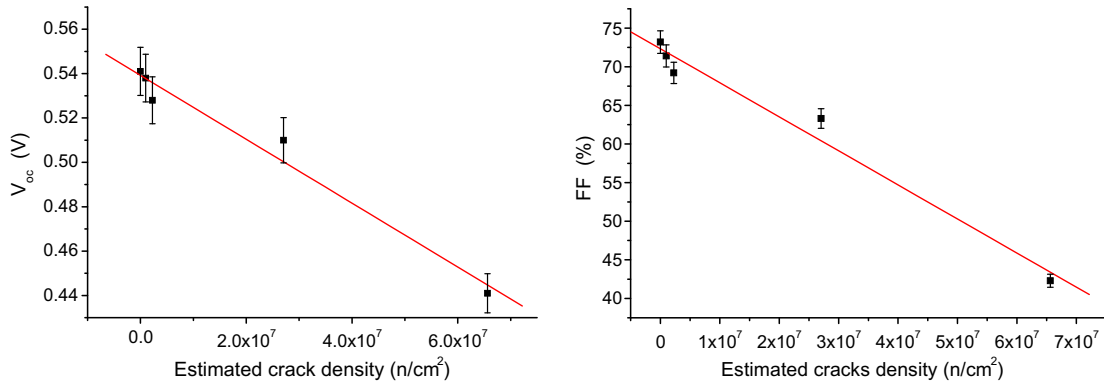


Fig. 5. Improvement of V_{oc} and FF with a decrease in the crack density; the latter having been evaluated from TEM micrographs.

dense, crack-less $\mu\text{-Si:H}$ devices permits an improvement of the resulting solar cell electrical characteristics.

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