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Relationship of drain induced barrier lowering and top/bottom gate oxide thickness in asymmetric junctionless double gate MOSFET

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ABSTRACT

The relationship of drain induced barrier lowering (DIBL) phenomenon and channel length, silicon thickness, and thicknesses of top and bottom gate oxide films is derived for asymmetric junctionless double gate (JLDG) MOSFETs. The characteristics between the drain current and the gate voltage is derived by using the potential distribution model to propose in this paper. In this case, the threshold voltage is defined as the corresponding gate voltage when the drain current is $(W/L)\times10^{-7}$A, and the DIBL representing the change in the threshold voltage with respect to the drain voltage is obtained. As a result, we observe the DIBL is proportional to the negative third power of the channel length and the second power of the silicon thickness and linearly proportional to the geometric mean of the top and bottom gate oxide thicknesses, and derive a relation such as DIBL=$25.15\eta L_g^{-3}t_{si}^2\sqrt{t_{ox1}\cdot t_{ox2}}$, where η is a static feedback coefficients between 0 and 1. The η is found to be between 0.5 and 1.0 in this model. The DIBL model of this paper has been observed to be in good agreement with the result of other paper, so it can be used in circuit simulation such as SPICE.

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1. INTRODUCTION

In order to reduce short channel effects (SCEs) known as secondary effects, the structures of three-dimensional transistor have been developed and used. The FinFET is the most used commercially available three-dimensional MOSFET [1-4]. The existing three-dimensional structure mainly used an inversion-type MOSFET using a junction-based structure with different doping type and concentration between source/drain and channel, but recently reached the limit of the technology of forming a junction with decreasing channel length to nano unit [5-8]. The transistor developed to solve this problem is a junctionless MOSFET [9, 10]. This structure is an accumulation-type MOSFET that overcomes process limitations by doping the source/drain and channel in the same type and concentration [11-13]. In the case of the symmetrical junctionless MOSFETs, many studies have been conducted [14-16]. However, many studies on the asymmetric junctionless MOSFETs capable of fabricating different top and bottom oxide thicknesses and applying different top and bottom gate voltages to each other have not been conducted [17-18]. In this paper, we propose an analytical potential model to analyze the drain induced barrier lowering (DIBL) of

the secondary effects in the asymmetric junctionless double gate (JLDG) MOSFET. The DIBL is affected by channel length, silicon thickness and oxide structure (thickness and dielectric constant). In general, the DIBL is proportional to the negative third power in the channel length and the second power in the silicon thickness, and is also linearly proportional to the oxide film thickness [19, 20]. The relationship among the top and bottom oxide film thicknesses and the DIBL should be re-established since the top and bottom oxide film thicknesses may be fabricated differently in the case of the asymmetric structure. Ding *et al*. proposed the potential model of the asymmetric junction-based double gate MOSFET and analyzed the short channel effects [21]. Raksharam et al. analyzed the short channel effect using the potential model of the symmetrical JLDG MOSFET [22]. However, the research on the asymmetric JLDG MOSFETs is very insufficient. In this paper, we modified the potential model of Ding et al. to be applicable to the junctionless MOSFET, and derived the potential model of the asymmetric JLDG MOSFET. We will present an analytical model of DIBL for channel dimension and top and bottom oxide thickness to apply in SPICE.

2. THRESHOLD VOLTAGE AND DIBL OF ASYMMETRIC JLDG MOSFET

Figure 1 shows a schematic diagram of the asymmetric JLDG MOSFET used in this paper. The source and drain were heavily doped with n^+ and the channel was also doped with N_d=3.5×10^{19}/cm^3. The top and bottom gate voltages are V_{gt} and V_{gb} respectively, L_g is gate length, t_{si} is silicon thickness, and t_{ox1} and t_{ox2} are the oxide thicknesses of the top and bottom, respectively. The V_s and V_d are the voltages of source and drain, respectively. The potential distribution modified using the Poisson equation and the boundary condition of Ding's model can be expressed as follows [21].

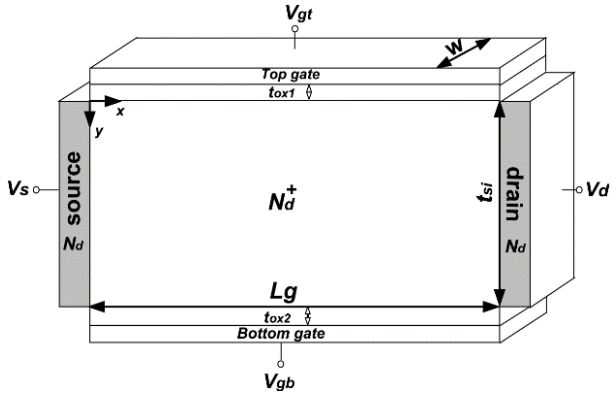

Figure 1. Schematic cross-sectional diagram of the asymmetric JLDG MOSFET

$$\phi(x,y) = V_s + \frac{V_d x}{L_g} + \sum_{n=1}^{\infty} A_n(y)\sin\frac{n\pi x}{L_g}, \tag{1}$$

$$A_n(y) = C_n e^{k_n y} + D_n e^{-k_n y} - f_n/k_n$$

$$f_n = \begin{cases} -\dfrac{4qN_d}{n\pi\varepsilon_{si}}, & n = 1,3,5,\cdots \\ 0, & n = 2,4,6,\cdots \end{cases}$$

$$C_n = \frac{C_{ox1}\left[\begin{array}{l}(\varepsilon_{si}k_n - C_{ox2})\left(f_n - G_n k_n^2\right) + \\ r(C_{ox1} + \varepsilon_{si}k_n)(f_n - H_n k_n^2)e^{k_n t_{si}}\end{array}\right]}{k_n^2\left[\begin{array}{l}C_{ox1}\varepsilon_{si}k_n(1+r)\left(1+e^{2k_n t_{si}}\right) - \\ (C_{ox1}C_{ox2} + \varepsilon_{si}^2 k_n^2)(1-e^{2k_n t_{si}})\end{array}\right]}, \quad D_n = \frac{C_{ox1}e^{k_n t_{si}}\left[\begin{array}{l}(\varepsilon_{si}k_n + C_{ox2})\left(f_n - G_n k_n^2\right)e^{k_n t_{si}} - \\ r(C_{ox1} - \varepsilon_{si}k_n)(f_n - H_n k_n^2)\end{array}\right]}{k_n^2\left[\begin{array}{l}C_{ox1}\varepsilon_{si}k_n(1+r)\left(1+e^{2k_n t_{si}}\right) - \\ (C_{ox1}C_{ox2} + \varepsilon_{si}^2 k_n^2)(1-e^{2k_n t_{si}})\end{array}\right]}$$

$$G_n = \begin{cases} \left(\frac{2}{n\pi}\right)\left[2\left(V_s - V_{gt} + V_{fbt}\right) + V_d\right], & n = 1,3,5,\cdots \\ 0, & n = 2,4,6,\cdots \end{cases}$$

$$H_n = \begin{cases} \left(\frac{2}{n\pi}\right)\left[2\left(V_s - V_{gb} + V_{fbb}\right) + V_d\right], & n = 1,3,5,\cdots \\ 0, & n = 2,4,6,\cdots \end{cases}, \quad r = C_{ox2}/C_{ox1}, \quad k_n = n\pi/L_g .$$

where ε_{si} is the dielectric constant of silicon, V_{fbt} is the flat-band voltage of the top gate, and V_{fbb} is the flat-band voltage of the bottom gate. $C_{ox1}(=\varepsilon_{tox1}/t_{ox1})$ and $C_{ox2}(=\varepsilon_{tox2}/t_{ox2})$ are the gate oxide capacitances of the top and bottom sides. Since the silicon dioxide is used as top and bottom gate oxide materials, $\varepsilon_{tox1}=\varepsilon_{tox2}=3.9$.

In the case of the junctionless structure, most of the moving electric charges in the channel are known to move through the central axis ($y=t_{si}/2$), and the relationship between the drain current and the gate voltage in the subthreshold region can be derived from the diffusion-drift current equation of (2).

$$I_d = \frac{qn_i\mu_n WkT\left\{1-\exp\left(\frac{-qV_d}{kT}\right)\right\}}{\int_0^{L_g}\frac{1}{\int_0^{t_{si}}\exp\left(\frac{q\phi(x,y)}{kT}\right)dy}dx} \tag{2}$$

where k is Boltzmann's constant, T is absolute temperature, n_i is the electron concentration of the intrinsic semiconductor, μ_n is the electron mobility, and W is a channel width.

The result of drain current-gate voltage obtained using (2) is compared with the results of 2D simulation and Xie's model [23] in Figure 2. As a result, it could be observed that they coincide with each other in the region below the threshold voltage. Therefore, the potential distribution of (1) presented in this paper is valid, and the validity of the drain current-gate voltage relationship obtained using this potential distribution is also proved. In this paper, the threshold voltage V_{th} is defined using the definition of threshold voltage used in TCAD [24-25]. In other words, the threshold voltage is defined as the gate voltage at when the drain current is equal to (3).

$$I_d = \left(\frac{W}{L_g}\right)\times 10^{-7}\,A \tag{3}$$

Then, the DIBL is obtained by using (4).

$$DIBL = \frac{V_{th}(V_d = 0.05\ V) - V_{th}(V_d = 0.55\ V)}{0.5\ V} \tag{4}$$

in this paper, the DIBLs obtained using (4) will be expressed according to channel length, silicon thickness, and top and bottom oxide thickness.

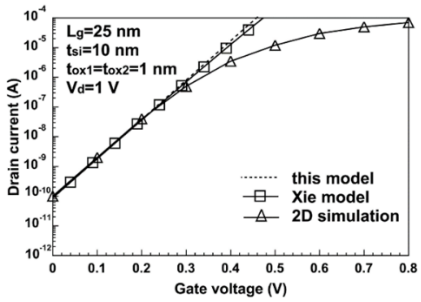

Figure. 2. Comparisons of the drain current-gate voltage characteristics for this model with results of 2D simulation and Xie's model

3. EXTRACTION OF DIBL MODEL FOR ASYMMETRIC JLDG MOSFET

First, the asymmetric type can be fabricated differently in the top and bottom oxide film thickness, unlike the symmetric type. Therefore, DIBL's contour curves for the variations of the top and bottom gate oxide thickness are shown in Figure 3. It was found that the top and bottom gate oxides were in inverse proportion to each other in order to maintain a constant DIBL as shown in Figure 3, and the DIBL increased as the oxide thickness increased. From the characteristics of the curve, it can be seen that the DIBL changes according to the product of the top and bottom oxide thicknesses, which in turn changes according to the geometric mean of the top and bottom gate oxide thicknesses. In other words, the relationship of (5) will be established.

$$DIBL \propto \sqrt{t_{ox1} \cdot t_{ox2}} \tag{5}$$

To demonstrate the validity of (5), the variation of DIBL with respect to the geometric mean of the top and bottom gate oxide thicknesses is shown with the silicon thickness as a parameter in Figure 4. As predicted in Figure 3, we can observe that the DIBL is proportional to $\sqrt{t_{ox1} \cdot t_{ox2}}$. Therefore (5) would be valid. The observation for the silicon thickness used as a parameter shows that the DIBL increases and the increasing rate (the linear slope in Figure 4) also increases as the silicon thickness increases. This means that the DIBL does not increase linearly when silicon thickness increases linearly.

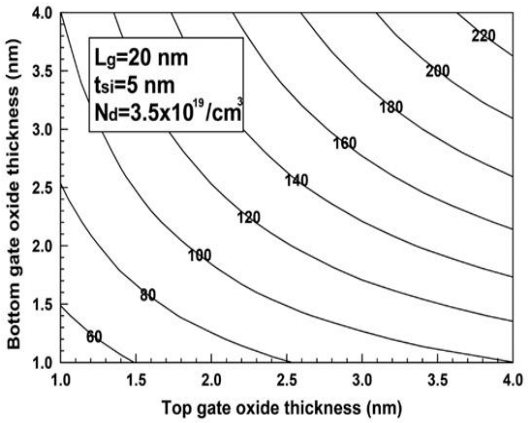

Figure 3. Contours of DIBLs for the top and bottom gate oxide thicknesses in the case of channel length of 20nm and silicon thickness of 5nm

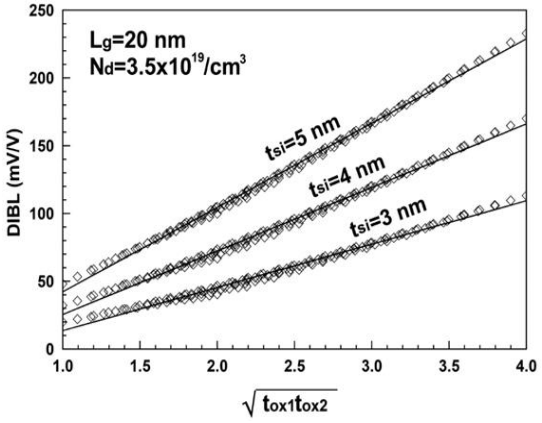

Figure 4. Relation of DIBLs for the geometric mean of the top and bottom gate oxide thicknesses with the silicon thickness as a parameter

The variation of the DIBL with silicon thickness is shown in Figure 5 in order to find out the relationship of DIBL and silicon thickness. In general, in a double-gate MOSFETs, the DIBL is known to be proportional to the square of silicon thickness [20]. As can be seen in Figure 5, the DIBL is proportional to the square of silicon thickness for not only the symmetrical JLDG MOSFETs with the same top and bottom gate oxide thickness, but also the asymmetric JLDG MOSFETs with the top gate oxide thickness of 2nm and the bottom gate oxide thickness of 1nm. Note that in the case of the asymmetric JLDG MOSFET, the same results are obtained as shown in Figure 3 and Figure 4 even if the top and bottom gate oxide thicknesses are interchanged.

As can be seen in Figure 5, the DIBL changes with channel length. Therefore, Figure 6 shows the DIBL of the JLDG MOSFET with the symmetric and asymmetric oxide thickness when the silicon thickness is 5nm in order to observe the variation of DIBL with respect to channel length. As with the conventional CMOSFET [17], we can see that the JLDG MOSFET is proportional to the negative third power of the channel length. In addition, it can be seen that not only the symmetric type but also the asymmetric JLDG MOSFETs having different top and bottom gate oxide thicknesses are equally proportional to the negative third power of the channel length. In this paper, the DIBL is observed for the JLDG MOSFET with channel length of more than 10nm. For the JLDG MOSFETs with channel lengths below 10nm, additional secondary effects, such as tunneling, have to be analyzed quantum mechanically [26, 27]. Taken together the above results, the DIBL can be expressed as the following (6).

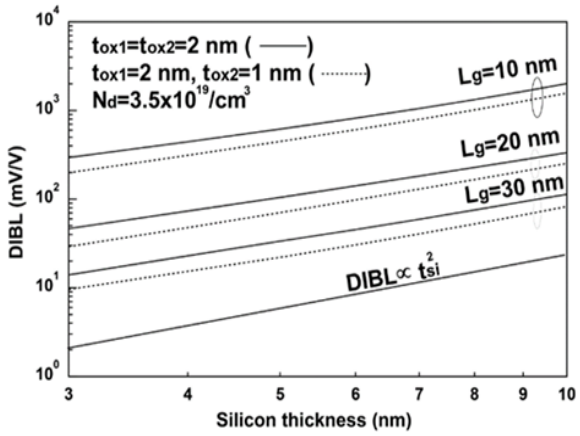

Figure 5. DIBLs for silicon thicknesses with channel length and oxide thickness as parameters

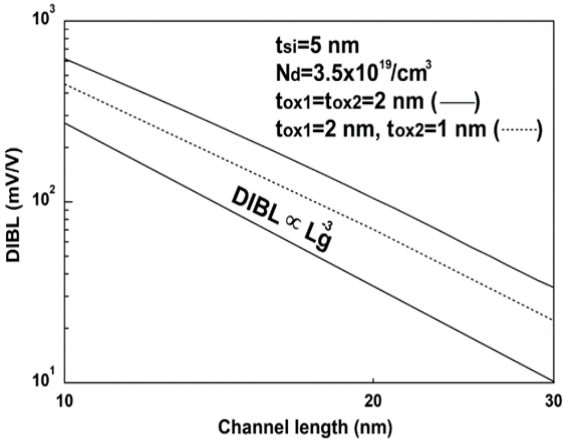

Figure 6. DIBLs for channel length in the case of silicon thickness of 5nm with oxide thickness as a parameter

$$DIBL = A\eta L_g^{-3} t_{si}^2 \sqrt{t_{ox1} \cdot t_{ox2}} \tag{6}$$

where A is the proportional constant and η is the SPICE parameter known as the static feedback coefficient. To obtain A, the value of $A\eta$ is firstly obtained from the following (7) by using the channel size and the oxide film thickness used to calculate the DIBL.

$$A\eta = DIBL / L_g^{-3} t_{si}^2 \sqrt{t_{ox1} \cdot t_{ox2}} \tag{7}$$

The maximum value obtained using (7) is 25.15, and A is set to 25.15 to obtain a reasonable range of the static feedback coefficients. The static feedback coefficients thus obtained are shown in Figure 7. Figure 7(a), (b), and (c) show a case in which the top and bottom gate oxide layers have the same symmetrical structure. However, the same type of relationship graphs can be derived in the case of the asymmetric JLDG MOSFETs if the top and bottom gate oxide thicknesses are adjusted to have the same geometric mean for the top and bottom gate oxide thicknesses as described above. The reason for this is that they show the same DIBL results. As can be seen in Figure 7, it can be observed that as the geometric mean of the top and bottom oxide thicknesses increases, the range of the static feedback coefficient increases and the change according to the silicon thickness also increases. In general, the SPICE parameter, static feedback coefficient, has a value between 0 and 1, so the DIBL model is reasonable for the asymmetric JLDG MOSFET presented in this paper. In other words, the DIBL model of the asymmetric JLDG MOSFET can be expressed by the following (8) depending on the channel length, silicon thickness, and oxide film thickness.

$$DIBL = 25.15\eta L_g^{-3} t_{si}^2 \sqrt{t_{ox1} \cdot t_{ox2}} \tag{8}$$

It can be seen from Figure 7 that the static feedback coefficient is approximately $0.5 < \eta < 1.0$ in the channel dimension and oxide thickness range calculated in this paper. In order to verify the validity of (8), the DIBL values obtained from Raksharam's model [22] and the analytical DIBL model of (8) presented in this paper are compared in Figure 8. As can be seen in Figure 8, it can be observed that the DIBL obtained using Raksharam's model falls within the range when the static feedback coefficient is between 0.5 and 1.0 in (8). Therefore, the DIBL can be obtained according to the channel dimension and the top and bottom oxide thickness by adjusting the static feedback coefficient. As can be seen in Figure 8, the change of DIBL with respect to the change of the static feedback coefficient is small as the channel length increases, but the DIBL changes significantly with the change of the static feedback coefficient as the channel length decreases. Therefore, the shorter the channel length, the more care must be taken when determining the static feedback coefficient.

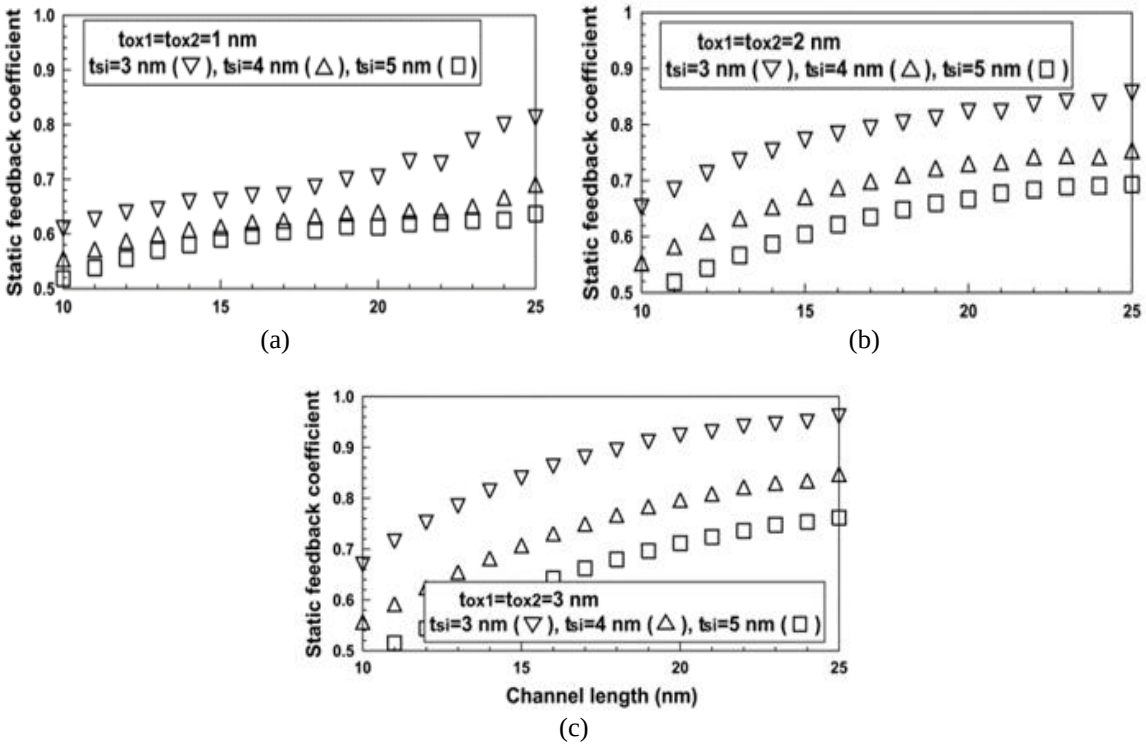

Figure 7. Static feedback coefficients for channel length with silicon thickness and oxide thickness as parameters in the case of (a) *tox1=tox2*=1nm, (b) *tox1=tox2*=2nm, and (c) *tox1=tox2*=3nm

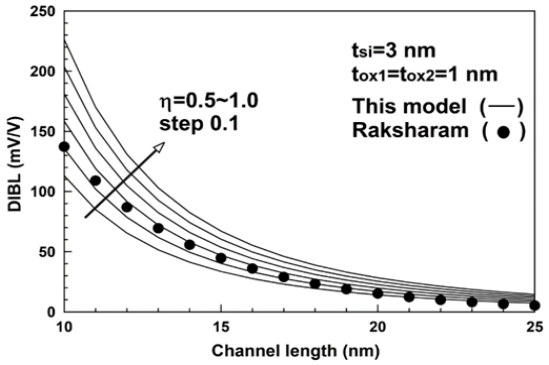

Figure 8. Comparisons of the DIBL model of (8) and Raksharam's model

4. CONCLUSION

In this paper, the relationship among the device dimension such as channel length, silicon thickness, and top and bottom oxide thickness and DIBL of the asymmetric JLDG MOSFET is derived. In general, for symmetrical double gate MOSFETs, DIBL is proportional to the negative third power of the channel length, the second power of the silicon thickness, and linearly to oxide thickness. In the case of asymmetry, however, the relationship that the DIBL is linearly proportional to the oxide layer must be corrected since the thicknesses of the oxide layers at the top and the bottom can be fabricated differently. As a result, it was found that the asymmetric JLDG MOSFET is proportional to the geometric mean of the gate oxide thickness at the top and bottom. The same relationship can be used for symmetrical JLDG MOSFETs with the same oxide thickness at the top and bottom. In addition, we can observe that the DIBL model presented in this paper is in good agreement with the model presented in other paper. The static feedback coefficient, which is a parameter used in the SPICE DIBL model of CMOSFET, is known to be about 0.7. In the DIBL model of the asymmetric JLDG MOSFET presented in this paper, the static feedback coefficient has a value between 0.5 and 1.0. It is believed that this model can be used sufficiently in circuit simulation programs such as SPICE. These results will serve as the basis for future fabrication of the asymmetric JLDG MOSFETs.

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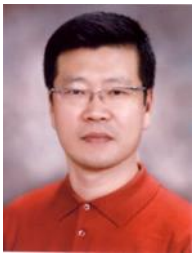
BIOGRAPHIES OF AUTHORS



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