Relaxing the maximum dc input amplitude vs. consumption trade-off in differential-input band-pass biquad filters

Julián Oreggioni, Pablo Castro Lisboa, and Fernando Silveira

Abstract

This paper shows that an important part of the power consumption of a biquad band-pass filter is associated with the feedback loop that fixes the high-pass frequency and blocks the dc input signals. The dc input amplitude that can be blocked is related to the maximum output current that one of the transconductors can provide, hence impacting on the required consumption through this effect. Then, a technique that efficiently blocks the dc input signal and fixes the high-pass frequency is introduced and analyzed in depth. Moreover, an architecture for ultra-low-power differential-input biquads is fully presented. The proposed architecture enables lowering the power consumption, or blocking higher levels of dc input without jeopardizing the power consumption. Results show that the proposed architecture, compared with a traditional one, presents a 30% reduction in power consumption and more than doubles the dc input that can be blocked.

Index Terms

Analog integrated circuits, ultra-low-power design, biquadratic filter, active filter, differential amplifiers

I. Introduction

Second-order filters, often referred as biquads, can be configured to be universal filters and they are suitable for cascade connection in order to achieve higher order filters [1]. Furthermore, biquads can provide differential input and band-pass filtering with amplification. These are key

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features in the input stage of diverse applications e.g. neural amplifiers, biopotential amplifiers or sensor interface circuits. The differential input is important in order to reject common mode interference, such as electromagnetic interference or undesired signals. Moreover, due to the low amplitude of the input signal, band-pass filtering is required (for noise reduction) as well as signal amplification.

In the area of biomedical or biological applications, several approaches have been reported in the last decade. They propose circuits that provide low-noise, ultra-low-power, band-pass filtering, differential input, amplification, high Common Mode Rejection Ratio (CMRR) and the capacity to reject large input dc values (e.g. dc offsets generated at the electrode-tissue interface). The approach proposed by Harrison et al. [2], based on capacitors for ac-coupling and MOS-bipolar high valued pseudo-resistors, is widely used [3], [4]. A disadvantage of the Harrison et al. approach is that the resistance of the pseudo-resistor is highly variable and the high-pass frequency is not well determined [5]. To overcome these drawbacks, other architectures have proposed to use differential-difference amplifiers (DDA) [5], [6] or chopper amplifiers [7], [8].

Continuous-time integrated Gm-C filters, have received considerable interest in various applications, such as hard-disc drives, video filtering, wireless communications, instrumentation systems and biomedical circuits [9], [10]. Gm-C filters are suitable for biomedical or biological applications because they present high input resistance, it is possible to integrate large time constants within a reasonable silicon area [11] and they have a simple and systematic design flow, but many of their other properties still need improving, such as operation at reduced power consumption [10].

Therefore, another possible approach to provide low-noise, ultra-low-power, band-pass filtering, differential input, amplification, high Common Mode Rejection Ratio (CMRR) and the capacity to reject large input dc values, is to use a traditional Gm-C biquad band-pass filter, for example the one shown in Fig. 1 [12], [13]. However, this solution requires an Operational Transconductance Amplifier (OTA) devoted to establish the high-pass characteristic and block the dc input (depicted by Gm3 in Fig. 1). This implies an overhead in terms of power consumption and silicon area. There are other Gm-C biquad architectures that achieve the band-pass characteristic without Gm3. However, these architectures, such as the one used in [14], do not have a differential input. These type of filters can be used in the middle of the processing chain, but they are not suitable for the input stage. This paper proposes to modify the Gm-C biquad

filter with differential input, using a technique that blocks the dc input and fixes the high-pass frequency without the aforementioned overhead.

This work presents three main contributions. Firstly, the trade-off between the biquad power consumption and its capacity of blocking large dc inputs is introduced. Secondly, this paper presents in a detailed manner, a technique for blocking the input dc component and fixing the high-pass frequency without jeopardizing the power consumption. Finally, this technique is applied to design biquad Gm-C band-pass filters, to lower the power consumption or to block higher levels of dc input without increasing the power consumption. The papers [6] and [15] address biomedical analog circuits which exploit the proposed technique, benefiting from what is being disclosed herein in detail for the first time.

The remainder of this paper is organized as follows: Section II introduces and describes the new architecture. Next, Section III presents the main details of the implementation; and Section IV presents the results. Finally, Section V contains concluding remarks and research directions.

II. Proposed Solution

A. *Input dc block in the traditional biquad*

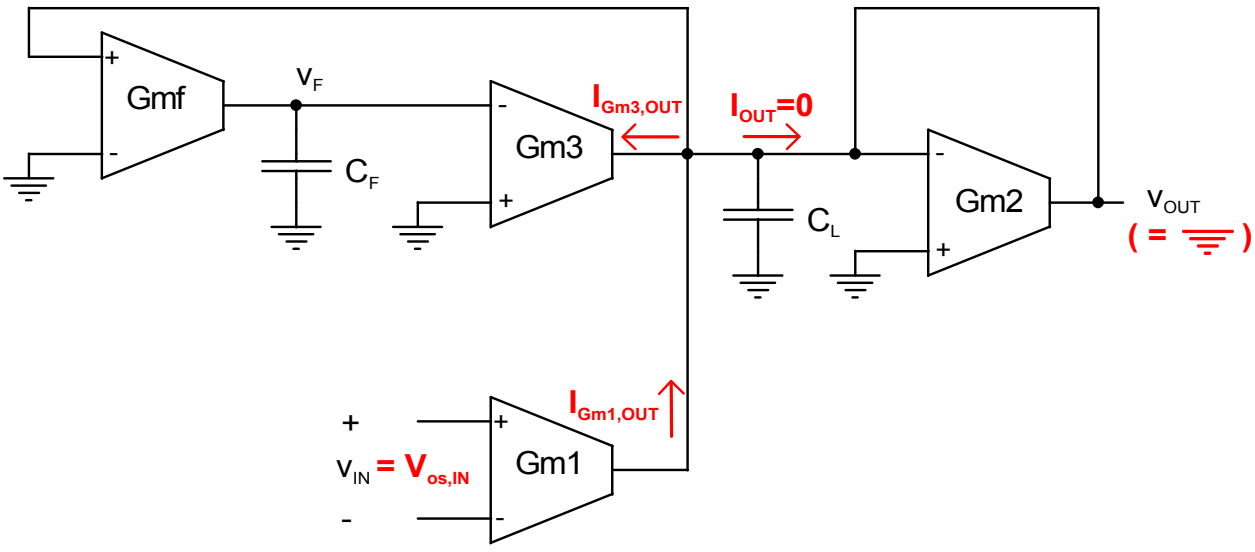

Fig. 1. Traditional biquad architecture of a band-pass filter with amplification [12] p. 847. The input dc blocking mechanism is highlighted: if $V_{os,IN}$ is a dc signal, v_{OUT} will be zero whenever Gm3 is able to drain the Gm1 ouput current ($I_{Gm1,OUT}$). This means that $I_{Gm3,OUT}$ has to be equal to $I_{Gm1,OUT}$. If Gm3 is not able to provide the needed current, the dc input signal won't be blocked and the band-pass characteristic will be lost.

In Fig. 1 a traditional biquad implementation of a band-pass filter with amplification is depicted [12]. In order to facilitate the analysis, this discussion will be presented on basis of a particular architecture of a transconductor (symmetrical OTAs). However, the principle is general and can be extended to other biquad implementations. Then, Gm1, Gm2, Gm3 and Gmf are symmetrical OTAs whose transconductances are, respectively, G_{m1}, G_{m2} G_{m3} and G_{mf}. We shall refer as $2.ID_j$ to the tail current of the input differential pair of Gmj (where j stands for 1, 2, 3 or f).

Gm3 is especially dedicated to establish the high-pass characteristic and block the dc input. Indeed, as shown in Fig. 1, any dc input signal $V_{os,IN}$ will generate a current at the Gm1 output ($I_{Gm1,OUT}$), that will be compensated by Gm3, in order to keep the output voltage v_{OUT} equal to zero (at ground voltage). This compensation will be done by means of the integrator Gmf-C_F. For instance, if $I_{Gm1,OUT}$ rises, then v_{OUT} will rise (Gm2 acts as a resistor to ground), then Gmf will increase its output current and v_F will rise as well, hence the Gm3 output current ($I_{Gm3,OUT}$) will fall. The equilibrium will be reached when $I_{Gm1,OUT} = I_{Gm3,OUT}$.

It is worth to emphasize that it is incorrect to analyze the blocking of the dc input solely on basis of the small signal analysis. This would lead to the wrong conclusion that Gm3 is able to block any level of input dc signal. A large-signal analysis shows that the maximum current that Gm3 is able to provide[1] is $I_{Gm3,OUT} = 2.ID3$, when its input differential pair is totally unbalanced, being $2.ID3$ the tail current of the input differential pair of Gm3. Next, if we consider an arbitrary dc input signal $V_{os,IN}$, then $I_{Gm1,OUT} = G_{m1}.V_{os,IN}$. Hence, the maximum dc input signal that this architecture will be able to block is given by Eq. 1.

$$V_{os,IN} \leq 2.ID3/G_{m1} \tag{1}$$

B. Description of the proposed architecture

In this work we introduce a change in a traditional biquad, aiming to reduce the overhead in terms of power consumption and silicon area that Gm3 introduces. We propose to replace Gm3 with a circuit that rejects the dc component at the output branch of Gm1 and fixes the high-pass frequency (see Fig. 2). The circuit is formed by the transistors M6, M7, M8 and M9 (see Fig. 3). Note that in order to maintain the circuit behavior it is necessary to swap the inputs of Gmf.

[1]For the sake of simplicity, and without loss of generality, we have assumed that the copy factor of the symmetric OTA current mirrors is 1:1.

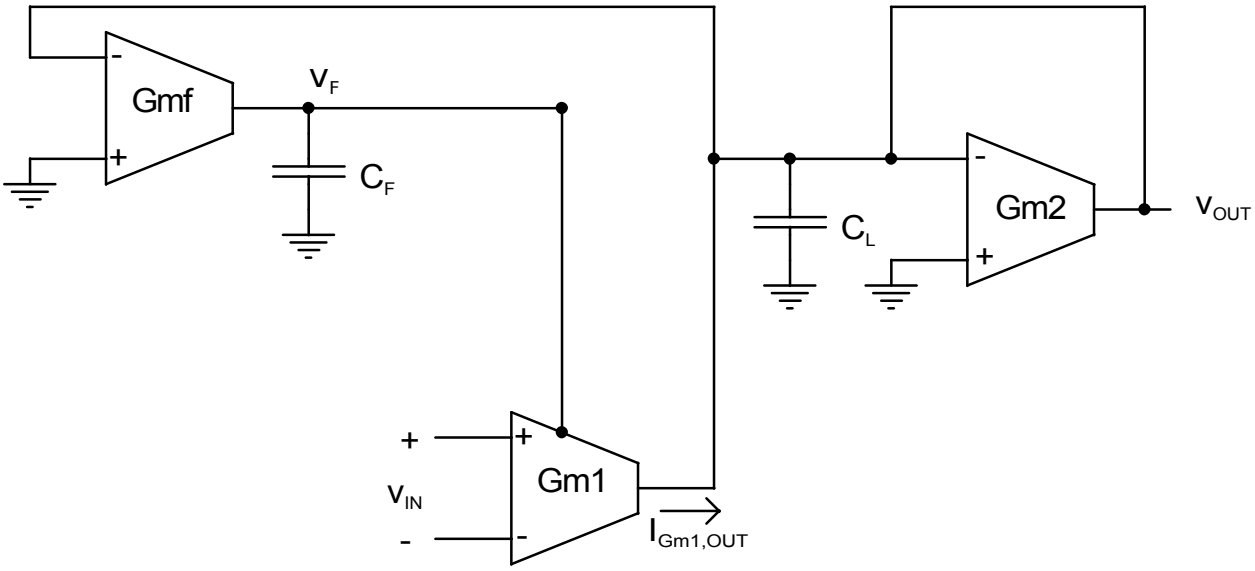

Fig. 2. Proposed circuit architecture.

Gm2 and Gmf are symmetrical OTAs whose respective transconductances are G_{m2} and G_{mf}. Gm1 is a special 3-input OTA (the third input is for the local feedback loop at the output for dc control) with the following transfer function (see Fig. 3):

$$i_{Gm1,OUT} \cong G_{m1} v_{IN} + (g_{m6} + g_{m9}) v_F \tag{2}$$

where G_{m1} is the Gm1 transconductance and g_{m6} and g_{m9} are the transconductance of M6 and M9. As will become clear in Section II-C, in Eq. 2 it was assumed that $gm_{7,8} \gg gm_{6,9}$ where g_{m7} and g_{m8} are the transconductance of M7 and M8.

C. Input dc block circuit

Fig. 3 shows the schematic of Gm1. In an OTA standard structure (without M6 and M9) M7 and M8 would be ordinary cascode transistors, but in this circuit they also perform another function. Jointly with M6 and M9, which are in charge of draining the excess current caused by a dc input signal, they are the core of the input dc block circuit.

Considering dc operation, the current by M1 and M2 is ID1. Any dc input signal in v_{IN} will generate a current ΔI through M1/M2, that will be copied to the output by M4-M5 and

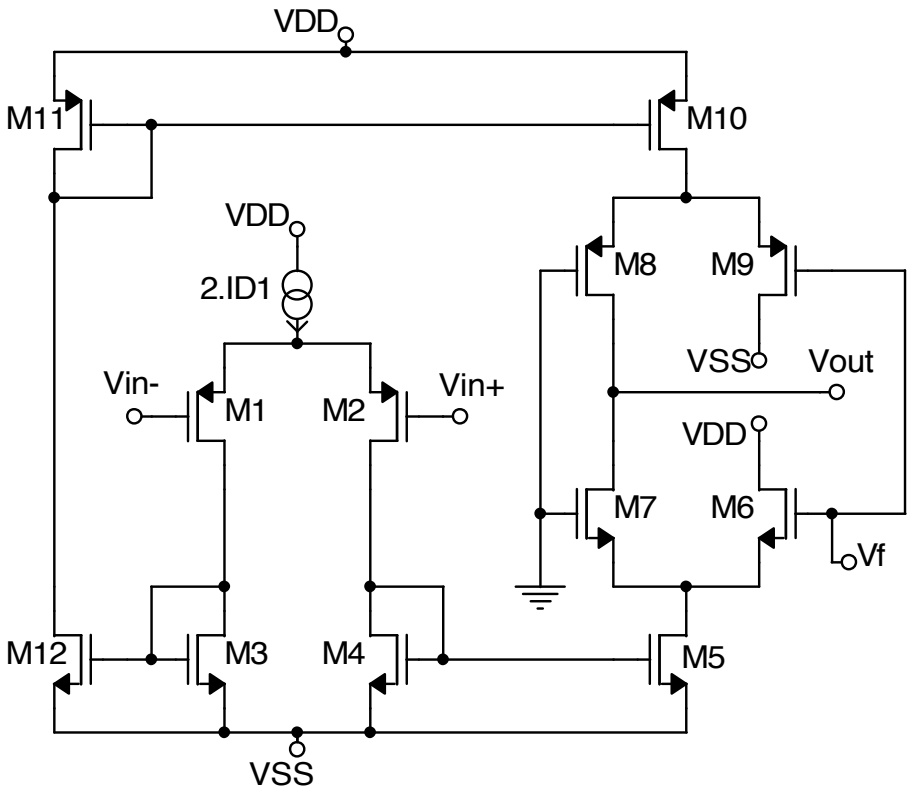

Fig. 3. Gm1 implementation at transistor level. M6-M9 are the dc block circuit.

M3-M12-M11-M10 current mirrors. Then, if M6 and M9 are not present, this current will flow by M7 and M8 and will exit the circuit at the output node.

The M6-M9 block, jointly with Gmf and C_F, are dedicated to establish the high-pass characteristic and to block the dc input. Indeed, the aforementioned ΔI current at the Gm1 output ($I_{Gm1,OUT}$) will be compensated by M6 or M9, in order to keep the output voltage v_{OUT} equal to zero, via the integrator Gmf-C_F.

For instance, when the dc input signal causes the current by M8 ($I_{D,M8}$) to rise (or equivalently causes $I_{D,M7}$, the current by M7, to fall), $I_{Gm1,OUT}$ will rise, then v_{OUT} will rise as well (Gm2 acts as a resistor to ground). Then Gmf will decrease its output current and v_F will fall, making M9 to drain more current (or equivalently making M6 to drain less current). The equilibrium will be reached when $I_{D,M7} = I_{D,M8}$ or consequently when $I_{Gm1,OUT} = 0$. A similar reasoning can be carried out if $I_{D,M8}$ falls (or equivalently $I_{D,M7}$ rises).

It is interesting to note that any mismatch present in the transistors of Gm1, that can generate

a ΔI current, will also be eliminated by the means of this technique.

One side-effect of this technique is that in ac operation, M6 and M9 will drain signal current. Then, if a high level of dc input must be blocked, a loss of gain will be registered. An alternative to overcome this problem is to size M6-M9 in a way that $gm_{7,8} \gg gm_{6,9}$. At this point, it is useful to define α as the ratio between the aspect ratios of M7-M8 and M6-M9: $g_{m7} = \alpha g_{m6}$ and $g_{m8} = \alpha g_{m9}$.

In small-signal operation it can be useful to interpret M6-M7 and M8-M9 as asymmetrical differential pairs where α defines the degree of asymmetry. In the design process, α will be a key parameter. On the one hand, if $\alpha = 1$, the differential pair will be symmetrical, half of the gain will be lost in M6 and M9, and the circuit will be able to block high levels of dc input signals. On the other hand, if $\alpha = 100$ or greater, the loss of gain as well as the capacity of blocking dc input signals will be negligible. A reasonable compromise is to take $\alpha = 10$ where the loss of gain is still negligible and the circuit presents a significant capacity of blocking dc input signals.

D. Transfer function

Assuming that $gm_{7,8} \gg gm_{6,9}$, the circuit depicted in Fig. 2 has the first-order band-pass transfer function presented in Eq. 3.

$$\frac{v_{out}}{v_{in}} = \frac{\frac{G_{m1}}{C_L}s}{s^2 + \frac{G_{m2}}{C_L}s + \frac{(g_{m6}+g_{m9})G_{mf}}{C_L C_F}} \tag{3}$$

and the low-pass frequency $f_{low-pass}$ is given by Eq. 4, the band-pass gain G by Eq. 5 and the high-pass frequency $f_{high-pass}$ by Eq. 6.

$$f_{low-pass} = \frac{G_{m2}}{2\pi C_L} \tag{4}$$

$$G = \frac{G_{m1}}{G_{m2}} \tag{5}$$

$$f_{high-pass} = \frac{(g_{m6} + g_{m9})}{G_{m2}} \frac{G_{mf}}{2\pi C_f} \tag{6}$$

Regarding noise, the performance of both architectures, the traditional biquad (Fig. 1) and the proposed architecture (Fig. 2), is similar and mainly depends on the design of Gm1 and Gm2 (transistor size and transistor inversion level of the input pairs and the current mirrors). Both architectures can provide excellent results in terms of noise, a deeper analysis of noise performance of the proposed architecture can be found in [15].

In summary, this architecture is suitable for low-noise ultra-low-power operation, presents high CMRR, offers an efficient way to block dc input signals and has a well-controlled high-pass frequency (since this frequency is not determined by highly variable MOS-bipolar high valued pseudo-resistors). The high-pass frequency depends on the value of transconductances and capacitances. If higher accuracy is required the transconductance can be automatically on-chip tuned.

III. Implementation

Biquad filters can be used to address different applications. Therefore, in Table I we present a filter specifications that tries to cover a wide range of applications (audio signals, sensor signals, biological/biomedical signals, etc.) without focusing on any in particular.

Based on the specifications established in Table I, two filters were designed and compared. While the first was based on our novel approach (Fig. 2), the second was based on a traditional implementation (Fig. 1).

TABLE I

Filter specifications.

$f_{low-pass}$	$7kHz$
$f_{high-pass}$	$5Hz$
Gain G	$100V/V$
Input dc block	$40mV$
CMRR	$80dB$

The filters were designed and simulated on a $0.5\mu m$ CMOS technology. In the design process, we applied methodologies that use the transconductance over drain current ratio (g_m/I_D) as the variable that guides the design space exploration [16].

The following values were used: $C_L = 2pF$, $C_F = 300pF$, $V_{DD} = 1.65V$ and $V_{SS} = -1.65V$.

The value of C_L was fixed to emulate a typical load capacitance. The value of C_F was chosen based on the low value of the required high-pass frequency, balancing the trade-off between the large area that implies a large capacitor and the need of implementing a ultra-low-value Gmf transconductor.

A. *Proposed architecture*

Given C_L and $f_{low-pass}$, then G_{m2} is fixed by Eq. 4. Hence, as G is given, G_{m1} is fixed by Eq. 5. In order to reduce noise and power consumption, the Gm1 input differential pair is biased in weak inversion (i.e. $(g_m/I_D)_{Gm1InDifPar} \geq 20V^{-1}$), then I_{D1} is fixed. In order to increase the input linear range of Gm2 (which is equal to the maximum expected output amplitude), the Gm2 input differential pair is biased in strong inversion (i.e. $(g_m/I_D)_{Gm2InDifPar} \leq 5V^{-1}$) and I_{D2} is fixed.

According to the discussion presented in Section II-C, α was set to 10. Finally, Gmf, g_{m6} and g_{m9} were established by the means of Eq. 6 and considering the following trade-off. Initially, it is desirable to have low values of Gmf, g_{m6} and g_{m9}, either to lower the high-pass frequency or to reduce the size of C_F. Secondly, low values of Gmf need very large transistors which imply excessively high C_{gs} values (which affects the low-pass frequency).

Table II presents the main parameters of the filter transconductors and Table III the parameters of the dc block circuit.

TABLE II

FILTER MAIN PARAMETERS (NEW APPROACH).

	Gm1	Gm2	Gmf
$(g_m/I_D)_{InDifPar}$	$23.3V^{-1}$	$5.0V^{-1}$	$18.8V^{-1}$
I_D	$352nA$	$17.4nA$	$44pA$
Gm	$8.2\mu S$	$87.2nS$	$834pS$
$(W/L)_{InDifPar}(\mu m/\mu m)$	38.8/1.2	1.5/152	1.5/1294

B. *Traditional implementation*

The design process is similar to the one carried out in the previous section. The only difference concerns the setting of the high-pass frequency. In this case, Gm3 has to be sized instead of

TABLE III

DC BLOCK CIRCUIT PARAMETERS (NEW APPROACH).

g_{m6}	$387nS$
$(W/L)_{M6}$	$1.5/36\ (\mu m/\mu m)$
g_{m7}	$3.66\mu S$
$(W/L)_{M7}$	$1.5/36\ (\mu m/\mu m)$
g_{m8}	$4.36\mu S$
$(W/L)_{M8}$	$1.5/8.3\ (\mu m/\mu m)$
g_{m9}	$411nS$
$(W/L)_{M9}$	$1.5/8.3\ (\mu m/\mu m)$

Gmf, g_{m6} and g_{m9}. For this purpose, Eq. 1 (which implies that $ID3 > 164nA$) and $f_{high-pass} = \frac{G_{m3}G_{mf}}{2\pi C_F G_{m2}}$ will be the design equations. Table IV shows the main parameters of the resulting design for the traditional biquad architecture.

TABLE IV

FILTER MAIN PARAMETERS (TRADITIONAL APPROACH)

	Gm1	Gm2	Gmf	Gm3
$(g_m/I_D)_{InDifPar}$	$23.3V^{-1}$	$5.0V^{-1}$	$18.8V^{-1}$	$5.0V^{-1}$
I_D	$352nA$	$17.6nA$	$44pA$	$176nA$
Gm	$8.2\mu S$	$87.6nS$	$834pS$	$883nS$
$(W/L)_{InDifPar}(\mu m/\mu m)$	38.8/1.2	1.5/152	1.5/1294	1.5/15.2

IV. RESULTS

Monte Carlo (MC) mismatch simulations (100 runs), at transistor level, of the ac, dc, noise and transient analysis were performed in both implementations. Unless otherwise stated, the transient analysis was made with a sinusoidal input signal of amplitude equal to $100\mu V_{PP}$ and a frequency of $1kHz$. I_{DD} is the total current consumption of the filter, v_{ni} is the input-referred noise voltage and the "Output Offset" is the dc voltage deviation from the reference at the output. The "Input Linear Range" is determined by the maximum input voltage where the Total Harmonic Distortion (THD) of the output voltage remains equal or less than 5%. PSRR+ corresponds to

the positive power supply rejection ratio (V_{DD}) and PSRR- corresponds to the negative power supply rejection ratio (V_{SS}).

A. *Proposed architecture*

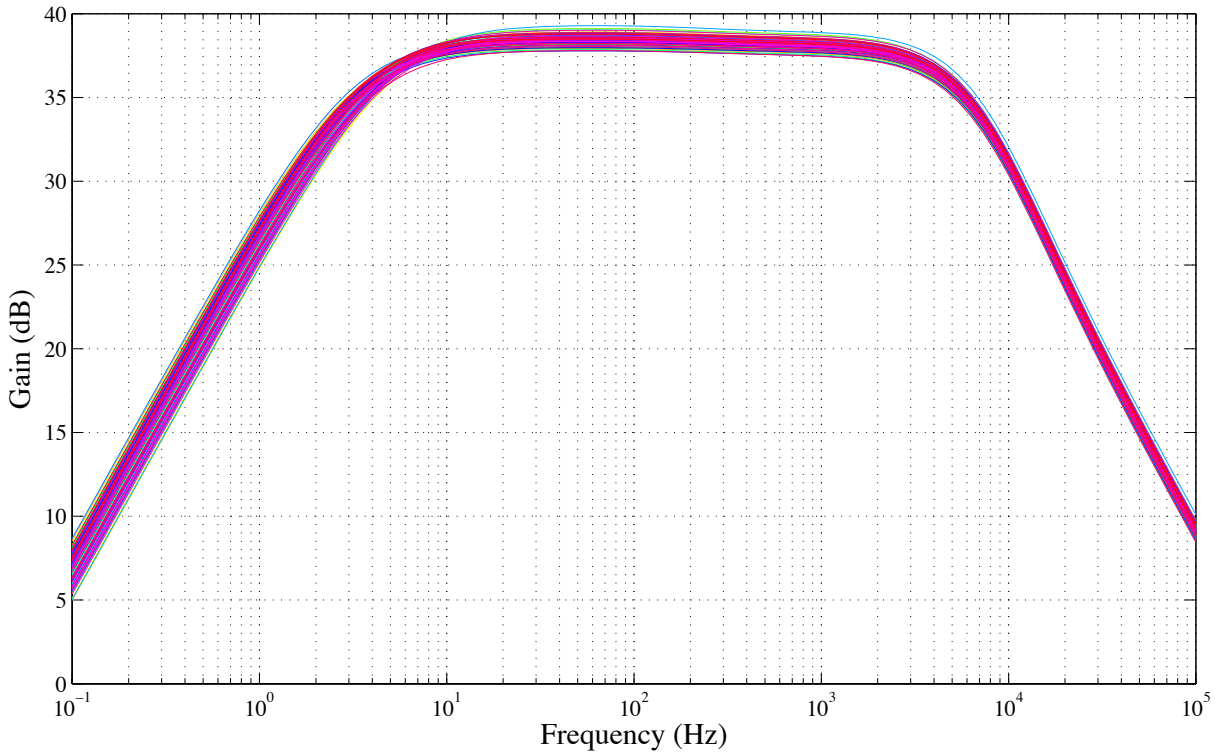

Fig. 4. MC simulations of the filter frequency response (proposed architecture).

Fig. 4 depicts the MC simulations of the filter frequency response of the new approach.

In Table V the simulated main filter characteristics are presented. The MC simulation mean value of the output dc voltage was $1.3mV$ and the standard deviation $\sigma = 4.6mV$. Therefore we have a systematic offset of $1.3mV$ and taking $\pm 3\sigma = \pm 13.8mV$ the worst case of the output voltage would be $15.1mV$.

Ac, dc and transient simulations were performed in order to test the blocking of a dc input $V_{os,IN}$. In Table VI the variations of the filter main parameters are presented.

For the input linear range analysis, a $1kHz$ sinusoidal signal was taken, and the input was varied from $100\mu V_{pp}$ to $10mV_{pp}$. The results are presented in Table VII.

TABLE V

FILTER CHARACTERISTICS (NEW AND TRADITIONAL APPROACH).

	New approach		Traditional approach	
	Typical value	Worst case (of 100 runs)	Typical value	Worst case (of 100 runs)
Gain G	$38.5dB$	$37.8dB - 39.3dB$	$39.5dB$	$38.9dB - 40.2dB$
$f_{low-pass}$	$5.4kHz$	$5.4kHz - 5.5kHz$	$5.4kHz$	$5.3kHz - 5.9kHz$
$f_{high-pass}$	$3.8Hz$	$3.1Hz - 4.6Hz$	$4.6Hz$	$4.3Hz - 4.6Hz$
CMRR	$89,5dB$	$76,6dB$	$90,0dB$	$76,0dB$
PSRR+	$53,5dB$	$51,0dB$	$58,6dB$	$57,7dB$
PSRR-	$65,9dB$	$61,2dB$	$88,5dB$	$81,5dB$
Output Offset	$1.3mV$	$15.1mV$	$1.9mV$	$16.3mV$
I_{DD}	$1.51\mu A$	-	$2.18\mu A$	-
v_{ni}	$14.1\mu V_{rms}$	-	$17.1\mu V_{rms}$	-
Input Linear Range	$8.7mV_{pp}$	-	$8.0mV_{pp}$	-

TABLE VI

FILTER RESPONSE TO AN INPUT DC OFFSET $V_{os,IN}$ (NEW AND TRADITIONAL APPROACH).

	New approach				Traditional approach			
$V_{os,IN}$	Gain G	I_{DD}	THD	$f_{high-pass}$	Gain G	I_{DD}	THD	$f_{high-pass}$
$-100mV$	$26.8dB$	$1.48\mu A$	0.37%	$3.4Hz$	-	-	-	-
$-50mV$	$35.1dB$	$1.48\mu A$	0.35%	$4.6Hz$	-	-	-	-
$-45mV$	$35.6dB$	$1.48\mu A$	0.35%	$4.6Hz$	$37.3dB$	$2.18\mu A$	0.37%	$1.1Hz$
$-10mV$	$38.4dB$	$1.48\mu A$	0.35%	$3.4Hz$	$39.4dB$	$2.18\mu A$	0.37%	$4.4Hz$
$0mV$	$38.5dB$	$1.51\mu A$	0.35%	$3.8Hz$	$39.5dB$	$2.18\mu A$	0.37%	$4.6Hz$
$10mV$	$38.3dB$	$1.56\mu A$	0.35%	$4.3Hz$	$39.4dB$	$2.18\mu A$	0.37%	$4.5Hz$
$45mV$	$35.7dB$	$1.81\mu A$	0.35%	$5.4Hz$	$37.3dB$	$2.18\mu A$	0.37%	$1.2Hz$
$50mV$	$35.1dB$	$1.84\mu A$	0.36%	$5.5Hz$	-	-	-	-
$100mV$	$26.6dB$	$2.05\mu A$	0.37%	$4.0Hz$	-	-	-	-

Table VIII presents process corners simulations of gain, high-pass frequency, low-pass frequency and dc blocking capacity. Both mismatch simulations presented in Table V and process corners simulations presented in Table VIII show that the variations are acceptable.

In order to confirm the stability of the loop of Gmf and Gm1, an open loop simulation was performed for three values of input DC voltage $V_{os,IN} = \{-100mV, 0V, 100mV\}$. The result

TABLE VII

FILTER INPUT LINEAR RANGE (NEW APPROACH).

$v_{IN}(mV_{pp})$	$v_{OUT}(mV_{pp})$	THD (%)
0.1	8.4	0.4
3.5	289	1.0
7.5	670	3.0
8.7	816	4.9
9.0	860	5.6
9.5	940	7.1
10.0	1031	9.0

TABLE VIII

PROCESS CORNER SIMULATION (NEW APPROACH): WORST CASE SPEED (WCS), WORST CASE POWER (WCP), WC0, WC1 AND TYPICAL (TYP).

	$V_{os,IN} = 0V$			$V_{os,IN} = 100mV$		
Corner	Gain G	$f_{low-pass}$	$f_{high-pass}$	Gain G	$f_{low-pass}$	$f_{high-pass}$
wcs	$38.7dB$	$4.9kHz$	$3.7Hz$	$27.6dB$	$4.9kHz$	$4.1Hz$
wcp	$38.2dB$	$5.9kHz$	$3.8Hz$	$25.7dB$	$5.9kHz$	$3.8Hz$
wc0	$38.4dB$	$5.4kHz$	$3.8Hz$	$26.4dB$	$5.4kHz$	$3.8Hz$
wc1	$38.5dB$	$5.3kHz$	$3.8Hz$	$27.0dB$	$5.3kHz$	$3.9Hz$
typ	$38.5dB$	$5.4kHz$	$3.8Hz$	$26.6dB$	$5.4kHz$	$4.0Hz$

depicted in Fig. 5 shows that the loop has a large phase margin in all conditions. This is related to the dominant pole set by Gmf and C_F, which fixes the high-pass characteristic of the overall filter.

B. Traditional implementation and comparison

In Table V the main results of the traditional implementation are presented.

Ac, dc and transient simulations were performed in order to test the blocking of a dc input $V_{os,IN}$. In Table VI the variations of the filter main parameters are presented.

From Table V, it can be seen that both filters comply with the specifications established in Table I. The main difference is that the new approach reduced the power-consumption by 30.7%.

The second main difference is that our approach is able to block a dc input of $100mV$ (or

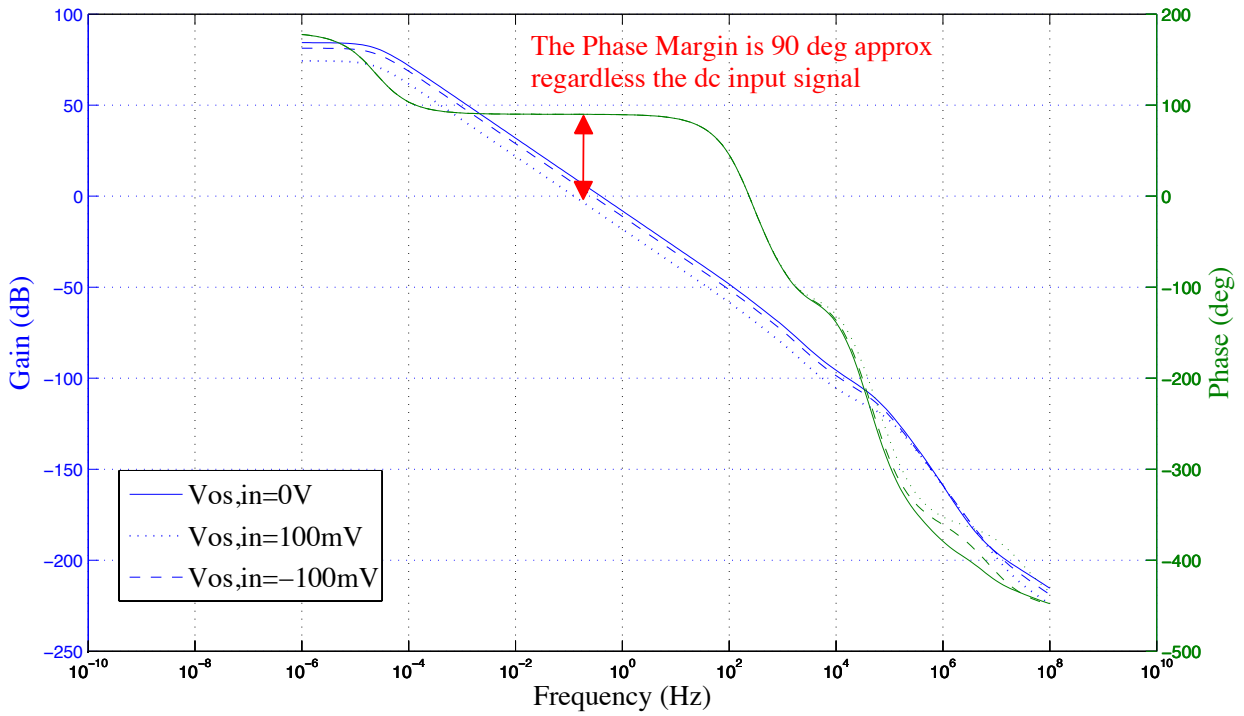

Fig. 5. Gm1-Gmf Open-loop frequency response (proposed architecture).

even higher) while the traditional one lost its high-pass characteristic from a dc input of $50mV$ on, as shown in Table VI.

An increment of $V_{os,IN}$, reduces the gain G and slightly modifies the high-pass frequency $f_{high-pass}$ in both implementations. In our approach the loss of gain is a bit higher, but it has to be pointed out that our implementation continues to give the band-pass characteristic regardless of the dc input. In order to achieve this behavior with the traditional implementation, its power consumption must be increased.

Finally, it is noted that the PSRR- of the traditional approach is higher than the one presented by the new approach. However, the value achieved by the new approach is acceptable for the considered applications.

Table IX compares differential input second order active band-pass filters reported in the literature. Since these filters were designed for different applications, their main characteristics are different, therefore the comparison has to be done carefully. The usage of capacitors to block dc signals allows to block almost any level of input dc signal but it decreases the value of the

CMRR ([2],[17], [18] and [19]). On the other hand, filters based on the traditional approach achieve higher CMRR values but are not able to block high levels of input dc signals ([20], [21] and [22]). To summarize, Table IX shows that the new approach is an efficient way to balance the trade-off between high precision in fixing $f_{high-pass}$, high CMRR and dc input signal blocking capacity.

TABLE IX

COMPARISON OF THE PROPOSED FILTER WITH OTHER DIFFERENTIAL INPUT 2ND ORDER ACTIVE BAND-PASS FILTERS (WHERE N/A STANDS FOR NOT AVAILABLE)

	[17]	[18]	[20]	[21]	[22]	[19]	[2]	This work
Bandwidth (Hz) Δf or f_C/Q	$1.5-370$	$2.0k/3$	$1.95/0.5$	$2.5k/1$	$660/1$	$10k$	$25m-7.2k$	$4-5.2k$
Gain G	$32dB$	$0dB$	$32.9dB$	$0dB$	$73dB$	$0dB$	$39.5dB$	$38.5dB$
Power	$1nW$	$2.85\mu W$	$6.31\mu W$	$16\mu W$	$290nW$	$3.36\mu W$	$80\mu W$	$4.98\mu W$
Input noise v_{ni} (μV_{rms})	27	58	791	38	100	433	2.2	14
CMRR	$60dB$ @$100Hz$	N/A	N/A	$27dB$ @$1kHz$	N/A	N/A	$42dB$ worst-case	$77dB$ worst-case
dc input amp. bounded	No	No	Yes	Yes	Yes	No	No	No
Precise $f_{high-pass}$	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
Dynamic Range (@THD)	$50dB$ (N/A)	$64dB$ (1%)	$51dB$ (1%)	$63dB$ (1%)	$51dB$ (2%)	$66dB$ (5%)	$69dB$ (1%)	$50dB$ (5%)
Supply	$0.6V$	N/A	$3.0V$	$1.2V$	$1.8V$	$2.8V$	$5.0V$	$3.3V$
Technology	$65nm$	$0.35\mu m$	$0.35\mu m$	$0.35\mu m$	$0.35\mu m$	$1.5\mu m$ BiCMOS	$1.5\mu m$	$0.5\mu m$
Application	ECG	Audio, Vibration	IR Sensor	Hearing Aids	Biomed. Device	Bionic Ears	Neural Amplifier	Multiple Purpose
Architecture	Alternat. Gm-C	Alternat. Gm-C	Trad. approach	Trad. approach	Trad. approach	Active RC	Active RC w/ pseudo-resist.	New approach

V. CONCLUSIONS

This paper shows that a significant part of the power consumption of a traditional differential-input biquad, is associated with the feedback loop that fixes the high-pass frequency and blocks

the dc input signals. It was also shown that the power consumption of this feedback loop is dictated by the current that this circuit needs to provide in order to compensate the current due to the dc voltage at the input.

A technique that efficiently blocks the dc input signal and fixes the high-pass frequency was presented and analyzed in depth. Furthermore, an architecture for ultra-low-power differential-input biquads was introduced. This architecture was fully presented with a strong focus in the mechanism that blocks the dc input, deriving the filter transfer function and the main design equations.

The proposed architecture presents, as the traditional approach does, a trade-off between gain and dc input blocking capacity. In our approach the loss of gain is greater than in the traditional approach, but it is remarkable that our implementation does not lose the band-pass characteristic for high dc input values. Therefore, it is possible to exchange gain for dc input blocking capacity.

This work avoids the overhead in terms of power consumption and silicon area that traditional approaches introduce for establishing the high-pass characteristic and to block the dc input. This feature enables lower power consumption or higher levels of dc input to be blocked without jeopardizing the power consumption. Results from MC simulations show that the proposed architecture, compared with a traditional one, presents a 30% reduction in power consumption and more than doubles the dc input that can be blocked.

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