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Reliability Challenges in Design of Memristive Memories

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Abstract—**The demand for highly scalable and low power memory has led to research in emerging technologies and devices. Among these devices, memristors has attracted increased attention as being a promising storage device. However, due to its nano-scale size it faces various types of reliability issues. In this study, we have reviewed the memristive mechanisms and reliability concerns existing in memristor memory design. Then, we have simulated the ionic drift memristor model in presence of the process variability. Next, by considering a normal distribution for the resistive distribution of memristors in LRS and HRS state we have shown the instabilities and probability of failure in read and write procedure of memristive memories, and highlighted the requisite and motivation for the reliability aware memristive circuit design.**

Index Terms—**Keywords-Memristor; Reliability; Variability; Endurance; RRAM; RTN**

I. INTRODUCTION

Redox-based resistive switches (RRAM), more generally termed as memristors are considered as one of the candidates for next generation of memory systems by ITRS [1]. They are compatible with the CMOS process flow and can be scaled smaller than today SRAM and flash technologies (<10 nm) [2]. New architectural paradigms such as crossbars have been proposed, which utilize the memristors for making highly dense memory structures [3]. Additionally, their non-volatile characteristic solves today technology leakage power consumption problem, and all this along with their high-speed operation, makes them a promising memory technology [4].

Memristor was firstly theorized by Chua [5] in 1971, when he predicted the existence of fourth element, relating the flux and charge to each other. However due to technological manufacturing limits it was not until recently physically constructed [6]. Memristor can store data in the state of high or low resistance, where the storage cells can be built by only one resistor (1R), or one transistor and one resistor 1T1R. There exist various types of memristors. Nevertheless, in this paper, we only focus on the binary metal oxide RRAMs. Some popular and frequently used memristors are built with HfOx and TiOx material [7].

To be used as storage devices, fresh memristors are subjected to an electroforming process in order to trigger their resistive switching behavior [4]. This forming process along with manufacturing at nano-scale size of memristors makes them susceptible to various kinds of reliability challenges. For instance, one of these reliability concerns in memristors is the variation of the resistance values from their nominal high and low range. This variability needs to be considered for robust circuit and memory operation.

There have been some efforts to overcome the memristor variability impact with improved processing or innovative circuit and architectural designs. Some of these works include using parallel memristors in order to reduce the variability effect [8]; and employing adaptive circuits to better distinguish the memristor resistance state in the read process [9]. Therefore to make progress in the design of reliable memristive memories, it is essential to analyze these reliability concerns in order to have a better insight for developing novel architectural designs in the field.

This paper is organized as following: Section II reviews some of the important memristor models and mechanisms in the literature; Section III presents the reliability concerns in the memristors; in Section IV and V we demonstrate our simulations regarding with reliability matters in memristors; and finally Section VI concludes the paper.

II. MEMRISTOR MODELS AND MECHANISMS

There are different realizations of the memristors in the literature, and in this section we briefly analyze these mechanisms and models. The first one is based on the published HP paper on memristors [6], where they presented the first physical model of a memristor. It was constructed by two metal layers and a thin film semiconductor of thickness D sandwiched in the middle. The behavioral mechanism of this memristor relies on linear dopant drift of oxygen vacancies by an external voltage bias applied across the device. This would cause a change in the resistance value in respect to rate of change of dopant drifts, where the value LRS corresponds to the lowest resistance value because of high dopant concentration and HRS to highest resistance value due to non-existence of dopants. This memristor model is characterized by the following equations:

$$Rmem=LRS*(x)+HRS*(1-x) \quad (1)$$

$$dx/dt=(\mu*LRS/D^2)*i(t) \quad (2)$$

$$x=w/d \ , 0<x<1 \quad (3)$$

where Rmem is the total memristance, x is the state variable, which its rate of change depends on memristor thickness the current passing through it, LRS and the dopant mobility (μ).

The above equations can result in pinched hysteresis loops of memristors in the simulation. However, the model described by them can get stuck at the boundaries of the state variable x (0 and 1), and also it does not emulate the natural non-linear behavior of dopant drifts manifested at thin film edges. Therefore, to solve these problems a window function is defined and multiplied in the (2) as following:

$$dx/dt= (\mu *LRS/D^2)*i(t)*f(x) \quad (4)$$

The window functions in [10] can overcome both issues, however makes the model predictivity dependent on it.

The second mechanism that describes the memristor switching dynamic is originated from a physics-based model [11]. In this model, the drift diffusion of vacancies in the oxide film is explained by change of w (effective distance of the tunneling gap), because of tunneling distance modulation under an applied voltage or current. This model is characterized by the tunneling current equations [11], and it is very sensitive to the changes of input signal, however it features the non-linear dynamics of memristors.

Finally, the third memristive operation kinetic is based on conductive filamentary (CF) switching. This model is very similar to the dielectric breakdown effect, where the formation and disruption of the CF results in memristor switching to low (LRS) and high resistance values (HRS). Initially the forming process constructs a filament between top and bottom electrodes without connecting them to each other; in this state the memristor is in its HRS mode. Appling a positive voltage at the top electrode moves the ions through the insulating layer and the ion formation between the metal contacts extends the CF and reduces the resistance toward the LRS value, depending on the CF width. In order to switch back the memristor to its HRS mode, a voltage with opposite polarity would reverse the ion migration process and will rupture the CF toward the HRS mode. Note that, the explained conductive filament process also depends on material used for fabrication of memristor [7]. The formulas describing this CF growth and dissolution are presented in [12]. Fig. 1 briefly demonstrates the first and third mechanisms and models (the second model is like the HRS state in Fig. 1.b where a tunneling current occurs), explained above.

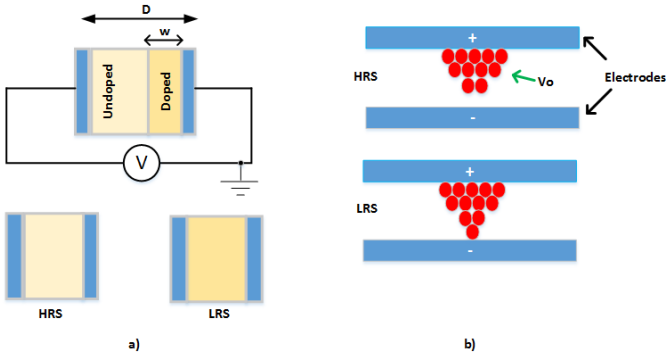

Figure 1. Memristor switching mechanism, a) Ionic drift model, b) Conductive filamentary switching.

III. MEMRISTOR RELIABILITY

The memristors are mainly affected by three reliability concerns: process variability, endurance and Random Telegraph Noise (RTN). In this section we briefly explain each effect.

A. Variability

There are different memristor parameters that fluctuate from their nominal value, such as the memristor's HRS and LRS. These deviations can be categorized into two types: device-to-device and cycle-to-cycle variability, where in this work we do not consider cycle-to-cycle variability in a device.

From the ohmic conduction model the resistance value can be estimated as:

$$R=\rho * L/S \qquad (5)$$

where due to the nano-scale size of these devices there exists variations in area (S) and memristor thickness (L) from the manufacturing process [13]. Also fluctuations in the doping concentration of the oxygen vacancies cause an additional source of variability. Another major reason for the device-to-device variability originates from random electroforming which is needed after device manufacturing in order to form an initial filament. This process can create different size filaments and various channel size in each device [14].

It is reported in the literature that HRS values have higher variations than the LRS values (because of the variations in CFs length) [4], and for this, they are a bigger concern. Furthermore the variability is affected by the device operation, such as higher voltage and bigger pulse width would reduce the resistance variation while the higher temperature increases it. This device-to-device variability will cause read instabilities by reducing the read margin and deviations in write time and write energy.

In this work, we consider the overall impacts of parameters that cause device-to-device resistance variability and assume a normal distribution for the HRS and LRS values, with a defined mean and standard deviation value.

B. Endurance

Another reliability concern in RRAM devices is the limited numbers of write cycles called endurance. This mechanism depends on different parameters, among others, the environment temperature and switching speed. Its effect can be better clarified by a detailed analysis of the set and reset process in RRAM devices.

The set process in RRAM devices is defined as the switching from high to low resistance value. The Oxygen ions (O^{2-}) and oxygen vacancies (Vo) are generated by the electric field in the setting phase, the Vo constructs a conducting filament and the resistance value switches from high to low. However the recombination of O^{2-} and Vo will rupture the filament and cause a switch from low to high resistance, which is called the reset process [15]. Due to the degradation mechanisms, the distance between high and low resistance values cannot remain like the fresh device, and their values would get variations from their expected value. In the literature three types of endurance failure are reported [15]. The first one is when the HRS value goes down in contrast to the LRS values that increase, due to the oxidation at electrodes during the process or forming step. The second failure type is degradation in HRS and decreasing its value because of extra Vo. Finally the third wearout mechanism also impacts the HRS values according to lack of O^{2-} to recombine with Vo. Fig. 2 [15] shows these endurance mechanisms.

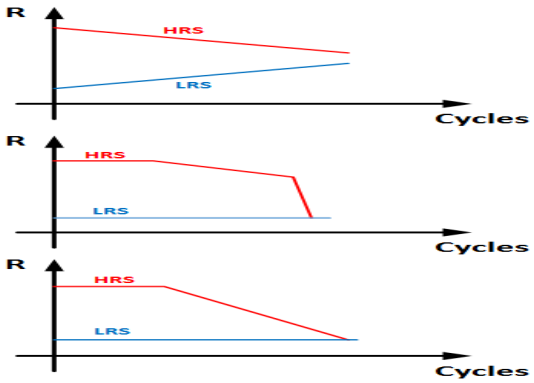

Figure 2. Endurance behavior in memristive devices [15].

It has been reported that by optimizing the set and reset voltages the endurance can be postponed and the number of cycles can get extended in a few orders [16]. Nevertheless, the degraded device cannot recover unlimited number of times because the O^{2-} would be consumed during the device operation, and the conductive filament cannot be successfully ruptured by Vo and O^{2-} recombination.

C. RTN

Random Telegraph Noise (RTN) is a noise phenomenon often seen in semiconductor devices, such as MOSFETs, p-n junctions, metal contacts and metal-insulator-metal (MIM) junctions, etc. It causes discrete random fluctuations between constant values, and has become a significant issue in advanced nano-scale circuit design [17]. The RTN effect is due to capture and emission of charge carriers near the interface and can cause variations of threshold voltage (V_T) and drain current (I_d) in MOSFETs. In RRAM devices the RTN effect generates current fluctuations at high and low resistance values [18]. The current variation by RTN can induce read instabilities in RRAM memories if enough consideration is not taken care.

RTN is usually described by Markovian process [17] where its switching process is assumed at only two discrete values. The distance between these two values is called $RTN_{p.p}$ and is the maximum noise, which might occur. Fig. 3 depicts one example of RTN noise in RRAM current in which two states are considered.

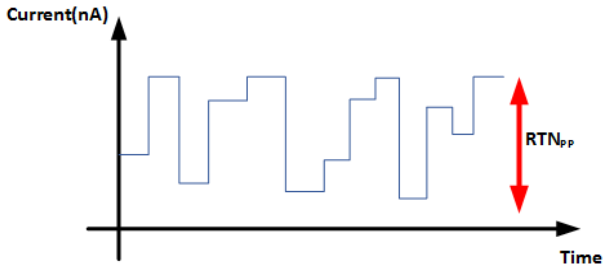

Figure 3. Current fluctuations in RRAM because of RTN.

In this work we also evaluate the impact of two level RTN ($RTN_{p.p}$) in the reliable function of the RRAM memory.

IV. PROCESS VARIABILITY AND AGING ON READING CYCLE

In this section, we present some simulations in Matlab to evaluate the potential reliability concerns in the memristor memories. Our studies are mainly corresponded to the probability of error in the read operation.

Fig. 4 depicts a 200 sample Monte-Carlo analysis of the hp memristor model [6], where we consider variability for LRS and HRS values. The mean values are considered as: LRS=100Ω and HRS=16kΩ, and we assume σ=10% variation in LRS values and σ=20% variation in HRS values, as fresh devices.

Fig. 4 demonstrates how the response hysteresis I-V loop, the memristor current and state variable (x) changes due to the resistance variations. However these graphs cannot tell us how reliable a memristor is in storing and reading the values in memories. Therefore to better analyze the impact of the variations in memristive memories we assume that our memristive crossbar memory (Fig. 5.a) is constructed by 1T1R storage cells [19,20] (Fig. 5.b, to avoid sneak path [21]) and CMOS peripheral [19]. Then, we analyze the graphs of probability of error (Pe) while reading the memristor state (at LRS or HRS state). Note that there are two different mechanisms to read the stored values in crossbar memories; these are based on measuring the memristor current directly or sensing the voltage generated by the memristor current and bitline capacitance and comparing them with a reference value (Fig. 5.c as an example).

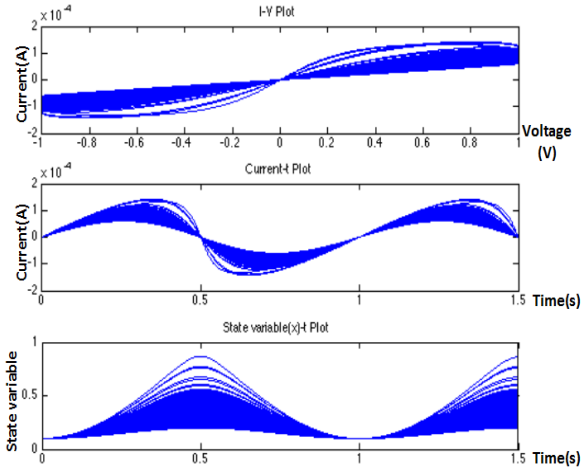

Figure 4. Monte-Carlo analysis of hp memristor model while considering variability effect in HRS and LRS values.

Depending on the memristor is in LRS or HRS state the current would differ and a ´0´ or ´1´ is read from the cell. In this work we do not enter deeply to the read and write circuit and methods of memristive memories and only consider the reliability in terms of memristor resistance values.

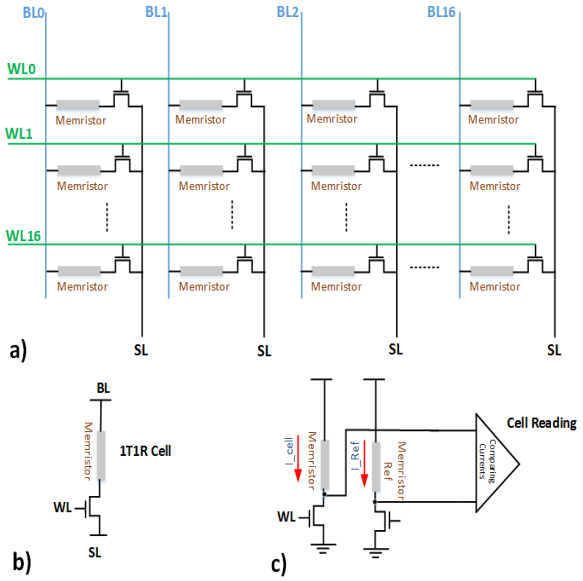

Figure 5. a) 1T1R crossbar architecture, b) The 1T1R cell, c) a read example of 1T1R cell.

In this sense, we consider normal distributions for the LRS and HRS values, a close distance between their mean values, 2X-5X (this is common in multi level storage cells (MLC) and also in aged devices) and plot the probability of error while reading the memristor state. The Pe is a parameter, which determines the possibility of an incorrect read in the memristive memory cell in respect to a reference resistance value (Rth). We plot the Pe graph while considering a reference point in resistance value (in which below Rth it is expected to be in LRS state and higher than Rth the HRS state is anticipated) and sweep it along the two distributions corresponding to LRS and HRS. Fig. 6.a depicts the two LRS and HRS distributions as an example (with mean values=1K, 2K and σ=100, 200 for LRS and HRS correspondingly) and Fig. 6.b shows the evolution of Pe according to the threshold point (the point that differentiates the LRS and HRS modes).

The Pe plot shows the best point to choose as the reference point to have the minimum probability of error while reading the memristor value.

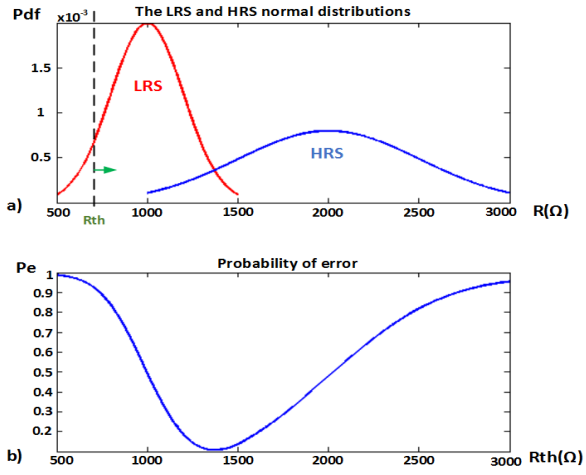

Figure 6. a) HRS and LRS normal distributions and the reference point (Rth) sweeping along them, b) Pe according to the reference point.

Then, in order to have a figure of merit that how the Pe graph evolves according to the distance between the LRS and HRS mean values, we depict the Fig. 7.a. From this graph, we observe that the Pe would vary when the HRS mean value gets far from the LRS mean value. Afterwards, Fig. 7.b correspondingly exposes the values of Pe_{min} converging toward zero, when the HRS and LRS values get far from each other.

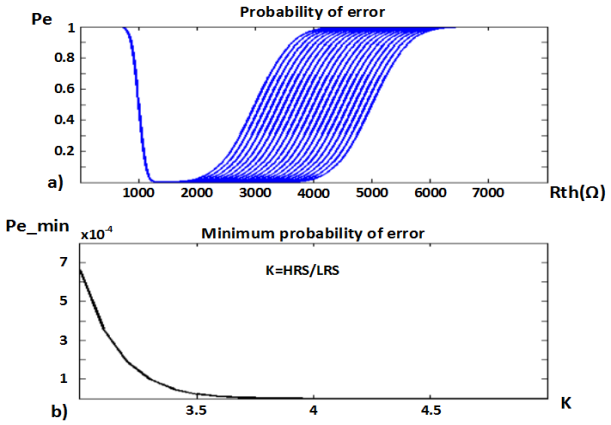

Figure 7. a) HRS and LRS getting distance, b) Pe_{min} according to the distance between HRS and LRS distributions.

Next, to analyze the impact of variability and aging simultaneously, we assume that the two distributions of LRS and HRS would move toward each other (worst case of endurance) in Fig. 8.a and then analyze the elaboration of the Pe graph in Fig. 8.b. As expected, the Pe_{min} value would raise because of the aging of the devices and the fact that they shift toward each other. This would signify the importance of considering the simultaneous impacts of variability and aging for robust and reliable memristive memory design.

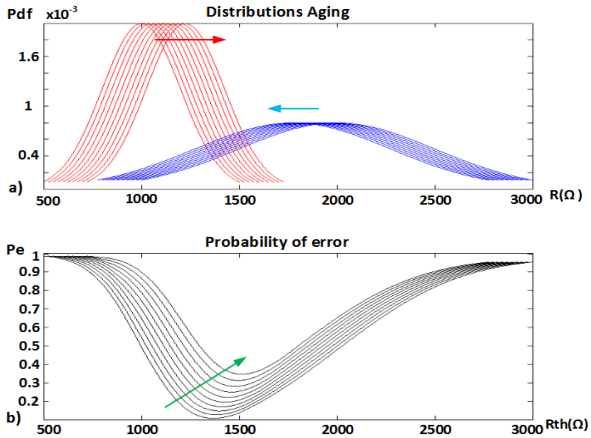

Figure 8. a) HRS and LRS distribution move toward each other because of aging, b) Pe worsens by the aging

Finally, to analyze the impact of RTN in the presence of variability, we have considered two extreme cases for the RTN values (the RTN_{PP} as shown in Fig. 3) and analyzed the Pe graphs. Fig. 9.a presents the LRS and HRS distributions with the RTN_{PP} added (the blue one) and subtracted (the black one) from them. Their combination makes nine possibilities for the Pe graph as shown in Fig. 9.b. One of these combinations develops the highest $Pe_{min,}$ which should be considered at design time.

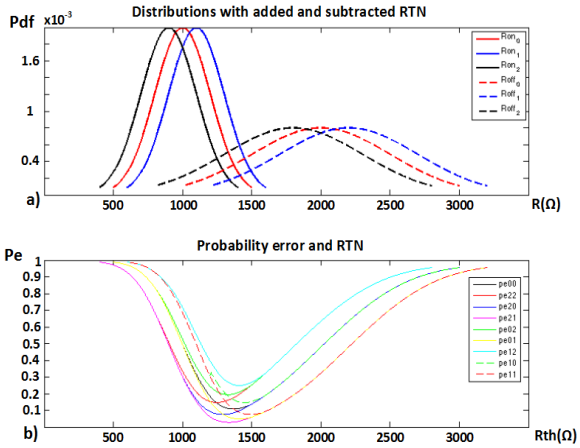

Figure 9. a) HRS and LRS with added RTN, b) Pe graph according to the combination of HRS and LRS distributions

V. PROCESS VARIABILITY ON WRITING CYCLE

There are two techniques for the writing of the memristor devices [8]. The first approach is called the preset writing in which the selected memristor is first reset to the LRS state and then by applying an appropriate pulse it is switched to the desired state. The second method is based on iterative writing and reading pulses until the memristor is written to the proper value.

By applying a squared pulse voltage to the memristor, with amplitude V_A and pulse width Tw we can change the state of memristor. The required duration of pulse Tw to assure the change of the state of memristor (from LRS to HRS and vice versa) in the HP memristor model has been calculated in [22] and can be expressed as follows:

$$Tw=(D^2/(HRS*LRS*2*\mu*V_A))*(HRS^2-LRS^2) \qquad (6)$$

Due to process variability in the memristor devices this write time differs from cell to cell, and therefore would cause error in the case of a limited pulse width. In this work, we have considered variability in LRS and HRS values with the values similar to the previous section. In this context, we have made 10000 Monte-Carlo simulations in Matlab to obtain the distribution of Tw, and then to calculate the probability of the write error in respect to sweep of a reference Tw (variable Tw_ref).

In this sense Fig. 10.a presents the obtained probability density function of Tw while variations in LRS and HRS values are considered following the distributions mentioned in previous sections. We have fitted the generated Tw distribution with a Gamma distribution bounded to [0, ∞]. This distribution is typically used to model aging and time-varying degrading statistic mechanisms.

Next, in Fig. 10.b, we present the probability of error in the write process, while we sweep the Tw_ref along the probability density function. It is shown as the Tw_ref increases (the pulse becomes wider) the probability of the error reduces and converges toward zero, evidently with extra energy cost.

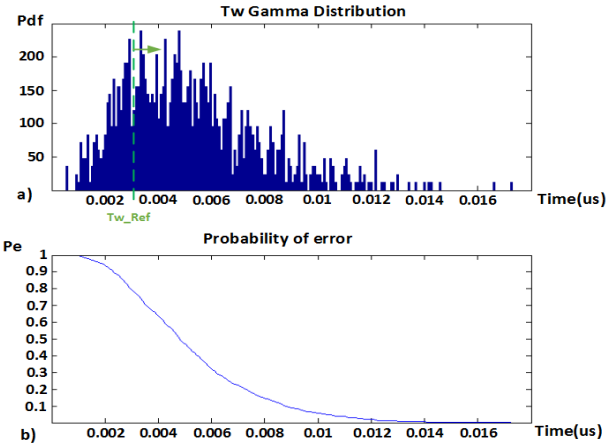

Figure 10. a) Tw according to variability in LRS and HRS values, b) Pe graph according to the sweep of the TW_ref point

VI. Conclusions

In this paper we have considered memristive memories, starting by memristance mechanism and going through the potential reliability effects of process variability, endurance limitation and RTN. Then we have presented some outcomes from the parameter variation in memristive memories, which would increase the probability of failure of the memory system. For instance corresponding to our assumptions, the aging would increase the probability of error up-to 30%; also the RTN impact can be as severe as 30% stochastic variation of error probability in its worst case. In the writing cycle we have concluded a relation between the writing failure probability and the writing pulse duration, which is directly related with the energy required in the process. All this motivates the necessity for design of adaptive and dynamic circuit design techniques to overcome such vulnerabilities.

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