Reliability of Lead-Free Interconnections under Consecutive Thermal and Mechanical Loadings

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To simulate more realistically the effects of strains and stresses on the reliability of portable electronic products, lead-free test assemblies were thermally cycled (–45°C/+125°C, 15-min. dwell time, 750 cycles) or isothermally annealed (125°C, 500 h) before the standard drop test. The average number of drops to failure increased when the thermal cycling was performed before the drop test (1,500 G deceleration, 0.5 ms half-sine pulse). However, the difference was not statistically significant due to the large dispersion in the number of drops to failure of the assemblies drop tested after the thermal cycling. On the other hand, the average number of drops to failure decreased significantly when the isothermal annealing was carried out before the drop test. The failure analysis revealed four different failure modes: (1) cracking of the reaction layers on either side of the interconnections, (2) cracking of the bulk solder, (3) mixed mode of component-side intermetallic and bulk solder cracking, and (4) void-assisted cracking of the component-side Cu_3Sn layer. The assemblies that were not thermally cycled or annealed exhibited only type (1) failure mode. The interconnections that were thermally cycled before the drop test failed by mode (2) or mode (3). The drop test reliability of the thermally cycled interconnections was found to depend on the extent of recrystallization generated during the thermal cycling. This also explains the observed wide dispersion in the number of drops to failure. On the other hand, the test boards that were isothermally annealed before the drop testing failed by mode (4).

Key words: Reliability, lead-free, thermal cycling, isothermal annealing, drop test, JESD22-B111, chip-scale packed (CSP)

INTRODUCTION

Increased functional complexity of portable electronic devices together with the requirements for miniaturization and environmental friendliness creates new reliability concerns. The employment of lead-free materials is giving rise to numerous new material combinations, the reliability performance of which is yet largely unknown. For example, Ni_3Sn_4 intermetallic compound is known to form at the interface between Ni-metallized soldering pads and SnPb solder. However, when even a small amount of copper (more than about 0.3 wt.%) is present in the solder matrix, such as in the near-eutectic SnAgCu solders, the formation of Cu_6Sn_5 is favored over the Ni_3Sn_4 at the Ni|solder interface.[1–6] The metastable solubility of Ni in Cu_6Sn_5 may be as high as 20 at.%,[1,2] even though the stable solubility is only about 4 at.%.[7] The binary Cu_6Sn_5 has shown good structural integrity under mechanical shock loading conditions, but the addition of Ni weakens its mechanical properties.[7–10] Cracking of metastable $(Cu,Ni)_6Sn_5$ has occasionally been observed even in samples prepared after soldering.[8,11,12] Furthermore, structural defects such as the voids discovered in the reaction layer formed on the Ni(P)|Au metallized soldering pads can reduce the reliability performance of the solder interconnections.[1,11–13] As opposed to what occurs in thermally cycled samples,[6,14–16] cracks propagate under fast deformation in the intermetallic layers instead of the bulk solder. This is due to the increased strength of tin-rich solder alloys by strain-rate harden-

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ing.[11,12,17–19] Therefore, good mechanical properties of intermetallic compounds are especially important, when interconnections are subjected to mechanical shocks.

Portable electronic devices are exposed to varying operational environments where mechanical shocks can be a critical threat to their functionality. Also, local temperature gradients inside the products can increase considerably during their operation. This increase in temperature not only can induce thermomechanical fatigue but also changes in the microstructures of the interconnections, and thereby it affects their mechanical properties over time. Conventionally, the reliability of portable electronic equipment has been tested by loading component boards with a single type of stress, typically either purely mechanical or purely thermomechanical, and thus the tests have been carried out with as-soldered microstructures. However, before portable devices are accidentally dropped, their components have undergone at least some thermomechanical loading.

In this paper, the reliability of chip-scale packed (CSP) area array components will be investigated under fast deformation rates with the JESD22-B111 compliant drop test.[20] The effect of component-side metallization, either Ni|Au or copper, on the drop test reliability performance will be studied first in the as-soldered state. The component-side metallization to be used in the tests with combined thermal and mechanical loading will be decided on the basis of the results. Two different printed wiring board (PWB) coatings, Ni(P)|Au or organic solderability preservative (OSP), will be used. The assemblies for these tests will be either thermally cycled or isothermally annealed before drop testing in order to simulate temperature changes due to the use of portable products before drop impact.

MATERIALS AND METHODS

The component was a CSP Sn0.2Ag0.4Cu-bumped 12 mm × 12 mm ball grid array having 500-μm bump diameter and 800-μm pitch. The height of the bumps was 480 μm. The number of bumps per component was 144 and the weight of the component was 0.32 g. The under bump metallization (UBM) of the component-side bump attachment pads was electrochemical Ni with a very thin layer of Au (denoted Ni|Au) or electrochemical copper.

The high-density build-up multiplayer (1 + 6 + 1, FR4) PWBs were manufactured by Aspocomp Group (Salo, Finland) with two different protective coating options on the copper soldering pads: Ni(P)|Au [Ni: 2 μm; immersion Au: ~0.02 μm; and 9 wt.% P in Ni] and OSP (0.2–0.5 μm). The test board shown in Fig. 1 was designed according to the JEDEC board level drop test standard (JESD22-B111).[20]

The component boards were assembled with the laboratory's full-scale production line using Multicore's Sn3.8Ag0.7Cu (wt.%) solder paste, which will result in a nominal interconnection composition of Sn0.5Ag0.5Cu when the solder paste and the component bump alloy have been mixed at the reflow.[6] The solder paste was printed (DEK 265 Horizon, Weymouth, UK) with a 100-mm-thick electroformed Ni stencil and metal squeegees. The mounting machine (Philips ACM Micro, Eindhoven, Netherlands) was set to achieve the highest possible accuracy ($\mu + 5\sigma < 30$ μm, $C_{pk} = 1.67$), and the reflow was carried out in a conventional forced convection oven (EPM/Heraeus EWOS 5.1 N2, Hanau, Germany) under air atmosphere. The temperature profile was set according to recommendations of the solder paste manufacturer. The peak temperature underneath the CSP component was measured (ECD Super MOLE Gold, Milwaukie, OR) as 241°C ± 0.5°C, and the time above 217°C was 50 sec ± 1 sec depending on the component location. Altogether 40 fully furnished test boards were assembled. Only the no via-in-pads side of the test board was used. Half of the PWBs were Ni(P)|Au coated and half were Cu|OSP coated.

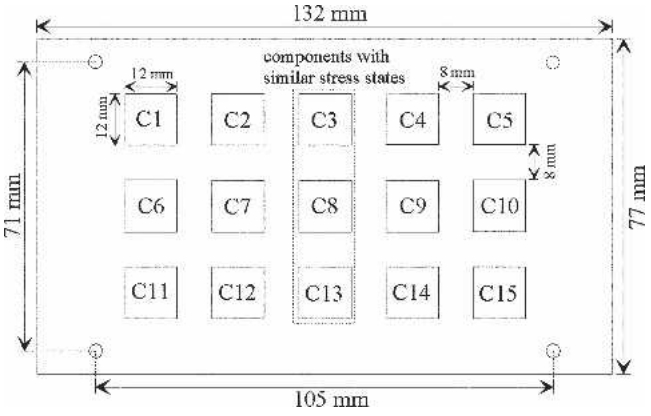


Fig. 1. Layout and dimensions of the drop test board.

After the postreflow inspection, ten assemblies with the Ni|Au (five with Ni(P)|Au and five with Cu|OSP on the PWB pads) and ten assemblies with the copper UBM (five with Ni(P)|Au and five with Cu|OSP on the PWB pads) on the component side were drop tested. Twenty assemblies all having copper UBM were either thermal cycled or isothermally annealed before the drop test. Five Ni(P)|Au and Five Cu|OSP assemblies were thermally cycled in a thermal shock chamber (Weiss TS 130, Menomonee Falls, WI) for 750 cycles according to the IEC 68–2-14N standard (+125°C/–45°C, with 15-min dwell time).[21] The number of cycles was chosen based on earlier experience on the particular component type.[6] Under the above-mentioned conditions, the solder interconnections start to recrystallize below 1,000 cycles, but the first electrical failures are detected only after 1,000 cycles. Isothermal annealing was carried out at 125°C for 500 h again for 5 Ni(P)|Au and 5 Cu|OSP assemblies. The temperature was chosen not to exceed the maximum temperature used in thermal cycling and the T_g of the PWB. The annealing time was chosen based on the growth kinetics of the Cu_6Sn_5 reported in the literature.[22–24] The total thickness of the intermetallic compound layers is expected to grow a few micrometers.

Drop testing was carried out according to the JESD22-B111 standard, but two deviations from the standard were made. (1) Multiple drops due to the bounce back after the initial impact were not eliminated because no means were available to do this. The first bounce back was about 30% of the initial drop height. The implications of this deviation are discussed in Ref. 11. (2) The 1.5 kΩ resistance through the daisy chain network was used as the failure criterion instead of the 1 kΩ, in order to exclude the noise inherent in the measurements. The drop height was set to satisfy the requirement of 1,500 G peak deceleration and 0.5 ms (half-sine pulse) pulse width requirement.

The failure mechanisms were studied from cross sections prepared by standard metallographic methods. Cross sections were investigated with optical microscopy (Olympus BX60, Tokyo, Japan) and field emission–scanning electron microscopy (FE-SEM) (JEOL 6335F, Japan Electron Optics Ltd., Tokyo). Polarized light was used in the optical microscopy because the reflection is dependent on grain orientation and thus differently oriented grains appear in different colors on the micrographs. The distribution of the elements in the interconnection interfaces was analyzed by energy dispersive x-ray spectroscopy (EDS) (Oxford, INCA, Oxon, UK).

The reliability of the solder interconnections was studied by employing a full-factorial design with five replications. When the component locations with the same type of loading were combined, the amount of replications was tripled. The type of PWB coating, the components pad metallization, and the pretreatment were the main variables studied. A factorial experiment, which is a series of experiments carried out according to the principles of experimental design, allows investigation of the main and interaction effects of the variables and the determination of the statistical significance of the effects. In full-factorial design, all possible combinations of the factor levels are used. By replicating experiments, an estimate of the experimental error can be given, which is the basic measure for determining whether the observed differences in the data are statistically significant. The difference in reliability performance is evaluated on the basis of average drops to failure. Parametric methods are based on the assumption that the data are normally distributed. The test for normality was that of Shapiro–Wilk.[25] When the drops to failure does not follow the normal distribution, nonparametric methods must be used to test the equality of two populations. The Wilcoxon rank-sum test procedure is almost as powerful as the two-sample T-test, and therefore, it was used in this work.[26]

The Weibull parameters were calculated by making use of the three-parameter cumulative Weibull-distribution function, which is given by

$$F(t) = 1 - \exp\left[-\left(\frac{t-\gamma}{\eta}\right)^{\beta}\right]$$

where F(t) is the cumulative density function, η is the characteristic lifetime, β is the shape parameter, and γ is the failure free lifetime. If the failure data plots with a concave trend and the fit of the regression are therefore poor, this may indicate the presence of a failure-free lifetime and the third parameter γ should be introduced. Otherwise, the γ equals zero.

RESULTS AND DISCUSSION

In order to make use of as many data points as possible in the reliability analysis, the three middle components, C3, C8, and C13 in Fig. 1, were pooled to form a single sample per test board. The difference in the drops to failure on the three component locations was studied separately for both the coating options with the use of the Wilcoxon rank-sum test, and no significant differences could be found. To validate the pooling of component locations, the maximum longitudinal strains during the impact at different component locations were calculated by the finite element method and verified experimentally.[11] The average drops to failure with standard deviations are shown in Fig. 2.

Table I presents the Weibull parameter estimates of the drop-tested samples. The difference in the η values cannot be tested statistically and therefore the reliability performance must be compared based on the average drops to failure (Fig. 2). Based on the Shapiro–Wilk Test for normality, the drops-to-failure data did not comply with the normal distribution and therefore the significance must be tested with nonparametric methods. In engineering sciences, the statistical confidence levels of more than 95% typically can be considered sufficient to reject the null hypothesis, and therefore all the tests in this paper are carried out at less than 5% risk level (α).

Reliability Comparison between Copper and Ni|Au UBMs

The choice of component-side metallization was studied with the as-soldered assemblies by making use of the 2^2 full-factorial design and the Wilcoxon rank-sum test. The effect of both factors, the PWB metallization and the component-side metallization, was statistically significant: the copper metallization on the component side is more reliable than the

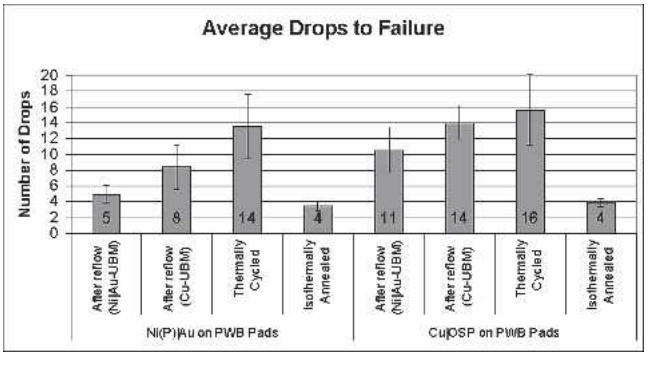


Fig. 2. Average drops to failure with standard deviations.

Table I. Estimated Weibull Parameters

PWB Coating	Predropping Treatment	η	β
Ni(P)/|Au	no aging (Ni)–ref.	6	1.7
	no aging (Cu)	10	1.5
	thermal cycling	16	1.3
	isothermal annealing	4	3.1
Cu|OSP	no aging (Ni)–ref.	12	1.9
	no aging (Cu)	16	3.7
	thermal cycling	18	1.8
	isothermal annealing	4	3.7

electrochemical nickel (α = 4.7%) and, on the PWB side, the Cu|OSP is more reliable than the Ni(P)|Au (α = 0.2%). No interaction existed between the two factors.

The failure analyses revealed that cracking of the reaction layers on either side of the interconnections was the primary failure mode (failure mode (1)). Regardless of the component-side metallization interconnections on the Ni(P)|Au metallized boards failed at the PWB side exhibiting cracking of the brittle reaction layers between the Ni(P) metallization and the bulk solder (Fig. 3a). The reasons for the inferior reliability performance of the Ni(P)|Au PWB coating have been discussed in more detail elsewhere.[12,13] The solder interconnections on the Cu|OSP coated PWBs failed at the component side, where cracks propagated through the $(Cu,Ni)_6Sn_5$ or the Cu_6Sn_5 reaction layer depending on the component UBM: $(Cu,Ni)_6Sn_5$ on the Ni|Au metallization and Cu_6Sn_5 on the copper metallization (Fig. 3b). The reason for this failure mode is that, under fast deformation rates, the flow stress of the solder is increased and stresses concentrate at the corner regions of the interconnections where the fracture strength of the intermetallic reaction zone is exceeded.[12]

The increase in the reliability when the component-side metallization is changed from Ni|Au to copper can be explained with the differences in mechanical properties of the intermetallic layers. As noted earlier, the addition of Ni has been observed to weaken the mechanical properties of Cu_6Sn_5 by producing severe cracking of the intermetallic phase. The cracking of the $(Cu,Ni)_6Sn_5$ is sometimes visible even after reflow.

Failure Mechanism in the Samples Drop Tested after Thermal Cycling

The effect of the thermal cycling on the drop test reliability was studied by making use of the 2^2 full-factorial design and the Wilcoxon Rank-Sum Test. The diagram in Fig. 2 shows an increase in the number of drops to failure when the thermal cycling treatment is carried out before the drop test, but the difference was not statistically significant (α = 19.3%). The reason for this is the relatively large dispersion in the drops to failure of the thermally cycled assemblies. The effect of PWB metallization was also not statistically significant.

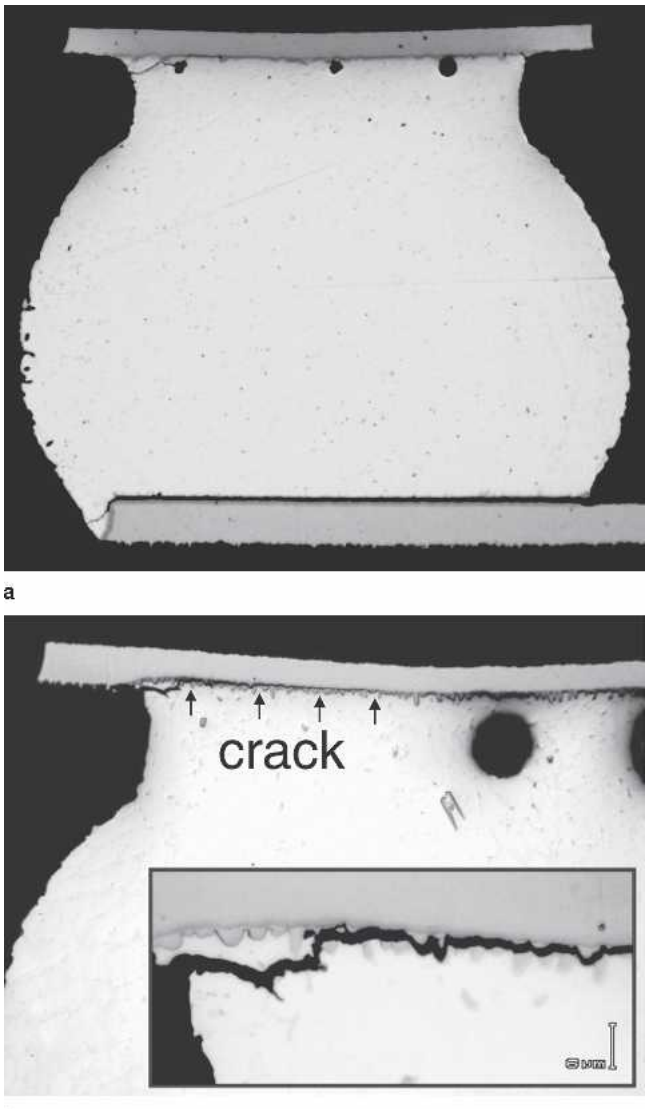
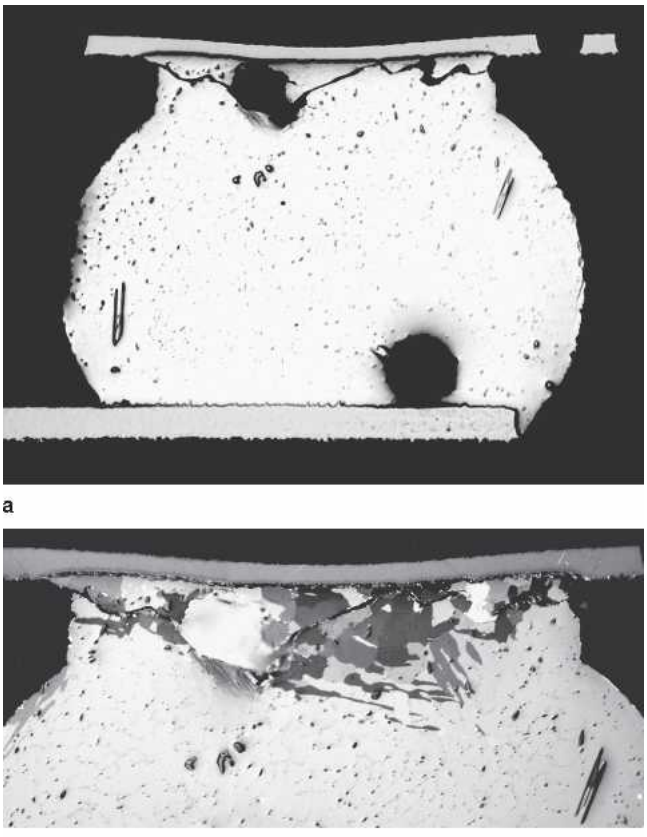


Fig. 3. Failure mode (1) of the as-soldered interconnections on (a) Ni(P)Au: brittle intermetallic fracture through the reaction layers between the Ni(P) and the bulk solder, and (b) CuIOSP: fracture through the Cu_6Sn_5 reaction layer.

It is interesting, however, that the failure mechanism has changed from that observed in the interconnections drop tested in the as-soldered state. In addition, the failure mode was the same regardless of the board-side metallization. The failure mechanism has changed from the brittle fracture through the intermetallic layers to intergranular fracture through the bulk of the solder. The cracks often propagate entirely in the bulk solder through the interconnection (failure mode (2)) but sometimes only partially propagate in the bulk solder and afterward move into the intermetallic compound layers (failure mode (3)). The cracks typically locate on the component-side "neck region" of the interconnections (Fig. 4a).

Because the thermal cycling alone determined the type of failure mode, the reason for the change in the failure mechanism has to do with the thermome-



a

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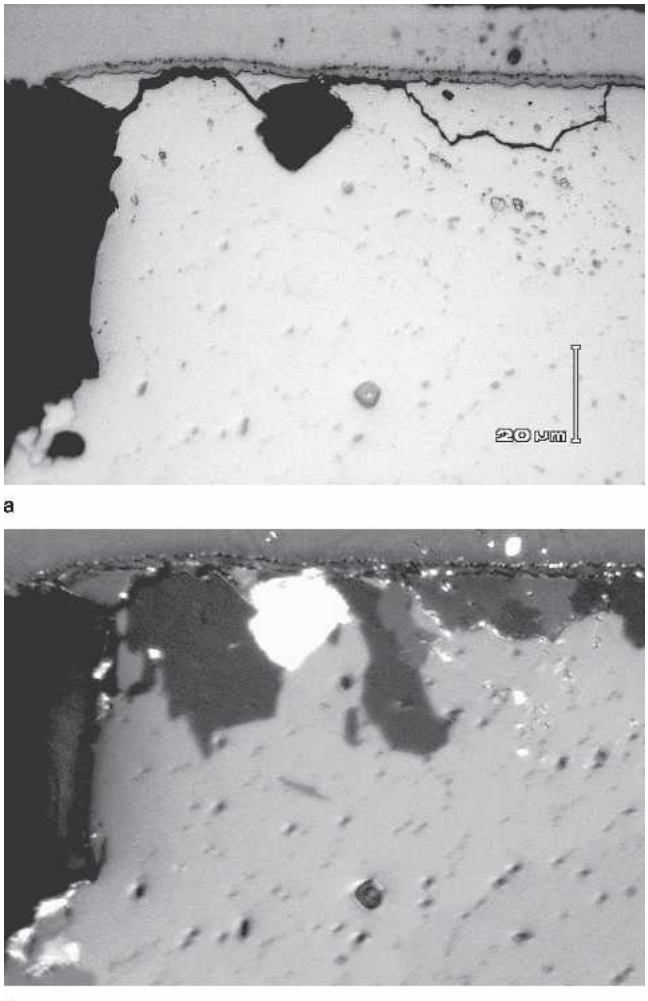
Fig. 4. Intergranular fracture through the bulk of the solder in thermally cycled interconnection (failure mode 2).

chanical stresses and the subsequent microstructural evolution produced during the thermal cycling. The microstructures of the solder interconnections that were formed during reflow soldering consist of relatively few colonies with high-angle boundaries between them. Inside these colonies, a cellular structure with small angle boundaries can be seen.[6,27] High-angle boundaries are required for cracks to grow intergranularly through the solder interconnections. These high-angle boundaries rarely run in a favorable orientation with respect to the highest normal stress, and therefore, they cannot provide potential sites for cracks to nucleate and propagate. However, due to recrystallization during thermal cycling, numerous new grain boundaries are generated. The recrystallization occurs first near the corner region of the interconnections, where the structure is the most heavily deformed plastically. The local recrystallization of solder interconnections enhances cracks to nucleate in and propagate through the recrystallized solder interconnections. The formation of a continuous network of high-angle (grain) boundaries enables intergranular fracture of interconnections. This change in the fracture mode from brittle intermetallic fracture to intergranular fracture can explain both the apparent increase in the average drops to failure and the large deviation.

Figure 4b shows the image taken with polarized light from the same interconnection from which the bright light image in Fig. 4a is taken. The reflection of the polarized light is dependent on the grain orientation of the surface, and therefore the different colors in the images represent different orientations. Figure 5 shows that when the network of high-angle boundaries is no longer available, the cracks grow further in the intermetallic layers between the metallization and the solder owing to strain rate hardening. Thus, when the assemblies have been thermally cycled, the drop test reliability is dependent on the extent of recrystallization in addition to the strain-rate hardening.

Failure Mechanism in the Samples Drop Tested after Isothermal Annealing

The assemblies isothermally annealed before the drop test performed significantly weaker than the other assemblies ($\alpha = 3.3\%$). The failure mode, cracking of Cu_3Sn layer, is different from what has previously been observed and the mode was the same regardless of the board-side coating. The



a

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Fig. 5. A change from intergranular fracture to brittle intermetallic fracture as the grain boundaries are no longer available (failure mode 3).

cracks nucleated in the bulk solder, but directly after nucleation, the cracks moved into the Cu_3Sn layer, where they propagated all over the interconnections.

The component-side intermetallic reaction zone of the interconnections is composed of two intermetallic compounds between the copper pad and the bulk solder: a thin uniform layer of Cu_3Sn next to the copper bump pad and a thick scallop-type layer of Cu_6Sn_5 between the bulk solder and the Cu_3Sn layer. The detailed microscopic studies executed after the reliability testing revealed that a great amount of voids formed inside the Cu_3Sn layer. The voids formed almost a continuous path that enabled the cracks to propagate by breaking the ligaments between adjacent voids (failure mode (4)). The fracture path is located, relative to the height of the Cu_3Sn layer, on the copper side rather than on the Cu_6Sn_5 side (Fig. 6). The thermally cycled samples were carefully investigated for similar behavior, and similar but smaller voids formed in the same phase, although their number was too small to have an effect on the failure mechanism.

In order to understand the failure mechanism, the general sequence of events during the formation of the reaction zone is discussed briefly. Immediately after the flux has removed oxides and the solder wetted the copper metallization, it starts dissolving into the molten solder. Very high local copper concentrations can be realized in the very vicinity of the Cu|liquid interface because the composition of the liquid is governed by the metastable solubility limit, which is higher than the stable one. After supersaturation, the molten solder immediately adjacent to the layer of copper starts forming solid Cu_6Sn_5 by the heterogeneous nucleation.[28,29] However, because copper is not in equilibrium with Cu_6Sn_5, reaction in this intermetallic zone will continue through solid-state diffusion to form a thin layer of Cu_3Sn between the copper pad and the Cu_6Sn_5. The formation of Cu_3Sn starts, in fact, already at the reflow soldering because a very thin dark layer can be observed between the copper and the Cu_6Sn_5 even with the optical microscope.

The layer of Cu_3Sn generated during soldering is very thin as compared to the thickness of the Cu_6Sn_5 phase; however, naturally, the thicknesses of both these layers grow during the solid-state annealing, i.e., during the use of electronic products. The diffusion rate of copper in Cu_3Sn is known to be much higher than that of tin and therefore the growth rate of the Cu_6Sn_5 phase in solid state is higher than that of the Cu_3Sn phase.[23,30] Oh measured the diffusion rates in Cu_3Sn and found that the rate of copper diffusion is about 3 times that of tin. The voids locating at the vicinity of the Cu|Cu_3Sn interface indicate that they are Kirkendall voids, as suggested by some authors.[31–33] However, the issue seems to be more complicated because we found voids in the Cu_3Sn layer only on the component side of the interconnections but not on the PWB side. The amount of impurities has been observed to affect the formation of voids in the Cu_3Sn layer.[1]

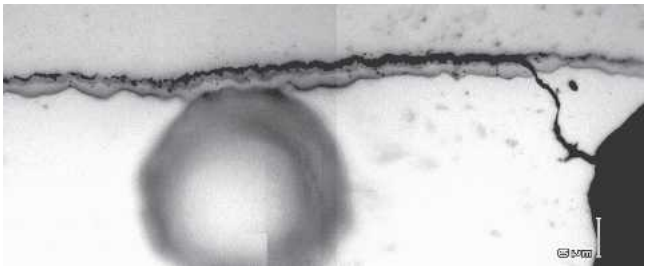

Fig. 6. Fracture through the voids inside the Cu_3Sn in the isothermally annealed interconnection (failure mode 4).

CONCLUSIONS

The effects of component-side metallizations on the drop test reliability were first studied with as-soldered assemblies. The copper UBM was found to be more reliable than the electrochemical nickel ($\alpha = 4.7\%$). On the bases of this result, the copper metallized components were chosen for drop tests with combined thermal and mechanical loadings. The drop test results of the thermally cycled or isothermally annealed assemblies were compared to the results achieved with the assemblies drop tested in the as-soldered state. Both pretreatments affected the drop test reliability, but the effects were different: the thermal cycling increased and the isothermal annealing decreased the average number of drops to failure. The difference between the average drops to failure of the thermally cycled and as-soldered assemblies was not statistically significant ($\alpha = 19.3\%$) owing to the large dispersion in the drops to failure of the thermally cycled test boards. The type of PWB coating affected the drop test reliability only in the as-soldered state, where the interconnections on the Cu|OSP were more reliable than those on the Ni(P)|Au ($\alpha = 0.2\%$).

The as-soldered, thermally cycled, and isothermally annealed test boards showed different failure modes. The as-soldered assemblies exhibited only brittle intermetallic cracking of the reaction layers (Cu_6Sn_5 or phosphide) on either side of the interconnections (mode (1)).

When the thermal cycling preceded the drop test, the failure mode changed to intergranular fracture through the bulk solder, and the failure mode was the same regardless of the board-side metallization. The cracks propagated either entirely through the bulk solder (mode 2) or first through the bulk and later on moved to the intermetallic layers (mode (3)). The change in the crack propagation can be explained in terms of the formation of continuous networks of grain boundaries by recrystallization. The high-angle boundaries of the recrystallized grains provide favorable paths for cracks to propagate. Once a crack tip reaches the border of the recrystallized area, it continues to propagate in the intermetallic compound layers due to the increased flow

stress of the nonrecrystallized part of the interconnections.

The assemblies isothermally annealed before the drop test were significantly weaker than the other assemblies. The failure mode was again different from what had been observed previously, and the mechanism was the same regardless of the boardside coating. The cracks nucleated in the bulk solder, but directly after the nucleation, they entered the Cu_3Sn layer. The large numbers of voids being formed in the Cu_3Sn layer during isothermal annealing constitute almost continuous paths for cracks to propagate through the entire interconnections.

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