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ORIGINAL ARTICLE

Reliability prediction of semiconductor devices using modified physics of failure approach

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Abstract Traditional approaches like MIL-HDBK, Telcordia, and PRISM etc. have limitation in accurately predicting the reliability due to advancement in technology, process, materials etc. As predicting the reliability is the major concern in the field of electronics, physics of failure approach gained considerable importance as it involves investigating the root-cause which further helps in reliability growth by redesigning the structure, changing the parameters at manufacturer level and modifying the items at circuit level. On the other hand, probability and statistics methods provide quantitative data with reliability indices from testing by experimentation and by simulations. In this paper, qualitative data from PoF approach and quantitative data from the statistical analysis is combined to form a modified physics of failure approach. This methodology overcomes some of the challenges faced by PoF approach as it involves detailed analysis of stress factors, data modeling and prediction. A decision support system is added to this approach to choose the best option from different failure data models, failure mechanisms, failure criteria and other factors.

Keywords Physics of failure · Reliability prediction · Time to failure · Failure mechanism · Failure mode · Failure modeling

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1 Introduction

The basic idea of the project is to predict the reliability of some specific components, which are used in the nuclear industry by methods called Reliability Prediction and Modeling Techniques. Reliability modeling and prediction is a relatively new discipline. Only since World War II reliability has become subject of study due to the relatively complex electronic equipment used during the war and the high failure rates observed. Reliability modeling and prediction is a methodology for estimating an item's ability to meet specified reliability requirements. A Mission Reliability prediction estimates the probability that an item will perform its required functions during the mission. A basic Reliability prediction estimates the demand for maintenance and logistic support caused by an item's unreliability. Reliability models and predictions are not used as a basis for determining the attainment of reliability requirements. Attainment of these requirements is based on representative test results such as those obtained by using tests plans from MIL-HDBK-781, Telcordia, PRISM, Physics of Failure etc. Reliability modeling and prediction should be initiated early in the configuration definition stage to aid in the evaluation of the design and to provide a basis for item reliability allocation and establishing corrective action

priorities. Reliability models and predictions are updated when there is a significant change in the item design, availability of design details, environmental requirements, stress data, failure rate data, or service use profile.

1.1 Reliability prediction

There have been two eras of Reliability Prediction. Until the 1980s, the exponential, or constant failure rate (CFR), had been the only model used for describing the useful life of electronic components. It was common to the six reliability prediction procedures that and was the foundation of the military handbook for reliability prediction of electronic equipments (MIL-HDBK-338B). Although the CFR model was used without physical justification, it is not difficult to reconstruct the rationale for the use of the CFR model, which mathematically describes the failure distribution of systems wherein the failures are due to completely random or chance events. Throughout that period, electronic equipment complexity began to increase significantly. Similarly, the earlier devices were fragile and had several intrinsic failure mechanisms that combined to result in a constant failure rate.

1.1.1 MIL-HDBK-217

During the 1980s and early 1990s, with the introduction of integrated circuits (ICs), more and more evidence was gathered suggesting that the CFR model was no longer applicable. Phenomena such as infant mortality and device wear out dominated failures; these failures could not be described using the CFR model. They further recommended that the exponential distribution should not be applied to every type of component and system without due awareness. The methods to find failure rate are (MIL-HDBK-338B; MIL-HDBK-217F):

1. The constant-failure-rate: The constant-failure-rate reliability model is used by most of the empirical-electronic reliability prediction approaches.
2. π factors: Almost all of the traditional prediction methods have a base failure rate modified by several π factors.
3. Two basic methods for performing reliability prediction based on the data observation include the parts count and the parts stress analysis. The parts count reliability prediction method is used for the early design phases, when not enough data is available but the numbers of component parts are known.

$$\lambda_S = \sum_{i=1}^{n} N_i (\lambda_g \pi_Q)_i \qquad (1)$$

The inconsistency among different traditional prediction methods is the main problem facing designers.

1.1.2 Physics of failure approach

Attempts, which began during the 1970s, to include physics-of-failure into military handbooks were not very successful. Although the need for a physics-of-failure methodology was realized in the 1970s, a physics-of-failure-like model for small-scale CMOS technology was not introduced until 1989. Even so, this approach, as an independent methodology, only started to attract attention during the 1990s in the form of recommendations to update the military handbook (Pecht and Kang 1988). The recommendations addressed the weaknesses of traditional approaches (White 2008):

- the misleading use of constant physics-of-failure,
- the use of the Arrhenius temperature model,
- the modeling of wear out mechanisms, and
- modeling mechanisms such as brittle die fracture.

Since then, the physics-of-failure approach has dominated reliability modeling. In this approach, the root cause of an individual failure mechanism is studied and corrected to achieve some determined lifetime. Since wear out mechanisms are better understood, the goal of reliability engineers has been to design dominant mechanisms out of the useful life of the components by applying strict rules for every design feature. The theoretical result of this approach is, of course, that the expected wears out failures are unlikely to occur during the normal service life of microelectronic devices. Nonetheless, failures do occur in the field and reliability prediction has had to accommodate this new theoretical approach to the virtual elimination of any one failure mechanism limiting the useful life of an electronic device. It depends on process, technology, manufacturer location, post processing techniques etc.

Physics-of-failure is an approach that tries to reveal and model the root cause processes of device failures. This branch of reliability combines knowledge about the device with the statistical aspects of failure occurrences. The fact that physics-of-failure is not widely used by engineers shows that it was not successful in achieving its goals. It seems that the key element of this lack of success is the complexity of modeling the MTTF of devices based on the underlying root causes. Moreover, the physics of device failures has not yet been clearly formulated. Scientists are still working on formulating the reasons behind each failure.

Moreover reliability aspects and prediction is critical to these components and this paper provides advanced physics of failure methodology for finding failure characteristics and reliability indices. The following Table 1 demonstrates various traditional prediction methods the differences between the values of time to failures of DC–DC converter constraints the ambiguity and risk in selecting appropriate figure.

There were significant advantages to this methodology like reliability design, condition monitoring, improvement in LCC and component selection to the application involved. This method requires sophisticated tools for failure analysis and advanced tools for analyzing the simulated data. Still, this methodology also has challenges like insufficient data from the manufacturer, needs expert judgment and also time taking process (MIL-HDBK-217F; White 2008; Panasonic Corporation 2000; Renesas Technology Corp 2008).

On the other hand, statistical methods were widely available in order to find out the reliability indices from the test data. This method was also considered as black box testing which concentrate on available data and proper model was selected depends on the application. There were possibilities to analyze the data and generated model to extract enormous amount of information to characterize the performance parameters. Some of them include design of experiments, accelerated testing, regression analysis, etc. Even, there were several tools available for model selection, mathematical formulation and model analysis. This methodology has some advantages like time consuming, no need for manufacturer data and parameter analysis.

Therefore, applying complex statistical tools to vague scientific principles adds several parameters to the equations, leading to a higher level of complexity. In contrast, a scientific model should give a simple explanation for the instances and then generalize the model. Until now, the physics-of-failure approach was not able to make accurate predictions or replace traditional approaches.

The electronic system reliability approach is a method built upon the advantages of both traditional and physics-of-failure methodologies; this approach combines the device physics-of-failure mechanisms with the constant failure rate model and applies them to the electronic system, which provides both a physical explanation for the electronic system failures, and a simplified statistical tool for reliability prediction. However, these approaches can still (White 2008):

- Use traditional prediction tools in specific field studies to obtain an approximate numerosity.
- Update the previous models based on statistical methods (like the Bayesian approach) and try to calculate the uncertainty growth of the electronic systems.
- Unify electronic-device failure mechanisms.
- Try to apply the new scientific models to electronic systems.

The inclusion of multidisciplinary science and engineering approaches was very effective in solving of real life problems and our modified approach was combination of both physics of failure (deterministic) and statistical (probabilistic) approaches in Fig. 1. This advancement methodology first starts with the proper understanding of basic failure physics of the component and process the physics of failure methodology. This knowledge was fed to the statistical approach to further refining of data for accurate models. Finally, we get three faces of models; history and literature, white box and black box models and these were sent to decision support system. The other inputs to this system were life cycle costs and regulatory requirements.

2 Failure mechanisms at wafer level

Advanced integrated circuits (ICs) are very complex, both in terms of their design and in their usage of many dissimilar materials (semiconductors, insulators, metals, plastic molding compounds, etc.). For cost reductions per device and improved performance, scaling of device geometries has

Table 1 Comparisons of different reliability prediction models (MTBF Report 2005)

Reliability prediction model	Company	1 Watt DC–DC converter				100 W AC-DC PSU	
		25 °C		85 °C		40 °C	
		Hours	Years	Hours	Years	Hours	Years
MIL-HDBK-217F EXAR	A	31,596,574	3,606.9			686,771	78.4
MIL-HDBK-217F Notice2	B	832,000	95	86,000	9.8		
MIL-HDBK-217F Notice2	C	156,000	17.8	124,000	14.2		
Telcordia SR332 Parts count	D	89,380,000	10,203.2	29,260,000	3,340.2		
Telcordia SR332 Parts stress	D	104,200,000	11,895	57,160,000	6,525.1		
Siemens SN29500	A	80,978,217	9,244.1			1,554,055	177.4
HRD5 Parts Stress	B	2,465,000	281.1	849,000	96.9		
HRD4 Parts count	B	1,132,000	129.2	1,132,000	129.2		
MIL-HDBK-217F EXAR	A	31,596,574	3,606.9			686,771	78.4
Telcordia SR332 Parts count	E					1,418,000	16.2

played a critically important role in the success of semiconductors. This scaling—where device geometries are generally reduced by 0.7 × for each new technology node and tend to conform to Moore's Law—has caused the electric fields in the materials to rise (bringing the materials ever closer to their breakdown strength) and current densities in the metallization to rise causing electromigration (EM) concerns. The higher electric fields can accelerate reliability issues such as: time-dependent dielectric breakdown (TDDB), hot-carrier injection (HCI), and negative-bias temperature instability (NBTI). This failure mechanisms behave differently depends on the technology such as CMOS, BJT and other semiconductors, process, manufacturer etc. In addition, the use of dissimilar materials in a chip and in the assembly process produces a number of thermal expansion mismatches which can drive large thermomechanical stresses. These thermomechanical stresses can result in failure mechanisms such as stress migration (SM), creep, fatigue, cracking, delaminating interfaces, etc. Several of them are described below (White 2008; Ohring 1998; Panasonic Corporation 2000; Renesas Technology Corp 2008; JEDEC Publication 2008; MOSIS Technical notes; Semiconductor Device Reliability Failure Models 2000; Semiconductor Reliability Handbook 2011; SONY—Sony semiconductor quality and reliability handbook 2000; Joseph Bernstein et al. 2006; Foucher et al. 2002; Shahrzad Salemi et al. 2008; MTBF Report 2005).

The following failure mechanisms have possibility to appear at wafer level in device including all technologies. Certainty of occurrence of these failure mechanisms on particular device depends on stress factors, process, technology and application.

Failure Mechanisms:

1. Electro Migration (EM)
2. Temperature Dependence Die-electric Breakdown (TDDB)
3. Hot Carrier Injection (HCI)
4. Negative Bias Temperature Instability (Slow Trap)
5. Stress Migration
6. Soft Error (Radiation)
7. Corrosions
8. Surface Inversion
9. Reliability Problem of non-volatile memory
10. Thermal Fatigue (Cycling)

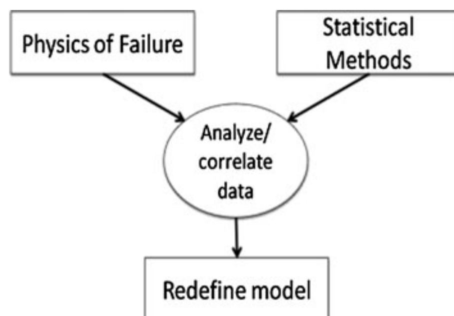

Fig. 1 Short idea of Modified approach

Scaling of devices is big advantage over the past technologies and apparently they found so many reliability issues which are so random at 45 nm technology. Out of the above list, there is a possibility that these failure mechanisms occurred at wafer level.

2.1 Electro migration (EM)

Failure occurs mainly due to the blocking (or voids) of interconnects through transport momentum at conductor-metal interface forming open-circuit failure mode. Also, atoms of one conductor pile up to another conductor cause short-circuit (hillock Failure or whisker failure). This mechanism happens predominantly at higher current density levels (>10^5 A/cm^2) and at higher temperatures. Activation energy, Ea has variable effect on Electro migration and it ranges between 0.5 and 0.8 eV. The following forms of EM are

i. Grain boundary diffusion on Al wires and surface diffusion in Cu wires.
ii. Thermal Effects: high power collide scattering joule heating.

Aluminum and Copper are the mostly used metals for contacts. Aluminum (Ea = 0.6 ± 0.1 eV) has good conductivity, good ohmic contacts and adherence to substrate where pure Copper is more robust (Jcu = 5JAl) to currents. Activation energy and mobility increases by adding 1 % palladium to metals. Electromigration causes due to increase in current density and mainly occurs in smaller grain boundaries. For a Bamboo structure; if, width is proportional to average grain size then the effect of electromigration decreases. For large magnitude currents, slotted wires are used to meet power requirements. Blech Length, the lower limit of length of interconnects at which electromigration is allowed, is used as design parameter. Solder joints made up of occurs at lower current densities. Electromigration is characterized using the time to failure model (Joseph Bernstein et al. 2006; Foucher et al. 2002), given below: Black's Equation,

$$MTTF = A(J^{-n})e^{(\frac{E_g}{KT})} \tag{2}$$

Where Ea = 0.5–0.8 eV, J is Current Density, K is Boltzman Constant, T is Temperature, $n = 2$, and A is Acceleration Factor.

The following are preventive methods for electromigration:

i. Adding 2–4 % of Cu increases resistance to EM by 50 times or adding W & Ti 0.95 eV

ii. Controlling the quality of wiring
iii. Smoothing of the process
iv. Prescribed current densities and enforcing rules on accelerated life testing

2.2 Temperature dependence die-electric breakdown (TDDB)

This mechanism occurs by continuously applying stress to Gate oxide film causing di-electric falling shorting anode and cathode (Panasonic Corporation 2000). This mechanism was also prominent while increasing/decreasing in electric field across the device. Time to failure increases with increasing electric field and temperature. But as electric field decreases, activation energy also increases which results in increase in internal stresses. For higher fields (>10 MV/cm), a mechanism called field enhanced thermal bond breakage is activated. The decrease in the activation energy also leads to electron reaction rate (Shahrzad Salemi et al. 2008).

2.2.1 E-Model

An electric field on oxide film causes injection of holes on anode side induces traps (Renesas Technology Corp 2008). Increase of traps leads to the formation of stress induced leakage current because of tunneling effect and further increase of these traps between gate and silicon substrate corresponds to increase in leakage current leads to gate oxide break down.

$$MTTF = Ax10^{-\beta \mathbf{E}} x e^{\left(\frac{Ea}{KT}\right)} \quad (3)$$

A, arbitrary scale factor, dependent upon materials and process; Eox, electric field across the dielectric in MV/cm; ß, Electric field intensity coefficient (cm/MV); K, Boltzman Constant; T, Temperature in K; Ea, $(\Delta H)_0$-a Eox; Ea, effective activation energy (eV); (ΔH)0, the enthalpy of activation for bond breakage in the absence of external E (~2.0 eV); a, effective molecular dipole-moment for the breaking bonds which value is ~7.2 eÅ.

2.2.2 1/E Model

This model is applicable for lower electric fields and current mechanism follows Fowler–Nordheim conduction. Electrons experience impact ionization at lower electric fields that damages the di-electric, which degrades further by accelerated field (MOSIS Technical notes). These accelerated electrons reaching anode produces hot holes which tunnel back to dielectric and this phenomena is known as hot hole injection mechanism (Semiconductor Device Reliability Failure Models 2000). 1/E Model:

$$TF = \tau_0(T) e^{\left(\frac{G(T)}{Eox}\right)} \quad (4)$$

Where τo(T), a temperature dependent prefactor, $\sim 1 \times 10^{-11}$ s; G, field acceleration parameter, ~350 MV/cm with a weak temperature dependence; Eox, electric field across the dielectric in MV/cm.

For ultra-thin oxides, Temp is non-Arrhenius,

$$MTTF = T_{BD0}(V) e\left(\frac{a(V)}{T} + \frac{b(V)}{T^2}\right) \quad (5)$$

2.3 Hot carrier injection

2.3.1 Hot carrier injection in CMOS

Charge carriers in high electric field are accelerated by gaining energy. Some charges have acquired hot energy and capable to overcome potential between Gate and Substrate. These carriers injected to Gate (some are trapped), form a space charge region, which results in change in threshold and transconductance. Injected carriers which are not trapped are drawn as gate current and other carriers are drawn as substrate current. Hot carrier Injection generated by these four mechanisms (Semiconductor Reliability Handbook 2011):

i. Drain Avalanche Hot Carrier DAHC injection Electrons from Source lead to impact ionization because of high electric field at Drain, which generates electron–hole pairs and has sufficient higher energy injected into Gate. Vgs = ½ Vds. This is the greatest factor at normal temperatures.
ii. Channel Hot Electron CHE injection (Vgs = Vds, lucky electrons which are not energy dissipation).
iii. Secondary generated hot electron SGHE injection.
iv. Substrate hot electron SHE injection.

Hot carrier injection is prominent at lower temperatures. Thermal vibrations of the charges increase and hence collisions decreases, thus have higher probability for mean free path of electrons to absorb more energy. Higher electric field injects carriers in the substrate thus increasing the probability of occurrence. The impact provides higher secondary electrons. As voltage of the source decreases, the impact of ionization modes depends on temperature.

The degradation by HCI is given by following equation

$$\Delta P = At^n \quad (6)$$

Where P, parameter gm; Vth, isat. The following models for n-channel and p-channel describes HCI failure mechanism.

n-channel, Eyring Model $MTTF = B(I_{sub})^{-N} e^{(Ea/KT)}$ (7)

p-channel $MTTF = B(I_{gate})^{-M} e^{(Eg/KT)}$ (8)

Where Igate is gate current, Isub is substrate current, Ea is activation energy, K is boltzman constant, T is absolute temperature and M,N and B are constants.

Substrate current and voltage in p-channel substrate doubles for each 0.5 V increase in voltage between source and drain (Semiconductor Device Reliability Failure Models 2000). The acceleration factor is thus given as

$$AF = e^{(B(1/Vdd - 1/Vdd,\max))} \quad (9)$$

The effect of HCI can be reduced by moderating electric field using lightly doped drain (LDD) structure with higher resistance at Drain and further reducing source voltage.

2.3.2 *Hot carrier injection in BJT*

HCI behaves differently to BJT technology. Berkeley (Hu 1989) simulated the circuit waveforms at arbitrary time in the future considering the hot-carrier degradation of the transistors in the circuit. The key physical model is the realization of transistor parameters are the functions of Age where

$$Age = \int \frac{I_{ds}}{WH} \left(\frac{I_{sub}}{I_{ds}}\right)^m dt \quad (10)$$

Where W is the transistor width, W and M are the functions of the oxide field, i.e., functions of Vgd, and are determined from dc transistor stress tests.

Under emitter–base reverse bias, a small reverse current, IR, flows through the junction due to band-to-band tunneling and impact ionization. These carriers apparently generate interface traps near the junction and introduce a component of non-ideal base forward current, ΔIB, which causes the current gain to decrease. It can be shown that

$$\Delta I_B = DJ_c^a \left(\int I_R^b dt\right)^c \quad (11)$$

This mechanism is not important in ECL circuits, where the base-emitter junctions do not experience revere bias stress. It is a potential factor in BICMOS circuits.

2.4 Negative bias temperature instability (NBTI)

The failure mode in NBTI is shift in threshold voltage; Vt. Holes are trapped between Si/SiO2 interfaces degrade the performance of device and happen mostly in PMOS. Holes are thermally activated and gains sufficient energy to disassociate Si/SiO2 defects near LDD. Concentration of holes increases with temperature rise. Due to NBTI, there is predominant degradation in Idsat and transconductance gm and off current. The increase in these currents leads to increase in Vth. Critical value of electric field is 6MV/cm and temperature from 25 to 100 °C.

Silicon dangling bond on interface inactivated by Hydrogen (Renesas Technology Corp 2008), Si–H, stress (high temperature), increase in bias, holes gives to electrothermal reaction, freeing Hydrogen atom. Silicon dangling bond becomes interface state and H diffuses in oxide film. Some diffusing Hydrogen joins with defects to form traps. Increase in interface state and charge resulting from traps in oxide for degrading Vth. Recovery can be done by removing stress bias and applying reverse bias. NBTI is predominant in circuits where DC stress is applied. Time to failure is found out using the following equation in Equation 12 (Renesas Technology Corp 2008).

$$MTTF = A10^{-\beta \mathbf{E}} e^{(\frac{Ea}{KT})} \quad (12)$$

Where MTTF: Time to Failure, A: Constant, E: Electric field intensity (MV/cm), k: Boltzmann constant, Ea: Activation energy (eV) 1 eV, β: Electric field intensity coefficient (cm/MV) 1 to 1.5

2.5 Stress migration

Metal atoms in wiring migrate due to stress (SONY—Sony semiconductor quality and reliability handbook 2000). Increase in temperature and difference in thermal expansion between materials causes increase in further. If it is beyond critical level, metal ions with thermal capabilities diffuse through grain boundaries and defects scattered in each grain boundary migrate creating voids. There are two types of causes of stress: intrinsic stress and molding method cause distortion in crystal lattice. Thermal stress produces with difference in coefficient of thermal expansion of different materials. Stress also depends on structure. At lower temperatures, disconnection of wire happens after long-term and at higher temperature (200 °C) for short-term wherever voids exhibit heat treatment. At lower temperatures, metal atom diffusion speed increases by increase in temperature, stress by insulating film and metal wiring are smaller. At higher temperatures, decrease in heat-treatment process and adjusting heating and cooling reduces migration.

Movement of metal atoms under stress-flux divergence results in voids. In metals, there is decrease in grain boundary diffusion only when grain size is less than line width. Stress Migration baking temperature (150–200 °C) at maximum creep rate leads to higher stress, lower mobility and lower temperature. Using of refractory metal barriers or layered metallization nullify voids.

Mechanical Stress Model:

$$MTTF = A_0 \sigma^{-n} e^{(Ea/KT)} \quad (13)$$

Thermo-mechanical Stress Model: σ α (ΔT)

$$MTTF = B_0(T_0 - T)^{-n} e^{(Ea/KT)} \tag{14}$$

Where σ,constant stress load; $n = 2–3$ for ductile metals; n is usually ∼5 if creep, thus T < Tm/2; T0, stress free temperature for metal and Ea = 0.5–0.6 eV for grain boundary diffusion; ∼1 eV for single grain (bamboo-like) diffusion.

2.6 Soft errors (Radiation)

Semiconductor memory defects recovered by rewriting data are called soft errors (SONY—Sony semiconductor quality and reliability handbook 2000). Source voltage, ground and α rays from Uranium and Thorium in packaging leads to degradation on materials. When α rays incident on silicon, electron and hole pairs are generated. Electric field causes holes to p-well and e- cluster in n diffusion area. Cluster electron node potential to drop. As Vs decreases, charge level accumulated at node, soft errors occur more easily.

The following precautions to be taken to reduce the effect of radiation:

i. Reducing level of α rays to penetrate; coating chip surface to attenuate,
ii. Difficult to e- makes cluster at nodes; less diffusion layer area or increase in substrate density,
iii. Increasing memory node Capacitance; decrease in insulating film thickness or adding Capacitance.

2.7 Corrosions

Corrosion failures can occur when ICs are exposed to moisture and contaminants (Semiconductor Device Reliability Failure Models 2000). IC corrosion failures are usually classified as one of two broad groups: bonding pad corrosion or internal-chip corrosion. The bonding pad is a rather large piece of on-chip metallization on the order of 50 μm × 50 μm. These bonding pads, historically, have provided the metallization contact surface for eventual Au or Cu-wire ball bonding. Internal corrosion (internal to the chip, away from the bonding pads) can also occur if some weakness or damage exists in the die passivation layer which could permit moisture and contaminants (e.g., chlorides) to reach the exposed metallization. The internal corrosion can cause electrical discontinuities at localized regions of die (McPherson 2010). Corrosion can be generally described in terms of a corrosion cell.

The corrosion cell must have four key components in order for corrosion to occur: an anode (a region for the oxidation reaction to occur), a cathode (a region for the reduction reaction to occur), an electrolyte (through which the ions can diffuse), and a conductor to provide a pathway for the electron flow from the oxidation region to reduction region.

Aluminium with Copper and Silicon increases corrosion failures. Bonding pad: die passivation does not cover metallization. Internal: damage in die passivation leads to moisture to reach metal. Standards for testing are 85/85 (Temperature & Humidity), Autoclave (2 atm absolute pressure) and HAST (85 %RH, steam pressure > ambient pressure).

There are several models demonstrated here which depends on applicability.

2.7.1 *Experimental reciprocal method*

The time-to-failure equation for IC failure due to corrosion is

$$TF = A_0 e^{\left(\frac{b}{RH}\right)} e^{\left(\frac{Q}{K_B T}\right)} \tag{15}$$

Where A0 is a process/material dependent parameter and serves to produce a distribution of times-to-failure (Weibull or lognormal distributions), b is the reciprocal humidity dependence parameter (approximately equal ∼300 %), RH is the relative humidity expressed as a 3 % and

Q is the activation energy (approximately equal to 0.3 eV for phosphoric acid induced corrosion of aluminum and generally consistent with wet corrosion.

This model was developed when phosphosilicate glass (PSG) was used for interconnect dielectric and/or passivation.

2.7.2 *Power law humidity model*

The time-to-failure equation for IC failure due to corrosion is

$$TF = A_0 (RH)^{-n} e^{\left(\frac{Q}{K_B T}\right)} \tag{16}$$

where n is the power-law exponent and equal to 2.7, RH = % relative humidity, and Q is the activation energy and equal to 0.7–0.8 eV for chloride-induced corrosion of aluminum.

This model was developed for chloride-induced corrosion in plastic-packaged chips. Cl-based dry etches are generally used for the aluminum-alloy metallization. If excessive amounts of chlorides are left on the die after post-etch cleanups, corrosion can occur with the addition of moisture.

2.7.3 *Exponential humidity model*

The time-to-failure equation for IC failure due to corrosion is

$$TF = A_0 e^{(-a.RH)} e^{\left(\frac{Q}{K_B T}\right)} \tag{17}$$

where a is humidity acceleration parameter and is equal to 0.10–0.15 (%RH) -1, RH is the % relative humidity, and Q is the activation energy and is equal to 0.7–0.8 eV for chloride-induced corrosion of aluminum in plastic packages. This corrosion model was developed when it was shown that, over a wide range of humidity (20–80 %), the surface conductivity is exponentially dependent on the humidity.

2.7.4 *Exponential humidity-voltage model*

The time-to-failure equation for IC failure due to corrosion is

$$TF = A_0 RH^{-N} f(V) e^{\left(\frac{Q}{K_B T}\right)} \quad (18)$$

Where A0, arbitrary scale factor; N, ~2.7; Ea, 0.7–0.8 eV (appropriate for aluminum corrosion with chlorides are present) and f(V) = an unknown function of applied voltage.

Originally used for Al corrosion, but applied to other failure mechanisms with different N & Ea values. From all these models, the power-law model is a widely used corrosion model in the IC industry for plastic-package chips.

2.8 Surface inversion

Mobile ions contaminate over time and accumulation causes drifts the ions at the interface (Semiconductor Device Reliability Failure Models 2000). Impure ions like sodium and potassium increase mobility of ions. Eventually at the Gate, there is a drift of charge carriers from poly anode to silicon substrate cathode. Positive ions at interface invert the surface and severely degrade oxide isolation. Ionic drift in SiO2 gate dielectric cause premature TDDB. Devices isolation leakage failures recover at unbiased temperature bake causes redistribution. It happens at E = 0.5 MV/cm and temperature at 100 °C.

2.9 Reliability problem of non-volatile memory

Electrons isolated from floating gate gain sufficient thermal energy to overcome energy barrier of surrounding oxide film (Renesas Technology Corp 2008). Designing of higher energy barrier leads to better quality.

Thermal excitation:

$$\frac{Vcc(t)}{Vcc(0)} = \frac{N(t)}{N(0)} = e^{\left[-vte^{(-Ea/KT)}\right]} \quad (19)$$

Data retention in memories happens generally at 10 years at room temperature. Degradation happens due to (Renesas Technology Corp 2008)

(a) Charge loss/gain due to initial effect in oxide; leakage path or particles
(b) Ionic contamination;
(c) Excessive electrical stress
(d) Stress from too many writes/erasures.

If there is a defect in interlayer film and no failure in erased state, then there is a failure in written state due to loss of electrons in floating gate (JEDEC Publication 2008). Failure occurs in both modes with less time and higher temperature. To prevent these failures, baking temperature at manufacture is to be raised. Intrinsic degradation leads to repeated cycles of Read/Write. Electrons trapped in oxide results in reduce in threshold voltage of 0/1 states.

2.10 Thermal fatigue

Fatigue failures can occur in ULSI devices due to temperature cycling and thermal shock (JEDEC Publication 2008; Semiconductor Device Reliability Failure Models 2000; McPherson 2010). Permanent damage accumulates during thermal cycling or temperature shock. Damage from thermal cycling can also accumulate each time the device undergoes a normal power-up and power-down cycle. Such cycles can induce a cyclical stress that tends to weaken materials, and may cause a number of different types of failures (MIL-HDBK-217F), including

- Dielectric/thin-film cracking.
- Lifted bonds.
- Fractured/broken bond wires.
- Solder fatigue (joint/bump/ball).
- Cracked die.
- Lifted die.

2.10.1 *Coffin-Manson model*

For ductile materials, low-cycle fatigue data are described well by the Coffin-Manson equation:

$$N_f = C_0(\Delta T - \Delta T_0)^{-q} N_f = A_0[1/\Delta\varepsilon_\rho]^B \quad (20)$$

Low cycle fatigue is defined as a stress condition in which some hundreds or thousands of cycles cause failure, while high cycle fatigue would require millions of cycles. The Coffin-Manson model was originally developed for ductile materials (iron and aluminum alloys for aircraft), but has been successfully applied to brittle materials also under all stress conditions.

2.10.2 *Modified Coffin-Mansion model*

$$\Delta\varepsilon_\rho \propto (\Delta T - \Delta T_0)^\beta \quad (21)$$

The Coffin-Manson equation works well, even for brittle material failures, where failure is dominated by crack initiation and growth, rather than simple plastic deformation.

During a temperature cycle, not all of the stress (temperature range, ΔT) may be inducing plastic deformation. If a portion of te cycle, $\Delta T0$, is actually elastic, then the elastic portion should be subtracted from the total strain range.

3 Modified physics of failure approach

Initially, the component was described thoroughly to get enough failure information. First need to check whether that component was existed in the field, and if it's available similar item analysis and if failures were present an extensive methodology was carried out and correspondingly failure analysis, failure mechanism and failure modeling was implemented to get an idea of the component. We need also to check whether the component was analyzed in the literature that information was also stored. After an extensive research and inputs from the similar and failure analysis, a detailed methodology needs to be planned in the sequential order of failure modeling, experimentation, simulations and statistical and data modeling. According to the plan, everything was executed simultaneously to reduce the amount of time in testing. After getting the data, several analyses of factors was conducted and modeling was developed from various methods. The essential information from all the blocks were given as inputs to the decision support system where it provides the best alternative was selected and considered as technique for reliability growth. This information was stored in the component database where it was useful for further analysis. The modified physics of failure will be implemented as in Fig. 2.

3.1 Component description

As informed above, this analysis requires as much as information for the pre- and post processing examination. Hence, the component was collected from the various data and sources are essential in building up data (MIL-HDBK-338B). The resources required for data part are:

i. Materials used for fabrication and its properties.
ii. Diagrams for layout of internal chip structure.
iii. Various stresses effecting at the field and its performance.
iv. Architecture used for design.
v. Processes carried out during the fabrication.
vi. Design of the circuitry.
vii. and technology implemented for fabrication.

The resources required for data part are:

i. Manufacturer of the product/item.
ii. Consumer data supplied.
iii. Similar items that was earlier carried out in house.
iv. Manuals for that component.
v. Field information.
vi. And design team for information.

3.2 Literature and History Data

As for the failure study, learning the literature was necessary for understanding the behavior of the component under the failure considerations (MIL-HDBK-338B). The aspects need to be considered in literature are:

i. Stress parameters in and off the field.
ii. Reliability growth techniques available.
iii. Testing information and setup.
iv. Possible failure point locations (weak areas).
v. Failure modeling methods and techniques and failure criteria.
vi. Failure analysis using sophisticated equipments.
vii. Failure mechanisms that effect the behavior of performance parameters.
viii. Operational life cycle of the component.

The aspects to be considered were provided as:

i. Field information.
ii. Prediction of life using MilHdbk and other standard handbooks.
iii. Reliability indices to be considered.
iv. Datasheets from the manufacturer.
v. Failure data provided in the research.

3.3 Similar item analysis

Several techniques have been developed and used in performing very early predictions of item reliability before any characteristics of the system design have been established (MIL-HDBK-338B).

i. Defining the new item.
ii. Identifying an existing item with nearly comparison.
iii. Obtaining and analyzing historical data.
iv. Drawing conclusions on the level of reliability.

Major factors for a direct comparison of similar items should include: Item physical and performance comparison, design similarity, manufacturing similarity, similarity of the service use profile, program and project similarity and proof of reliability achievement.

3.4 Reliability indices

There are several indices are present to define reliability of the component. They are time to failure, failure rate, percentage of degradation and probability. An appropriate parameter was selected by limiting with the failure criteria of the component. It comes under one of the parameters in the design considerations.

3.5 Failure analysis

Failure analysis consists of confirming reported failures and clarifying failure modes or mechanisms using electrical measurements and various scientific analysis technologies. This section introduces specific failure analysis methods. However, before performing the actual analysis work it is necessary to thoroughly investigate failure circumstances and accurately understand the failure contents. This makes it possible to determine the optimum analysis methods and carry out swift processing.

As semiconductor devices become more highly integrated and incorporate more advanced functions, manufacturing processes are becoming more miniaturized and complex, and include diverse reliability factors. In addition, semiconductor devices have come to be used over an extremely wide range of fields, so failure causes and mechanisms are also complex. Under these circumstances, an extremely high reliability level is required of semiconductor devices. Reliability must be built in from the device development stage to the manufacturing stage in order to ensure a high level of reliability.

There are several destructive and non-destructive sophisticated methods are available at several handbooks and simulations in order to characterize the device at various levels, to implement failure analysis and also to find failure point location (MIL-HDBK-217F; White 2008; Panasonic Corporation 2000; Perry Martin 1999). This is the comprehensive list of several non destructive failure analysis techniques applicable for each failure mechanism.

- Hot carrier injection: hot spot: photo emission analysis, thermal analysis, SEM, Liquid Crystal method.
- TDDB: oscilloscope for detection of breakdown voltage.
- Electromigration: Electron Probe Micro analysis.
- To quantify the internal Image: Image Analyzing System.
- Temperature and heat related failures: Thermal Analysis System.
- Impurities like S, P, F, Cl, Br and I: X-Ray Fluorescence Spectrometer and also FTIR.
- Corrosion: Time of flight secondary ion mass spectrometer.
- ESD: Optical beam induced current analysis (OBIC), TEM, Optical Microscope, SEM.
- Latchup: Optical beam induced current analysis (OBIC).
- For Electric Measurements: IC Tester, Oscilloscope and Curve Tracer.
- Surface Analysis: Transmission Electron Microscope (TEM).

3.6 Failure mechanisms

Advanced integrated circuits (ICs) are very complex, both in terms of their design and in their usage of many dissimilar materials (semiconductors, insulators, metals, plastic molding compounds, etc.). For cost reductions per device and improved performance, scaling of device geometries has played a critically important role in the success of semiconductors. This scaling—where device geometries are generally reduced by 0.7 $\times$ for each new technology node and tend to conform to Moore's Law—has caused the electric fields in the materials to rise (bringing the materials ever closer to their breakdown strength) and current densities in the metallization to rise causing electromigration (EM) concerns. The higher electric fields can accelerate reliability issues such as: time-dependent dielectric breakdown (TDDB), hot-carrier injection (HCI), and negative-bias temperature instability (NBTI). This failure mechanisms behave differently depends on the technology such as CMOS, BJT and other semiconductors, process, manufacturer etc. (MIL-HDBK-217F; White 2008; Panasonic Corporation 2000). In addition, the use of dissimilar materials in a chip and in the assembly process produces a number of thermal expansion mismatches which can drive large thermo-mechanical stresses. These thermo-mechanical stresses can result in failure mechanisms such as stress migration (SM), creep, fatigue, cracking, delaminating interfaces, etc. (Renesas Technology Corp 2008; JEDEC Publication 2008; MOSIS Technical notes).

3.7 Failure modeling

In order to predict the life time of the component, an appropriate model was designed or developed or selected which depends on the data generated from the experimental and simulation results. Apart from the standard physics of failure models, several models that were generated from the statistical results were also compared to define behavior of the stress and performance parameters (JEDEC Publication 2008; MOSIS Technical notes; McPherson 2010). As mentioned in Fig. 3, the model depends on the field and testing data, failure mechanisms and modes, stress parameters involved and by reference as failure criteria; it can be compared with the existing models.

3.8 Design of experiments

This technique was well established technique to find the variability of the input stress parameters and its effect on the performance parameter. Design of Experiments (DOE) techniques enables the designers and fabrication engineers to determine simultaneously the individual and interactive effects of many stress factors with respective levels that could affect the output results in any design (Condra 2001). DOE also provides a full insight of interaction between parameters and thus efficient in converting standard design into a robust one. DOE helps to make concentrate on the sensitive stress-levels and sensitive areas in designs that

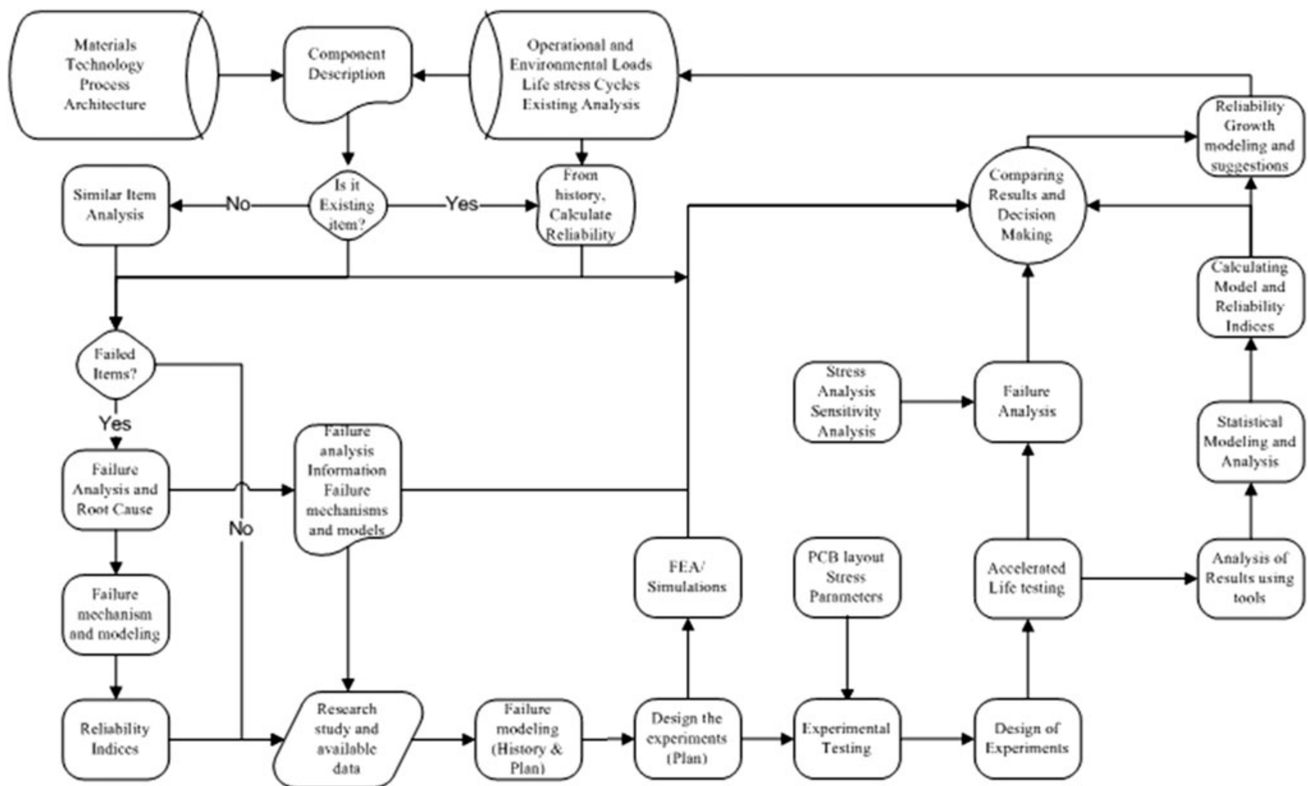

Fig. 2 Advanced block diagram of proposed physics of failure approach

cause problems in degradation, best performance and yield. Designers are then capable to reconfigure these parameters to reduce problems and correspondingly produce robust and higher designs before production. Design of experiments (DOE) is the design of any information-gathering exercises where variation is present, whether under the full control of the experimenter or not. Stress factors, levels and their interactions are tabulated for response curve and provides and runs that will best and worst solutions. In standard procedure, Taguchi method was implemented by considering the stress factors with levels with some number of runs. In general, there was a risk in selecting in levels of parameters.

In our work, we modified the conventional DOE into two steps: screening step and testing step. Initially appropriate samples were selected for each stage for repeatability and accuracy. The first step demonstrates the observance of input stress parameters on the output parameter. The response curve generated from this step provides the increase/decrease of respective stress parameter results in the degradation of performance output parameter. Then in accordingly the worst levels of the stress was selected for second testing step in constraints with the datasheet of the component. In the testing step, the experiments were conducted from the inputs of step 1. By this methodology, the ambiguity and risk in the selecting the stress levels was eliminated.

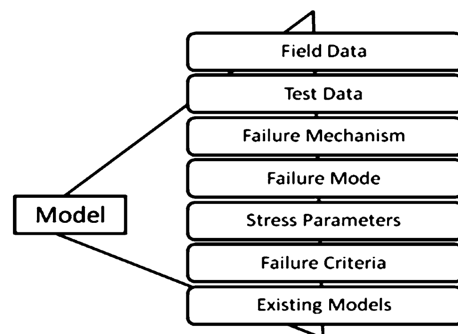

Fig. 3 Model dependence parameters

3.9 PCB design and layout

In order the experiment the electronic component, an appropriate circuit was designed and fabricated using Printed Circuit Board. There were several tools available to design the circuitry to compatible with PCB. The board layout was properly designed to reduce the interspatial effects, size and interoperability. As the experiment was needed to be exposed under stressed accelerated testing, the

circuitry need to be designed in such a way that the component under stress was segregated with the other control and power circuitry. This technique helps to reduce the effect the trace changes of other components such as resistor, capacitor and other miscellaneous components on the measured parameters as this components may vary their parameters in according with stress.

3.10 Experimental testing

After developing the circuit, the items were subjected to the stresses and monitor the output variables using various instruments. The experimental setup consists of various instruments such as voltage suppliers, oscilloscopes, voltage and current meters etc. ("EIAJ ED-4701 semiconductor device environment and durability testing methods" 1994). Accordingly, it was properly maintained in controlled environments to reduce the external noises. As it was needed to be subjected to the accelerated testing, the experiment stage needs to be properly monitored periodically for the effective control. The following stress parameters are temperature, voltage, current, radiation exposure etc. The planned Design of Experiments was subsequently applied on this circuitry to find the results.

3.11 Simulations

The simulation tools present a virtual environment and also gather information of the respective dimensions by graphical illustration (MIL-HDBK-217F). Simulations are carried out using advanced softwares tools such as Cadence, SPICE, etc. by providing inputs of stress parameters, device parameters and limits. This step will run simultaneously with the experimental testing for purpose of comparison with results from experimentation. Finite Element Analysis tools such as Ansys, Comsol, nanoHUB etc. are also carried to study the behavior of device and material characteristics.

3.12 Accelerated testing

In normal operating conditions, the component takes more amount of time to degrade and subsequently results in failure. In order to speed up the testing time, the applied parameters need to be stressed and correspondingly the testing time was reduced (Wayne Nelson 2004). Then using extrapolation and considering the acceleration factor, the failure time at operating conditions was calculated. Hence, accelerated life testing involves acceleration of failures with the single purpose of quantification of the life characteristics of the product at normal use conditions. In the most of the electronic components, the failure time was quite high and hence more rigorous stress levels need to be considered. Accelerating factors and stressed applied, either singly or in combination, include

i. More frequent power cycling.
ii. Higher vibration levels.
iii. High humidity.
iv. More severe temperature cycling.
v. Higher temperatures.

Most common model for temperature is Arrhenius model

$$AF = e^{\frac{Ea}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)} \quad t_f = Ae^{\frac{E_a}{kT}} \tag{22}$$

where AF, acceleration factor; Ea, activation energy; k, Boltzmann constant; T1, T2, operating and stress temperatures; tf, TTF.

From the normal and operating temperatures, acceleration factor was calculated by substituting this value, time to failure was calculated.

3.13 Analysis of results

The data generated from both experimentation and simulation was fed to this step. This step involves the behavior study of input stress parameters, design parameters, model parameters with respect to the performance and failure criteria. Individual graphs were also drawn to make some conclusions on the performance. It's like pre-processing stage to characterize the interdependence of the variables and observe the phenomenon of the imminent illustrations. The results were properly analyzed using some of the advanced statistical methods and tools to acquire essential information for further processing.

3.14 Stress and sensitivity analysis

This is pre-processing step for failure analysis which provides the affect of stress inputs on the variability of material characteristics using simulations and sensitivity data. This analysis is sub-section of failure analysis in which after acquiring information from the non-destructive testing techniques and simulation data, each and every stress parameter was demonstrated using contour graphs and 3D modeling information. This analysis provides parameters affecting the performance of the component. The sensitivity part provides the interaction between variability of each stress with the output variable.

3.15 Statistical modeling and data analysis

The preprocessing data was applied in this stage to qualify and quantify the data to assess the information. Using some of the statistical methods such as regression, response

surface regression, parametric analysis, DOE, quality methods, reliability/survival analysis, accelerated life testing, and support vector machine and other techniques to model the input–output interactions by illustrating the several graphical analysis were generated. This extensive examination of the parameters provides enormous amount of information at which we can judge the performance of the component. The models generated in the stage were considered as basis for the next steps as it decides the reliability growth techniques. The consideration and analyis the physics of failure models was also taken into account and further modify these models in accordance to the customized design.

3.16 Reliability indices

From the selected reliability indices at the planning stage, these figures were calculated using developed models such as Physics of Failure, MilHdbk standard handbooks, Response Surface Regression, other regression techniques and support vector machine. All these figures need to be calculated in consideration with the failure criteria. These figures were further compared in a common platform to assess the variability and degradation of the performance parameters with the operating conditions. The outputs of this stage are reliability indices, design range and metrics, safety limits and best parameters for maximum performance.

3.17 Reliability growth

The final objective of this overall methodology is to find the best design and manufacture alternatives to increase the life time of the component. The techniques required for enhancement in TTF and reduction in degradation of parameters is called reliability growth (Chary et al. 2012). This step provides only the prediction so such that uncertainty and confidence levels were also included. The possible reliability growth techniques cover in

i. Changes in design parameters.
ii. Incorporation of additional circuitry.
iii. Selection of different manufacturer.
iv. Failure site improvement.
v. Fabrication suggestions to manufacture for in-house components.

3.18 Non-technical factors

In deciding the optimal characteristics of the component, several other factors need to be considered at the managerial level. These include risk analysis, government policies, management choices, availability, life cycle cost, human interaction etc. to be considered.

3.19 Decision support system

This is the final stage of the entire proposed modified block diagram which involves much more productive decision can be made by the information gathered from different parts of the Fig 4. The following figure demonstrates the various factors required as an inputs to the decision support system to finalize the judgment on the component for reliability growth and further to take necessary measures. The inputs to the system are:

(a) Failure AnalysisFrom acquiring the information of failure point locations at different parts of the block diagram, such as similar item analysis, tested failure analysis, in the literature and from historical data, a final conclusion needs to be stated as input to the support system. This was considered as quality input.
(b) Statistical ModelsModels were generated at different parts of the diagram such as in the literature, historical data, failed items and the tested data. An appropriate prediction model was selected for quantitative analysis and thus decisive finding was fed to system.
(c) SimulationsSimultaneously we carried out simulations on the component to identify the stress behavior on the performance parameters and any other essential information was provided to the central system.
(d) RiskThe possible risk associated with each alternative was considered as input.
(e) Life Cycle CostAs cost was one of the main criteria for a business, total cost accumulated for each alternative was considered.
(f) Non-technical factorsOther non-technical factors were also discussed.

An expert group consists of reliability engineers, electronic design and fabrication engineers, material engineers, statisticians, field engineers and management need to be discussed on the several alternatives and appropriate solution was to be selected by optimal suggestions from all the people in the group. Each alternative was excessively discussed and generates report considering all the factors and this information will feed back to the database of the component in which this information is useful in further analysis.

4 Predicted outcomes

By implementing this advanced methodology, the following productive outcomes provides efficient information as

- Root cause analysis provides the exact failure site location which provides pin pointed improvement area.
- Suggesting different alternatives for the enhancement in reliability.

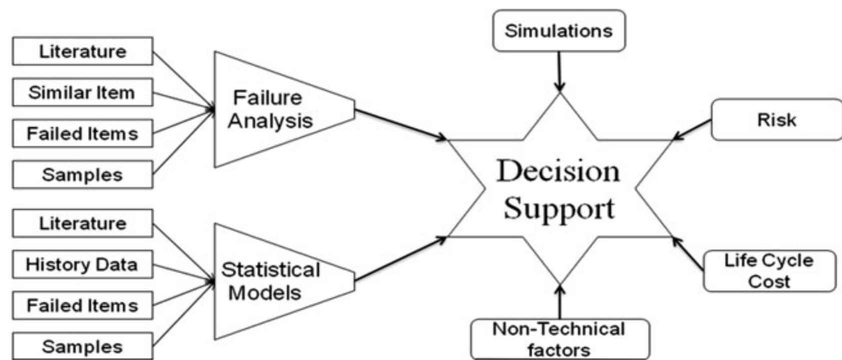

Fig. 4 Decision Support System

- Reduction in the repair/recall/replacement cost.
- Feasible for flexible reliability design using the data w.r.t the application.
- Also available for similar item analysis.

4.1 Advantages

The advantages by using this methodology are

- Proper learning of failures so that future product development, design, strategy and implementation will be more successful.
- Reputation in market due to reliable product outcomes.
- Cost, time and human work for recalling, repairing and replacement decreases.
- Qualitative and quantitative data is available for the selected component and consider as a basis for advance in design with less time.
- Modeling the component as per requirement and provides in-house research.
- Increase in time to market depends on supply of products.

4.2 Challenges

This methodology has following challenges and limitations

- Materials, process and technologies are always not available to the customer datasheet by companies due to confidentiality.
- Requires more sophisticated instruments (also cost) for analysis which are always not possible.
- Modeling of the failure criteria/degradation phenomena of new materials needs insightful research.
- It takes time to carry out and require cost for all analysis.
- Need expert reviews on the cause of failure.

5 Conclusion

Physics of failure methodology alone does not provide enough information on the component and hence incorporation of statistical methods will improve the effectiveness of the prediction of the reliability indices. The proposed modified approach accommodates enormous amount of information which also provides several other alternatives which improves the mechanism. But this method is only applicable to the critical parts and components which is very important and provide safety to the costly equipment. This type of rigorous analysis does not require for less important components.

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