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Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

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Acting Director of the United States Patent and Trademark Office

(12) **United States Patent**
Chen

(10) **Patent No.: US 8,502,323 B2**
(45) **Date of Patent: Aug. 6, 2013**

(54) **RELIABLE NORMALLY-OFF III-NITRIDE ACTIVE DEVICE STRUCTURES, AND RELATED METHODS AND SYSTEMS**

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H01L 21/20 (2006.01)

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USPC **257/392**; 257/E27.061; 257/E21.631

(58) **Field of Classification Search**
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See application file for complete search history.

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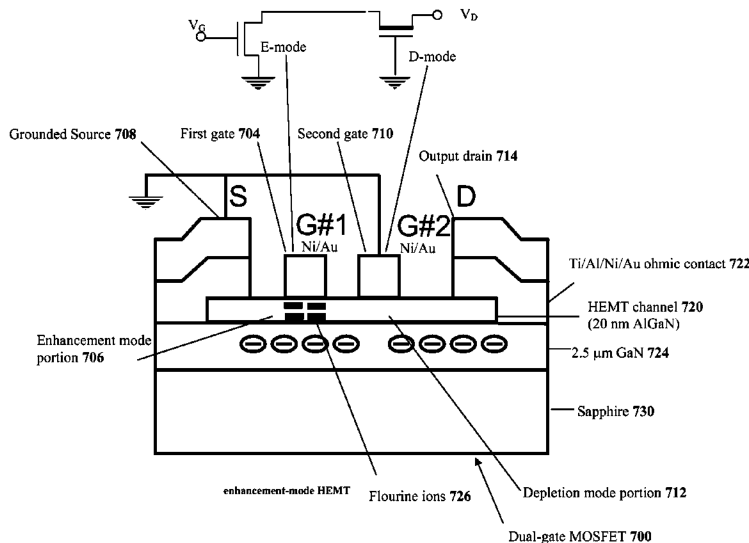
(57) **ABSTRACT**

A field-effect transistor includes a first gate, a second gate held at a substantially fixed potential in a cascode configuration, and a semiconductor channel. The semiconductor channel has an enhancement mode portion and a depletion mode portion. The enhancement mode portion is gated to be turned on and off by the first gate, and has been modified to operate in enhancement mode. The depletion mode portion is gated by the second gate, and has been modified to operate in depletion mode and that is operative to shield the first gate from voltage stress.

8 Claims, 10 Drawing Sheets



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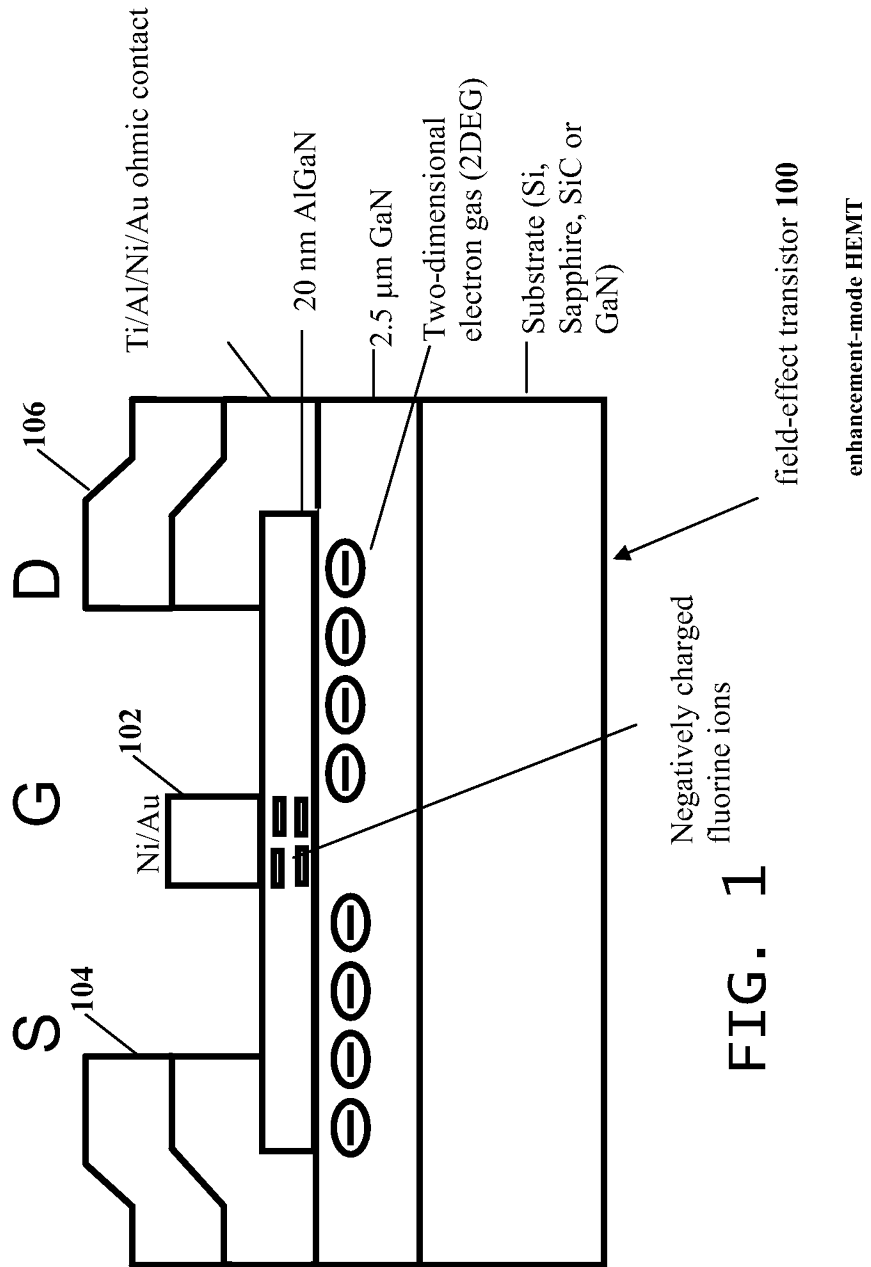


FIG. 1

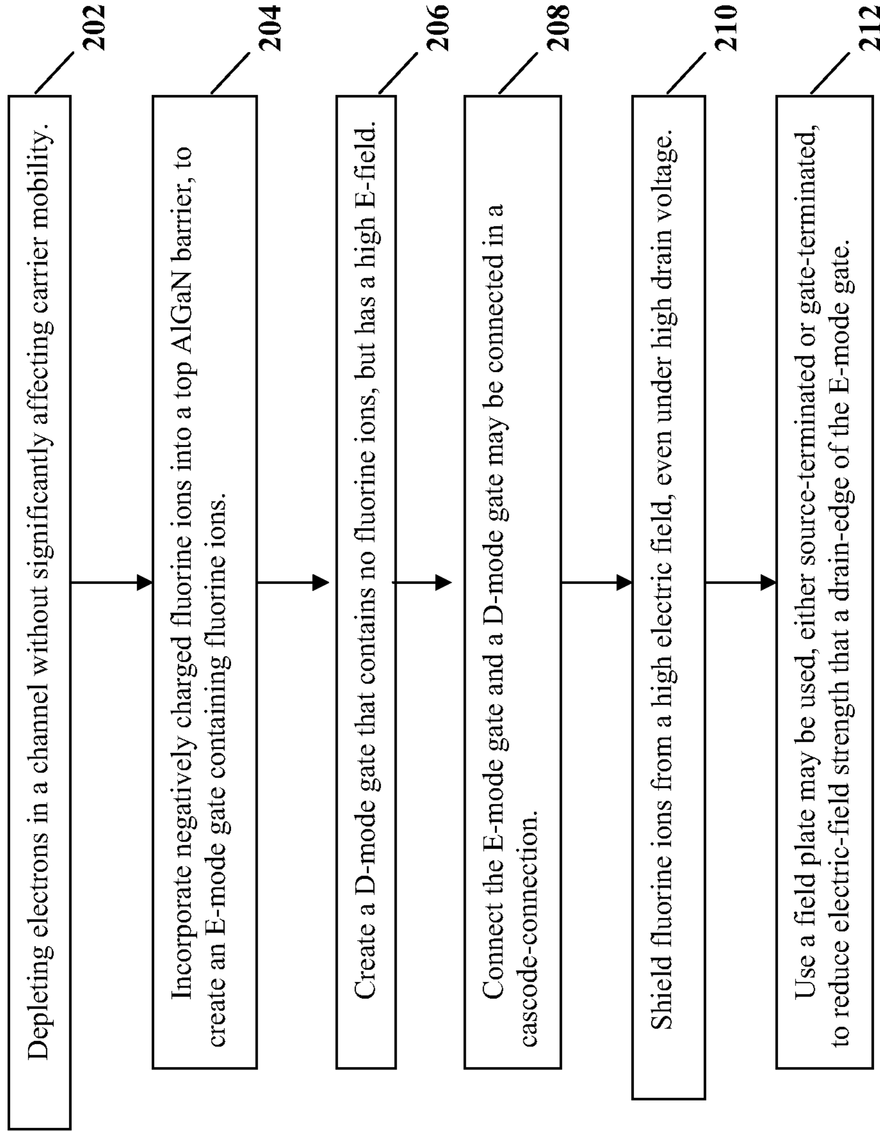


FIG. 2

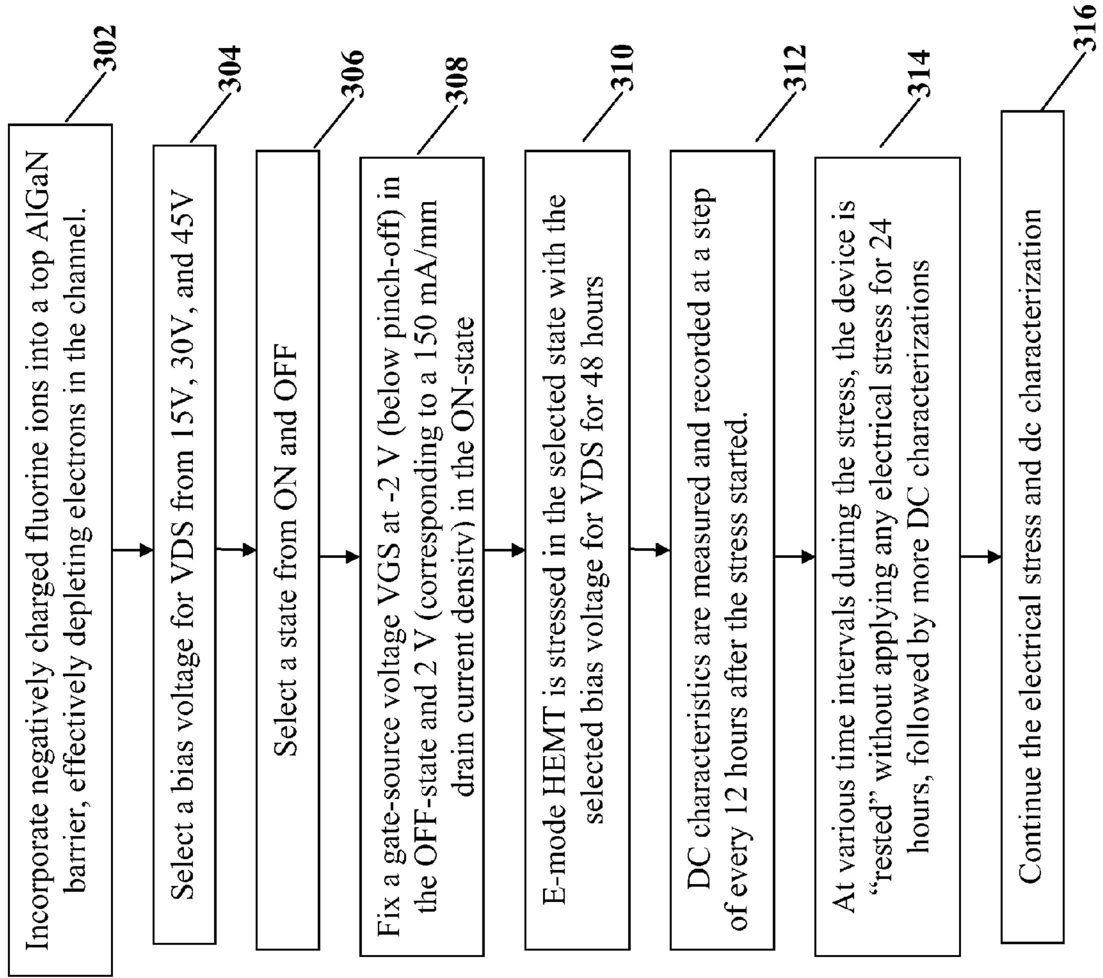


FIG. 3

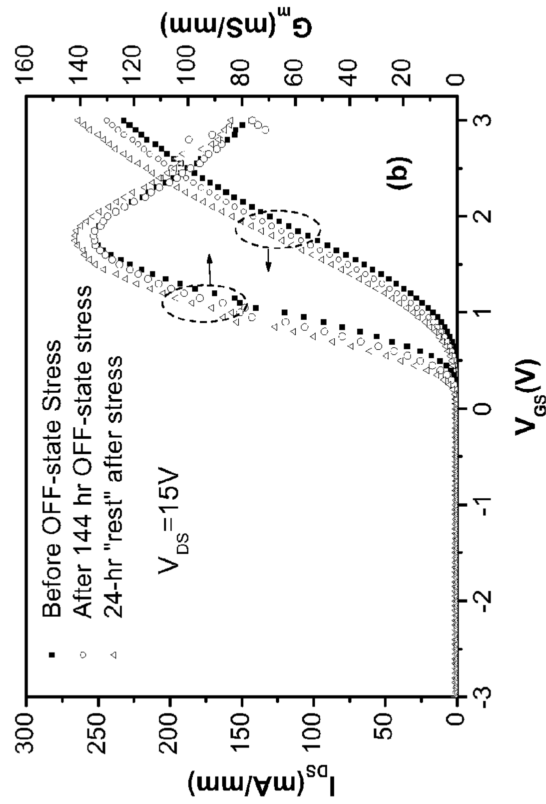


FIG. 4b

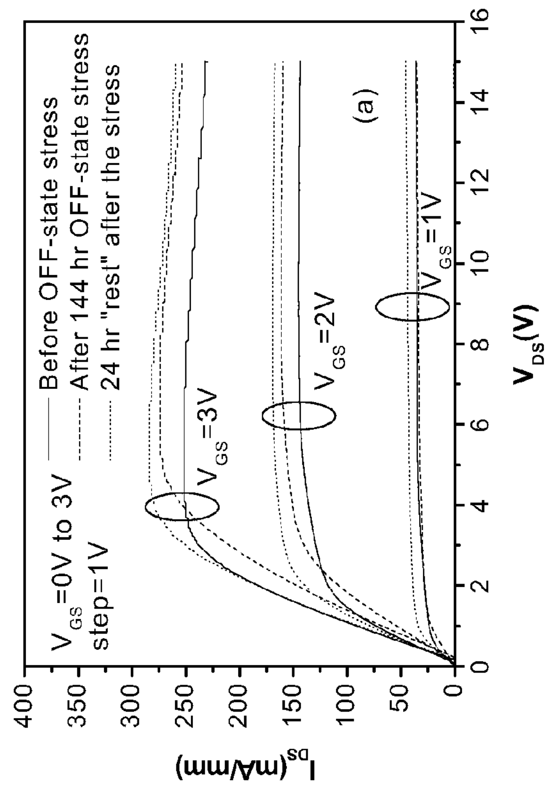


FIG. 4a

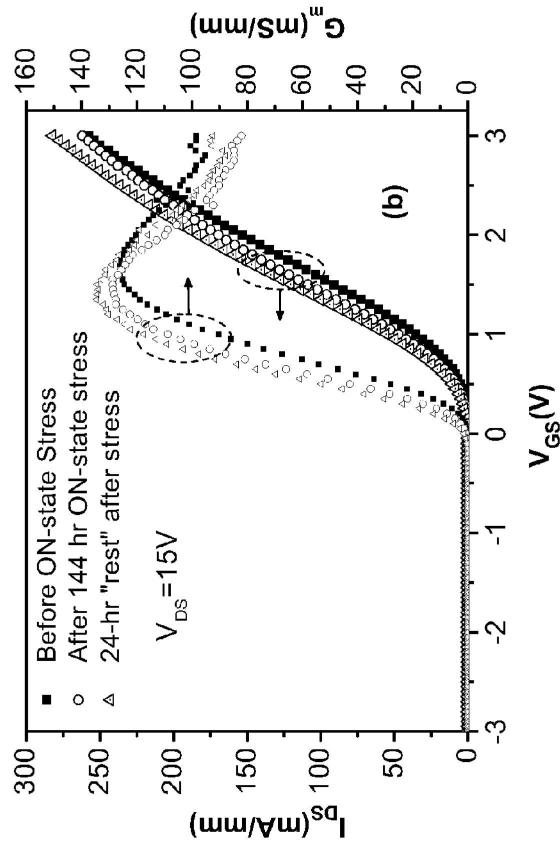


FIG. 5b

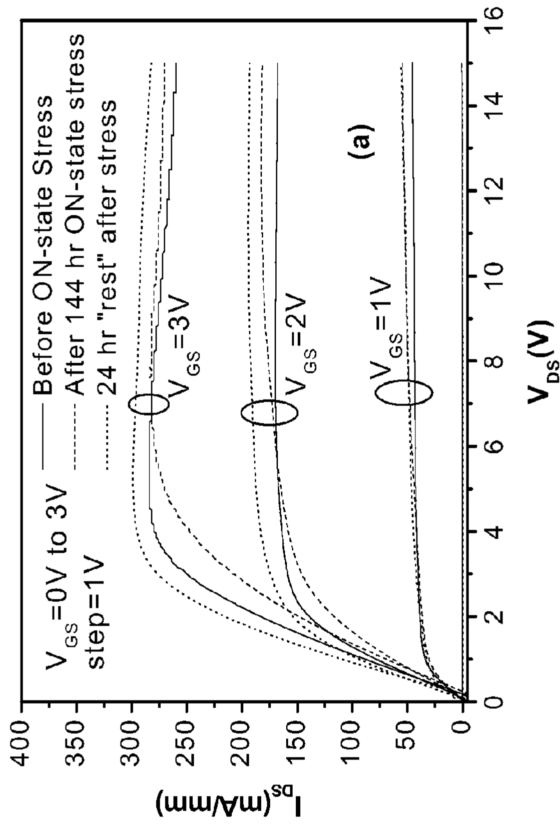


FIG. 5a

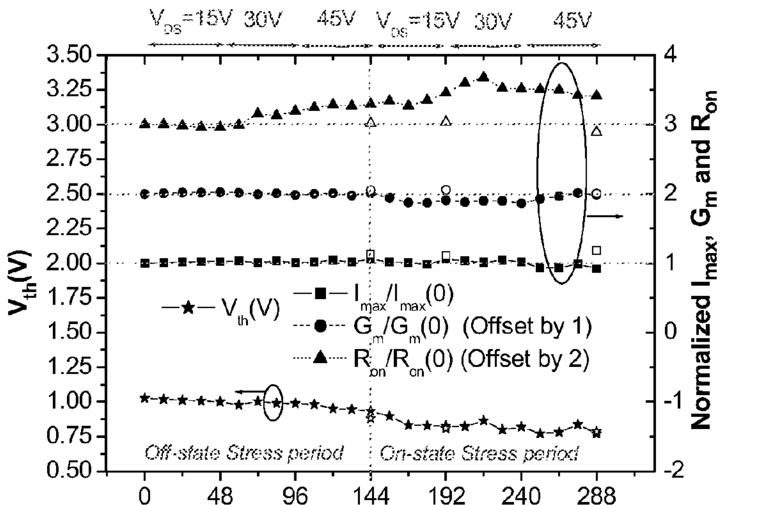
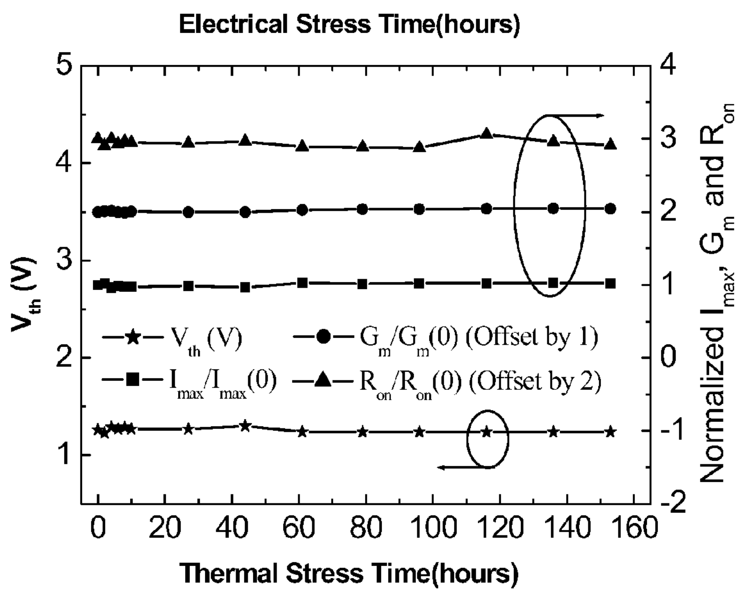


FIG. 6a



DC characteristics (V_{th}, I_{max}, G_m and R_{on}) as a function of thermal stress time. Stress temperature is 350 °C. The measurement is conducted at room temperature after the sample is cooled down at various time of the entire stress process.

FIG. 6b

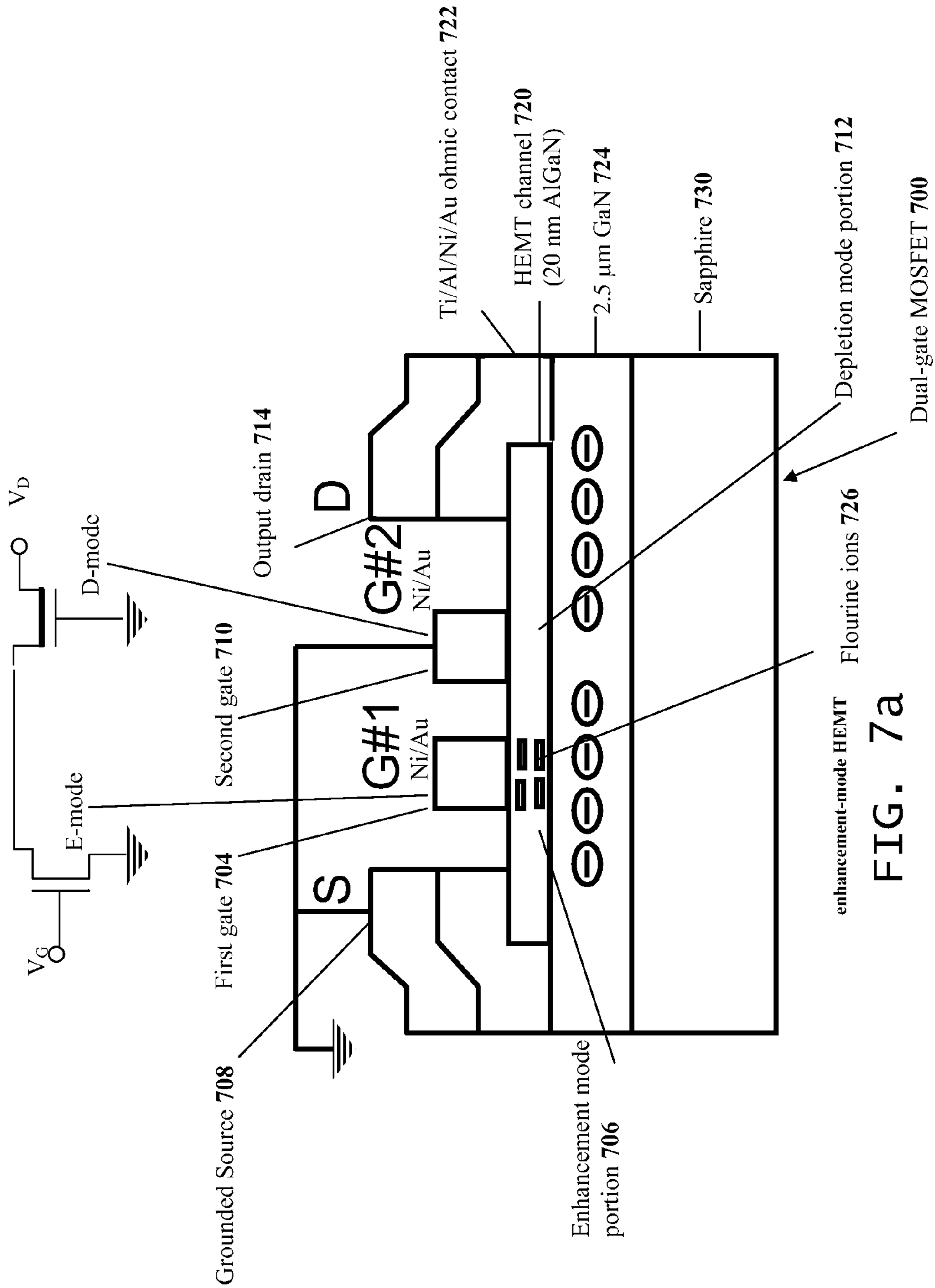
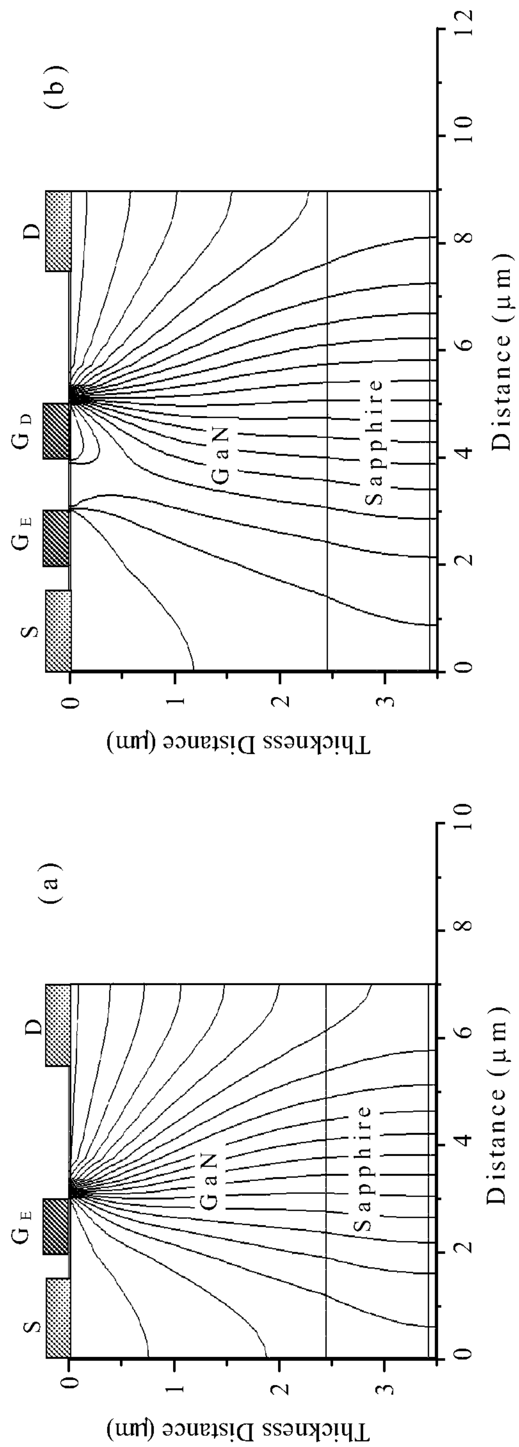


FIG. 7a



Equal-potential lines in OFF-state (a) single-gate and (b) dual-gate E-mode HEMTs. V_{DS} is 50 V.

FIG. 7b

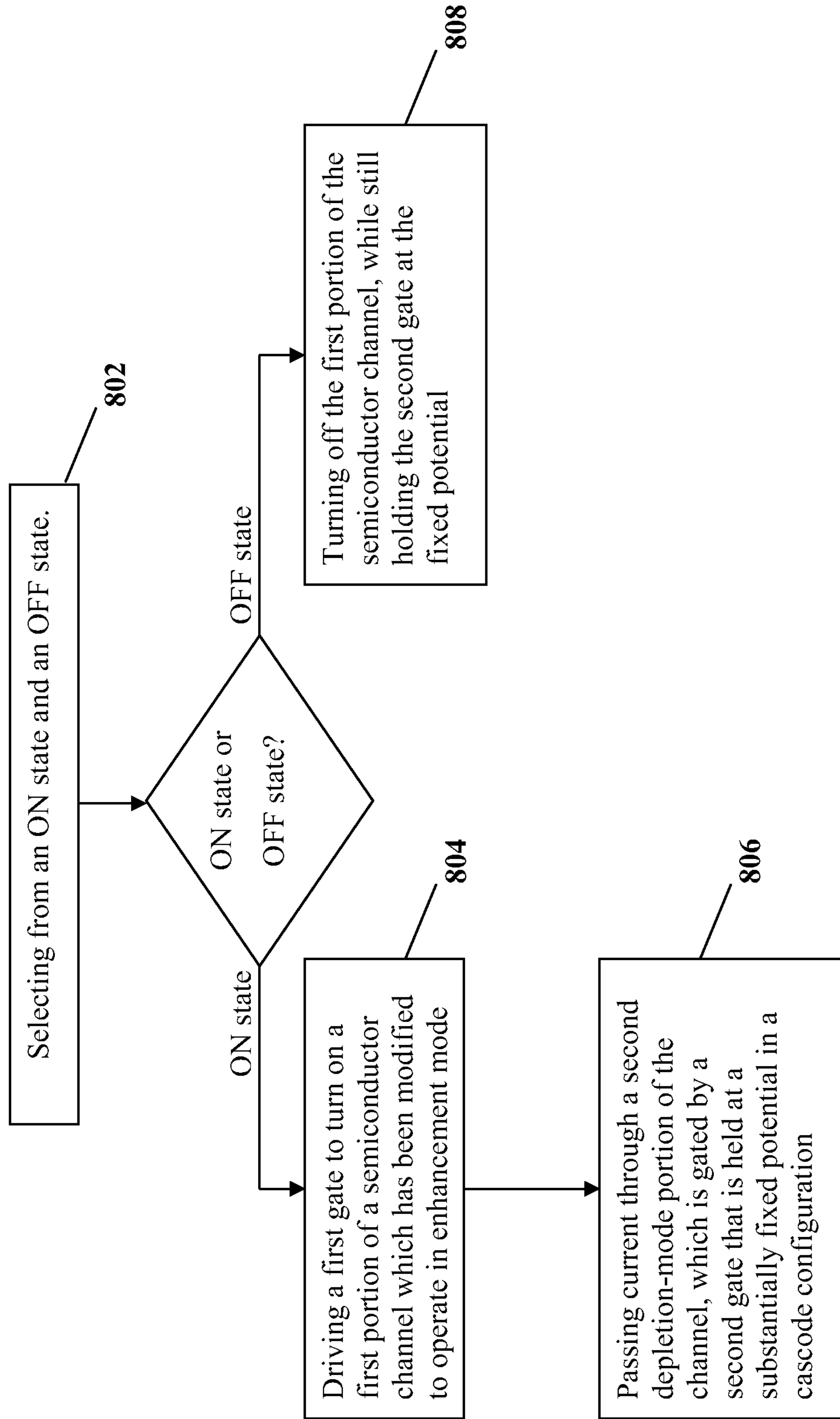


FIG. 8

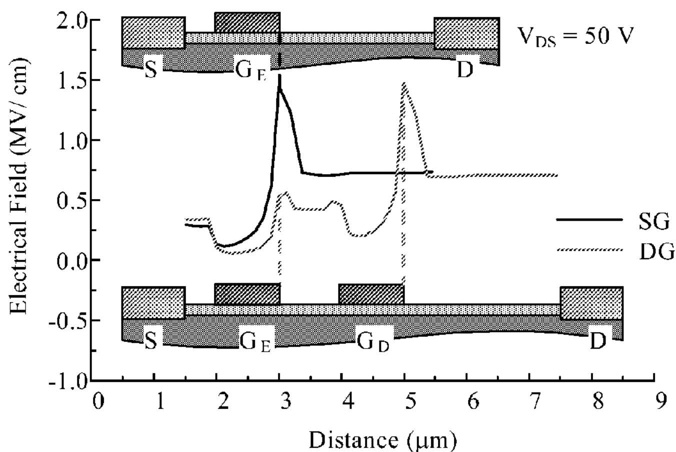


FIG. 9a

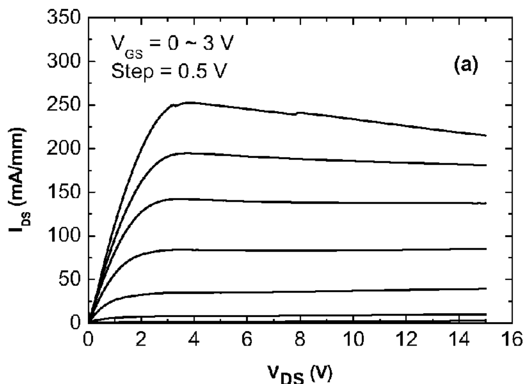


FIG. 9b

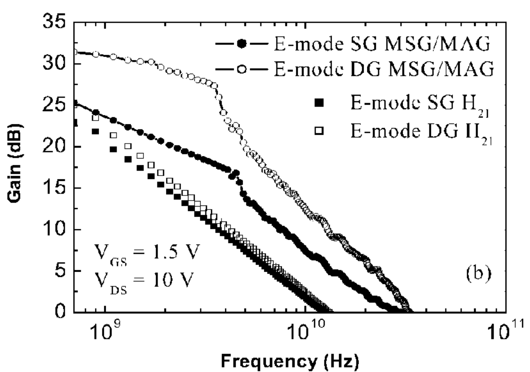


FIG. 9c

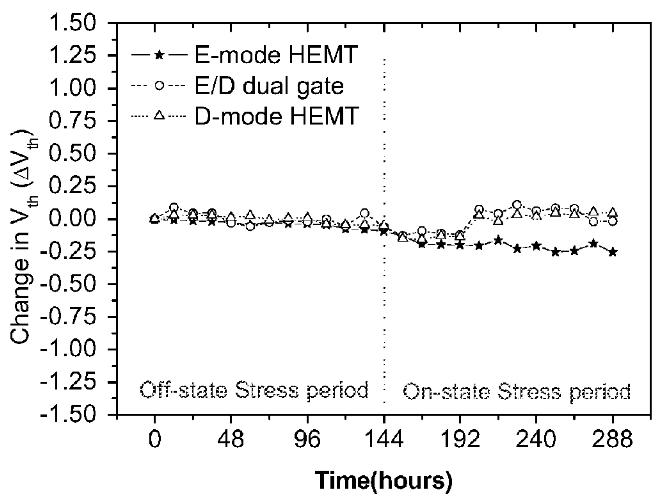


FIG. 9d

RELIABLE NORMALLY-OFF III-NITRIDE ACTIVE DEVICE STRUCTURES, AND RELATED METHODS AND SYSTEMS

CROSS-REFERENCE TO OTHER APPLICATION

Priority is claimed from U.S. Provisional Application Ser. No. 60/953,808 filed Aug. 3, 2007, which is hereby incorporated by reference.

BACKGROUND

The present invention relates to electronics, more particularly to semiconductor devices and related methods, and most particularly to III-N type devices in which both enhancement- and depletion-mode devices are made available by patterned dopant ions.

Many field effect transistors (FETs) operate in an ON state at zero applied gate voltage; such transistors are called "depletion-mode." "Enhancement-mode" FETs are those which are in an OFF state at zero applied gate voltage.

An important area of research in semiconductor devices has been the search for a semiconductor technology using a material with a wider bandgap than silicon. Wider bandgap materials have the potential to operate at higher temperatures and higher breakdown voltages. Many years of research and development have been invested in III-V compound semiconductors, such as GaAs and related compounds (InP, AlGaAs, etc.).

In recent years the family of "III-N" semiconductors has been an area of intense development. GaN provided the first blue LED, and such LEDs are now in commercial use. Development of transistors or other active devices in this materials system is very attractive, because of the high bandgaps available (e.g. 3.4V for GaN, and higher for AlGaN alloys).

A difficulty in achieving III-N active devices was the lack of enhancement-mode devices. A key breakthrough in this area was achieved by the present inventor and colleagues, using fluorine implantation to introduce fixed charge into the top (higher-bandgap) layer of a HEMT-like device. These techniques are described in published U.S. patent applications 2007-0295993, 2007-0228416, and 2007-0278518, all of which are hereby incorporated by reference in their respective entireties for all purposes.

Note that the points discussed above may reflect the hindsight gained from the disclosed inventions, and are not necessarily admitted to be prior art.

SUMMARY

The present inventor has realized that threshold voltage drift can occur, in devices of the types described above, under voltage stress. The present application teaches that such voltage drift can be prevented, in various embodiments, by using dual-gate enhancement/depletion devices, especially if the gates are connected in a cascode configuration. This provides a more reliable and stable device, at the cost of only minimal degradation in the device's drive capability.

BRIEF DESCRIPTION OF THE DRAWINGS

The following figures form part of the present specification and are included to further demonstrate certain aspects of the present claimed subject matter, and should not be used to limit or define the present claimed subject matter. Consequently, a more complete understanding of the present embodiments and further features and advantages thereof may be acquired

by referring to the following description taken in conjunction with the accompanying drawings, in which the leftmost significant digit(s) in the reference numerals denote(s) the first figure in which the respective reference numerals appear, wherein:

FIG. **1** is a cross sectional schematic diagram of a field-effect transistor **100** including at least one teaching of the present invention.

FIG. **2** is a flowchart of a method of manufacturing a field-effect transistor, and includes at least one teaching of the present invention.

FIG. **3** is a flowchart of a method for using a field-effect transistor, e.g. E-mode AlGaN/GaN HEMT fabricated by a fluorine plasma treatment, and includes at least one teaching of the present invention.

FIGS. **4***a* and **4***b* are graphs of source-drain output characteristics and transfer characteristics, respectively, of the E-mode HEMT before and after 144-hours OFF-state stress, in accordance with the method of FIG. **3**.

FIGS. **5***a* and **5***b* are graphs of source-drain output characteristics and transfer characteristics, respectively, of the E-mode HEMT before and after an additional 148-hours ON-state stress, in accordance with the method of FIG. **3**.

FIG. **6***a* is a graph of DC characteristics (Vth, Imax Gm and Ron) as a function of high electric-field stress time, in accordance with the method of FIG. **3**.

FIG. **6***b* is a graph of DC characteristics (Vth, Imax, Gm and Ron) as a function of thermal stress time.

FIG. **7***a* is a cross sectional schematic diagram of a dual-gate MOSFET (metal oxide semiconductor field-effect transistor) **700** including at least one teaching of the present invention.

FIG. **7***b* illustrates the equi-potential profiles in a single- and dual-gate enhancement-mode devices.

FIG. **8** is a flowchart of a method of operating a field-effect transistor that incorporates at least one teaching of the present invention.

FIG. **9***a* is a graph of electric-field strength distribution from the source to drain in, in accordance with the E-mode single-gate and E/D dual-gate HEMTs of FIG.

FIG. **9***b* is a chart that shows E/D dual-gate HEMT characteristics, dc source-drain output characteristics, short-circuit current gain (h21) and maximum stable/maximum available gain (MSG/MAG), for the dual-gate device in comparison with the single-gate device.

FIG. **9***c* is a graph that shows a variation of Vth as a function of high-field stress time in single-gate and dual-gate E-mode HEMTs, and FIG. **9***d* similarly compares gain v. frequency for single and dual-gate devices.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross sectional schematic diagram of a field-effect transistor **100** including at least one teaching of the present invention. The field-effect transistor **100** includes a HEMT (High Electron Mobility Transistor), which uses a heterostructure, i.e. a junction between two materials with different bandgaps, instead of local doping to provide mobile electrons in a channel. The heterostructure includes a highly doped wide-bandgap n-type donor-supply layer whose electrons drop completely into an undoped narrow-bandgap channel layer with no dopant impurities. The undoped narrow-bandgap channel layer then accommodates a two-dimensional electron gas, i.e. a very thin layer of highly mobile conducting electrons with very high concentration. The electrons can move quickly without colliding with any impurities because the undoped narrow-bandgap channel layer is

undoped. The heterojunction created by different band-gap materials forms a steep canyon in the conduction band on the undoped narrow-bandgap channel layer side from which they cannot escape. A buffer layer may be included.

Negatively charged fluorine ions are incorporated into the top AlGaN barrier, which effectively depletes the electrons in the channel. For practical implementation of the fluorine plasma treatment technology in the fabrication of normally-off III-V FETs, it is important to ensure the stability of the fluorine ions, making sure that they do not move around after long-term electrical stress. The field-effect transistor **100** has a threshold voltage that remains stable during the device operation, especially under high electric-field electrical stress or high temperature thermal stress, provided the fluorine ions do not migrate due to intense electrical-field and/or thermal stress. Enhancement mode (or normally off) transistors, whose channel current is zero when a gate voltage is zero, are often more appropriate for FETs in a power electronics or logic circuit. Normally-on (depletion mode) devices remain ON at zero gate bias and become OFF at negative gate bias The heterojunction, or two-dimensional electron gas (2DEG) is a thin layer where the Fermi energy is above the conduction band, giving the channel low resistance or high electron mobility. Of course, other compounds may be used. GaN, AlN, AlInN, AlGaN, InGaN, InAlGaN or combinations thereof, each possibly doped e.g. with Silicon, each consisting of one or more layers; regions may be possibly separated by a spacer.

For example, a gate **102** has a length of 1 μm, and is spaced from a source **104** by a distance of 1 μm (gate-source spacing) and from a drain **106** by a distance of 3 μm (gate-drain spacing). The devices need not be passivated. Initial values of Vth, Imax, Gm, Ron, may be +1.02 V, 240 mA/mm, 135 mS/mm, and 11.9 ohm-mm, respectively. The off-state breakdown voltage (VBK) is about 60 V before the stress test. The field-effect transistor **100** has an ON state and an OFF state. When the device is being used, VDS may be, for example, 15V, 30 V, or 45 V, or other value. A gate-source voltage VGS may be fixed at −2 V (below pinch-off) in the OFF-state and 2 V (corresponding to a 150 mA/mm drain current density) in the ON-state. High quality III-V device substrates and active device and buffer layers may be grown epitaxially, using molecular beam epitaxy (MBE), metalorganic chemical vapor deposition (MOCVD), vapor phase epitaxy, and variations thereof.

FIG. **2** is a flowchart of a method of manufacturing a field-effect transistor, and includes at least one teaching of the present invention. The method of FIG. **2** includes converting a channel of an as-grown depletion-mode (D-mode) III-nitride HEMT structure into E-mode. Specifically, the method comprises depleting **202** electrons in a channel without significantly affecting carrier mobility. For example, negatively charged fluorine ions may be incorporated **204** into a top AlGaN barrier, to create an E-mode gate containing fluorine ions. A D-mode gate may also be created **206** that contains no fluorine ions, but has a high E-field.

The E-mode gate and a D-mode gate may be connected **208** in a cascode-connection. Fluorine ions may be shielded **210** from a high electric field, even under high drain voltage. If desired, a field plate may be used **212**, either source-terminated or gate-terminated, to reduce electric-field strength at a drain-edge of the E-mode gate.

FIG. **3** is a flowchart of a method for using a field-effect transistor, e.g. an E-mode AlGaN/GaN HEMT fabricated by a fluorine plasma treatment, and includes at least one teaching of the present invention. The method depicted with respect to FIG. **3** tests reliability of enhancement-mode AlGaN/GaN HEMTs (fabricated by a fluorine plasma treatment technique) by applying OFF-state and ON-state long-term high-electric-field stress, with focus on Vth's stability under high electric-field stress.

A moderate negative shift (−0.25 V) is observed in the threshold voltage after 288 hours of stress. This shift, however, can be eliminated with an enhancement/depletion dual-gate configuration, which effectively prevents high electric field from influencing the fluorine plasma treated area.

Enhancement-mode (or normally-off) III-nitride HEMTs, with a positive threshold voltage (Vth), are key components for high-speed power switches, high temperature GaN integrated circuits, and RFICs and MMICs with single voltage supply. They provide the benefits of simple circuit configuration as well as favorable operating conditions for device safety. A robust and low-cost technique, namely, the fluoride-based plasma treatment, [2] has been developed for converting the channel of as-grown depletion-mode (D-mode) III-nitride HEMT structures into E-mode.

The E-mode HEMTs are fabricated using the fluorine plasma treatment technique, and feature a 1 μm gate length, a 1 μm gate-source spacing and a 3 μm gate-drain spacing. The devices are not passivated for simplicity in analysis. Initial values of Vth, Imax, Gm, Ron, are +1.02 V, 240 mA/mm, 135 mS/mm, and 11.9 mm. The off-state breakdown voltage (VBK) is about 60 V before the stress test. Negatively charged fluorine ions are incorporated **302** into a top AlGaN barrier, which effectively depletes the electrons in the channel. Stability and reliability of the fluorine ions and the threshold voltage's stability during the device operation are addressed, for practical implementation of the fluorine plasma treatment under high electric-field electrical stress or high temperature thermal stress.

A set of testing conditions, including a bias voltage for VDS, a gate-source voltage VGS, and a time interval, is selected. Specifically, a bias voltage for VDS is selected **304** from 15V, 30V, and 45V, and a state is selected **306** from ON and OFF. The gate-source voltage VGS is fixed **308** at −2 V (below pinch-off) in the OFF-state and 2 V (corresponding to a 150 mA/mm drain current density) in the ON-state. The E-mode HEMT is stressed in the selected state with the selected bias voltage for VDS for 48 hours **310**. DC characteristics are measured **312** and recorded at a step of every 12 hours after the stress started. At chosen time intervals, 144 hours, 196 hours and 288 hours, the device is "rested" for 24 hours **314** with no electrical stress applied, followed by DC characteristics. If all sets of testing conditions have not yet been executed, another set of testing conditions is selected **316**.

FIGS. **4***a* and **4***b* are graphs of source-drain output characteristics and transfer characteristics, respectively, of the E-mode HEMT before and after 144-hours OFF-state stress, in accordance with the method of FIG. **3**. The characteristics after the stress include the ones measured right after the stress and with a 24-hour of no-stress rest.

FIGS. **5***a* and **5***b* are graphs of source-drain output characteristics and transfer characteristics, respectively, of the E-mode HEMT before and after an additional 148-hours ON-state stress, in accordance with the method of FIG. **3**. The characteristics after the stress include the ones measured right after the stress and with a 24-hour of no-stress rest.

FIG. **6***a* is a graph of DC characteristics (Vth, Imax Gm and Ron) as a function of high electric-field stress time, in accordance with the method of FIG. **3**. Solid symbols are results measured right after the stress. Hollow symbols are the data measured after a 24 hours of no-stress rest. FIG. **6***b* is a graph of DC characteristics (Vth, Imax, Gm and Ron) as a function

of thermal stress time. Stress temperature is 350° C. The measurement is conducted at room temperature after the sample is cooled down at various time of the entire stress process.

With respect to FIGS. **4***a*, **4***b*, **5***a*, **5***b*, **6***a* and **6***b*, it is observed that Vth experienced a gradual but persistent high-field-induced negative shift (from 1.02 V to 0.77 V) after 144 hours of OFF-state plus 144 hours of ON-state high-field stress. This negative shift in Vth cannot be recovered by no-stress rest, while the degradation in the on-resistance (Ron) can "recover" after the rest. It is also found that Vth, Ron, maximum drain current density Imax, and peak transconductance Gm are stable during 153 hours of thermal stress at 350° C., suggesting excellent thermal stability for the fluorine ions incorporated in III-nitride materials.

FIG. **7** is a cross sectional schematic diagram of a dual-gate MOSFET (metal oxide semiconductor field-effect transistor) **700** including at least one teaching of the present invention. The dual-gate ("DG") HEMT is based on a cascode-connection of an E-mode gate and a D-mode gate, and leads to improved stability and reliability by physically separating the E-mode gate from the high electric field. The dual-gate MOSFET **700** is arranged in a cascode arrangement, with a common source FET (i.e., a FET having a grounded source terminal **708**) driven by a signal source Vin, and a common gate FET (i.e., a FET having a grounded gate terminal) providing an output signal Vout. The common source FET has a drain, and the common gate FET has a source, that are coupled together within a HEMT channel **720**, designated as a two-dimensional electron gas. The dual-gate MOSFET **700** also includes a Ti/Al/Ni/Au ohmic contact 722, 2.5 μm GaN **724**, Fluorine ions **726**, and Sapphire **730**. Since the shift in Vth is due to the presence of high electric-field in the gate region of the E-mode HEMT, physical separation of the E-mode gate and high electric-field could lead to improved stability and reliability. To improve Vth's stability, a dual-gate (DG) HEMT based on a cascode-connection of an E-mode gate and a D-mode gate is designed and fabricated as shown.

In the dual-gate MOSFET **700** of FIG. **7**, however, the common source FET is operated in enhancement mode. The common source FET includes a first gate **704** which is driven by the signal source Vin, an enhancement mode portion **706** within the HEMT channel, which is gated to be turned on and off by the first gate, and the grounded source terminal **708**. The first gate **704**, or first gate terminal, is fabricated of a material such as nickel, gold, nickel/gold alloy, or other conductive material. The enhancement mode FET includes an enhancement mode portion and a depletion mode portion.

The enhancement mode portion **706** has an insertion element that can deplete the semiconductor channel near the first gate. The insertion element can include, for example, fluorine ions **726**; enhancement mode can be achieved by implantation of fluorine ions **726**. The depletion mode portion **706** of the semiconductor channel **720** at least partially shields the insertion element, such that the insertion element does not significantly migrate from the enhancement mode portion in response to an electrical-field and/or thermal stress at the depletion mode portion.

The common gate FET, i.e. depletion mode FET, has a second gate **710**, or second gate terminal, that is fabricated of a material such as nickel, gold, nickel/gold alloy, or other conductive material and that that is held at a substantially fixed potential, such as ground potential (as a common gate). For example, the second gate **710** may be electrically coupled to the source terminal of the field effect transistor.

The second gate **710** is electrically coupled to a fixed potential, such as a ground potential. The second gate **710** may comprise a field plate. If desired, the second gate **710** may be electrically coupled to the first gate **704**.

The depletion mode FET also has a depletion mode portion **712**, gated by the second gate **710**, that inherently operate in depletion mode (without any fluorine ions **726** incorporated in the AlGaN layer) and that is operative to shield the first gate **704** from voltage stress. The depletion mode FET also has an output drain **714**.

The fluorine ions **726**, or such other insertion element as may be desired, are shielded from high electrical-field stresses that may be encountered near the depletion mode portion or near the output drain **714**. As a result, the fluorine ions **726** are not dislodged or moved by such stresses, and remain in place, preserving the enhancement mode of the common source FET. Since the threshold potential (i.e., the threshold voltage) of the MOSFET **700** is primarily governed by the ability of the common source FET to remain in enhancement mode, the MOSFET **700** has a substantially stable threshold potential in a presence of electrical-field stress at the depletion mode portion. FIG. **7***b* illustrates the equi-potential profiles in single- and dual-gate enhancement-mode devices. The peak electric-field is located at the edge of the D-mode gate (away from the E-mode gate and fluorine ions) in the dual-gate device.

The output of the cascode arrangement is effectively isolated from the input, both electrically and physically, and thus is very stable. The enhancement mode transistor has nearly constant voltage at both drain and source. The depletion mode transistor has nearly constant voltage at its gate and source. Thus, the only nodes with significant voltage on them are the input and output, and these are separated by the central connection of nearly constant voltage and by the physical distance of two transistors. Thus in practice there is little feedback from the output to the input. Metal shielding is both effective and easy to provide between the two transistors for even greater isolation when required.

The E/D cascode-connected DG HEMT structure has improved stability of Vth of E-mode HEMTs under high-electric-field stress. The D-mode gate resides between the E-mode gate and the drain, and is electrically connected to the source, effectively shielding the E-mode gate (where is treated by fluorine plasma) from high electrical field during high voltage device operation. No persistent negative shift in Vth is observed in the DG HEMT after stress. In addition, the E/D DG HEMT shows higher power gain because of the reduced feedback capacitance and larger output resistance.

Both the OFF-state and ON-state, with high-field stress, result in gradual negative shift of Vth. This shift persists even after 24 hours of no-stress rest, indicating the occurrence of high-electric-field-induced negative shift in the threshold voltage. This also suggests that a solution could be found for improving the Vth's stability by shielding the fluorine plasma treated region from high electric field.

Both the OFF-state and ON-state stress results in degradation in the Ron. This degradation, however, recovers after the no-stress rest and even improves (smaller Ron) eventually. The recovery trend is consistent with what has been reported in conventional D-mode HEMTs, although the negative shift in Vth also contributes by presenting a smaller channel resistance. Both Imax and Gm suffer minor degradation under stress, but recover after the no-stress rest, a result of the reduced Ron.

The negative shift in the threshold voltage after long-term high field stress suggests that the certain changes occurred in the gate region as a result of the stress. The negatively charged fluorine ions experience a strong coulomb force during the electric stress, which could lead to a physical migration of

these ions away from the gate edge. The reduction of the negatively charged fluorine ions in the gate region could then lead to a negative shift in Vth. A direct observation of the electrical-stress-induced migration of the fluorine ions is needed to confirm this argument.

Thermal stress test of an E-mode HEMT was conducted by putting the device on a hot stage at 350° C. in vacuum, for up to 153 hours. At various time, the device was taken out and cooled down to room temperature, at which the dc testing was performed. No obvious degradation is observed in Vth, Imax, Gm and Ron.

The HEMT of FIG. **1** is a highly efficient GaAs enhancement/depletion (E/D) dual-gate (DG) high electron mobility ET (HEMT) that can be operated with a small single biasing supply with a large output impedance, about an order of magnitude larger than a single-gate FET). It has a small feedback capacitance, since the second gate screens the signal feedback from the drain to the first gate, improving isolation between input and output terminals and improving linearity of input-output characteristics, as well as improving device gain. It has a small phase distortion, since polarity of phase deviation in common-source FETs and common-gate FETs is opposite. Finally, it has a large design flexibility, since the first gate has high gain and the second gate has high breakdown voltage.

FIG. **8** is a flowchart of a method of operating a field-effect transistor that incorporates at least one teaching of the present invention. The method includes selecting **802** from an ON state and an OFF state. In the ON state, the method includes driving **804** a first gate to turn on a first portion of a semiconductor channel which has been modified to operate in enhancement mode. The method also includes passing **806** current through a second depletion-mode portion of the channel. The current and the channel are gated by a second gate, which is held at a substantially fixed potential in a cascode configuration. In the OFF state, the method includes turning **808** off the first portion of the semiconductor channel, while still holding the second gate at the fixed potential, wherein the second portion of the channel shields the first gate from voltage stress.

FIG. **9***a* is a graph of electric-field strength distribution from the source to drain in, in accordance with the E-mode single-gate and E/D dual-gate HEMTs of FIG. **7**. The simulation is carried out using ISE's Santaurus simulator. VDS is set at 50 V. In the dual-gate device, the peak field occurs at the drain-side of the D-mode gate instead of the E-mode gate where the fluorine ions are located. As indicated by the simulation results, the electric fields peak at the edge of the D-mode gate of the E/D DG device.

FIG. **9***b* is a chart that shows E/D dual-gate HEMT, dc source-drain output characteristics. FIG. **9***c* shows the short-circuit current gain (h21) and maximum stable/maximum available gain (MSG/MAG), for the dual-gate device in comparison with the single-gate device. The dual-gate HEMT shows improved power gain because of the increased output resistance and the reduced feedback capacitance.

The threshold voltage of the E/D DG HEMT exhibits much improved stability with no persistent negative shift. The trend of Vth as a function of the electrical-stress time is very close in the E/D dual-gate HEMT and the D-mode single gate HEMT (which did not experience the fluorine plasma treatment). Compared to the single gate device, the dual-gate HEMT also shows comparable dc performance and improved high frequency power gain as a result of the reduced feedback capacitance and increased output resistance.

FIG. **9***d* is a graph that shows a variation of Vth as a function of high-field stress time in single-gate and dual-gate E-mode HEMTs. The results of a D-mode single-gate HEMT are also plotted for comparison. Moderate negative shift in Vth is observed in the fluorine plasma treated enhancement-mode HEMT under high-electric-field stress. The device is stable under thermal stress at 350° C. for 153 hours. An E/D dual-gate HEMT is demonstrated to be effective in preventing the shift in Vth and improving its reliability by shielding the E-mode gate with a D-mode gate from high electric field. Similarly, FIG. **9***c* compares gain v. frequency for single and dual-gate devices as described.

Several implementations and embodiments have thus been described. It will be appreciated, however, that other implementations and embodiments may also be substituted within the scope of this disclosure. For example, the field-effect transistor need not include a HEMT; another type of transistor may be used.

Thus, although the invention has been described with reference to several exemplary embodiments, it is understood that the words that have been used are words of description and illustration, rather than words of limitation. Changes may be made within the purview of the appended claims, as presently stated and as amended, without departing from the scope and spirit of the invention in its aspects. Although the invention has been described with reference to particular means, materials and embodiments, the invention is not intended to be limited to the particulars disclosed; rather, the invention extends to all functionally equivalent structures, methods, and uses such as are within the scope of the appended claims.

It is to be noted, however, that the appended drawings illustrate only typical embodiments of the present claimed subject matter and are, therefore, not to be considered limiting of the scope of the present claimed subject matter, as the present claimed subject matter may admit to other equally effective embodiments.

According to various disclosed classes of embodiments, there is provided: A field-effect transistor, comprising: a first gate; a second gate held at a substantially fixed potential in a cascode configuration; and a semiconductor channel having an enhancement mode portion, gated to be turned on and off by said first gate, which has been modified to operate in enhancement mode, and a depletion mode portion, gated by said second gate, which has been modified to operate in depletion mode, and which is operative to shield the first gate from voltage stress.

According to various disclosed classes of embodiments, there is provided: An active device structure in a III-N-type semiconductor material, comprising: first and second conductive source/drain regions, positioned to connect to different locations of a III-N-type semiconductor channel; and first and second gate terminals, each capacitively coupled to a different respective portion of said channel between said source/drain regions; said channel having different respective threshold voltages, of opposite signs, with respect to said first and second gate terminals.

According to various disclosed classes of embodiments, there is provided: A method of operating a field-effect transistor, comprising: in the ON state, driving a first gate to turn on a first portion of a semiconductor channel which has been modified to operate in enhancement mode, while also passing current through a second depletion-mode portion of said channel which is gated by a second gate which is held at a substantially fixed potential in a cascode configuration; in the OFF state, turning off said first portion of said semiconductor channel, while still holding said second gate at said fixed potential, wherein said second portion of said channel shields said first gate from voltage stress.

According to various disclosed classes of embodiments, there is provided: A method of operating a III-N field-effect transistor, comprising: in the ON state, driving a first gate to turn on a first portion of a III-N semiconductor channel, while also passing current through a second portion of said channel which is gated by a second gate which is held at a substantially fixed voltage; and in the OFF state, turning off said first portion of said semiconductor channel, while still holding said second gate at said fixed potential; wherein said first portion of said channel, but not said second portion of said channel, is coupled to localized fixed charge; whereby the operation of said second gate limits voltage stress on said localized fixed charge.

According to various disclosed classes of embodiments, there is provided: A fluoride based plasma method for converting channel of an as-grown depletion-mode (D-mode) III-nitride HEMT structures into E-mode, the fluoride based plasma method comprising: depleting electrons in a channel without significantly affecting carrier mobility, including incorporating negatively charged fluorine ions into a top AlGaN barrier, implementing a D-mode gate containing no fluorine ions but having a high E-field; implementing a modifiable D-mode gate containing no fluorine ions but having a high E-field; converting the modifiable D-mode gate to an E-mode gate containing fluorine ions; arranging a cascode-connection of the E-mode gate and the D-mode gate; and shielding fluorine ions from a high electric-field even under high drain voltage.

According to various disclosed classes of embodiments, there is provided: A field-effect transistor includes a first gate, a second gate held at a substantially fixed potential in a cascode configuration, and a semiconductor channel. The semiconductor channel has an enhancement mode portion and a depletion mode portion. The enhancement mode portion is gated to be turned on and off by the first gate, and has been modified to operate in enhancement mode. The depletion mode portion is gated by the second gate, and has been modified to operate in depletion mode and that is operative to shield the first gate from voltage stress.

Modifications and Variations

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly the scope of patented subject matter is not limited by any of the specific exemplary teachings given. It is intended to embrace all such alternatives, modifications and variations that fall within the spirit and broad scope of the appended claims.

For example, a wide variety of geometries can be used to lay out the first and second gates and the source/drain regions.

For another example, the profiles of the source and drain regions can be different or similar.

Moreover, a wide variety of diffusion or metallization structures can be used to control the distribution of electric field maxima (in the off state) and current density maxima (in the on state) near the source/drain regions.

For example, the materials used do not strictly have to be the AlGaN/GaN combination of the preferred embodiment. As this technology develops, it is to be expected that the disclosed innovative teachings will be applied to other semiconductor alloys which have similar behavior.

For another example, the disclosed teachings are not strictly limited to HEMT-type devices, but can also be used with IGFETs or even IGFET/HEMT hybrids.

The disclosed innovations provide a basic innovation in FET-type current injection structures. As will be appreciated by those skilled in device technology, this injection structure can be used in a wide variety of more complex devices, including devices which are partially bipolar as well as unipolar devices.

None of the description in the present application should be read as implying that any particular element, step, or function is an essential element which must be included in the claim scope: THE SCOPE OF PATENTED SUBJECT MATTER IS DEFINED ONLY BY THE ALLOWED CLAIMS. Moreover, none of these claims are intended to invoke paragraph six of 35 USC section 112 unless the exact words "means for" are followed by a participle.

The claims as filed are intended to be as comprehensive as possible, and NO subject matter is intentionally relinquished, dedicated, or abandoned.

What is claimed is:

1. A field-effect transistor, comprising:
- a first gate having a first connection to a variable voltage source;
- a second gate having a second connection to a fixed voltage source and held at a substantially fixed potential in a cascode configuration; and
- a semiconductor channel having
  - an enhancement mode portion, gated to be turned on and off by said first gate, which has been modified to operate in enhancement mode, and
  - a depletion mode portion, gated by said second gate, which has been modified to operate in depletion mode, and which is operative to shield the first gate from voltage stress.

2. The field-effect transistor of claim **1**, wherein said enhancement mode portion further has a fixed charge positioned to deplete the semiconductor channel near the first gate.

3. The field-effect transistor of claim **2**, wherein:
- the depletion mode portion is situated between the enhancement mode portion and a drain terminal of the field-effect transistor; and
- said fixed charge is at least partially shielded by the depletion mode portion of the semiconductor channel to mitigate fixed charge migration from the enhancement mode portion in response to an electrical-field at the depletion mode portion.

4. The field-effect transistor of claim **1**, wherein the field-effect transistor has a substantially stable threshold voltage under electrical-field stress at said depletion mode portion.

5. The field-effect transistor of claim **1**, wherein the second connection to the fixed voltage source is electrically coupled to a source terminal of the field effect transistor.

6. An active device structure in a III-N-type semiconductor material, comprising:
- a first conductive source and drain region and a second conductive source and drain region, positioned to connect to different locations of a III-N-type semiconductor channel; and
- first and second gate terminals in a cascode configuration, each capacitively coupled to a different respective portion of said III-N-type semiconductor channel between said first conductive source and drain region and the second conductive source and drain region, and wherein one of said gate terminals has a first connection to a variable voltage source, and the other has a second connection to a fixed voltage source;
- said III-N-type semiconductor channel having different respective threshold voltages, of opposite signs, with respect to said first and second gate terminals.

7. The structure of claim **6**, wherein said channel consists essentially of Gallium Nitride.

8. The structure of claim **6**, wherein both said gate terminals are separated from said channel by a semiconductor layer having a wider bandgap than said channel.

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