SCIENTIFIC REPORTS

OPEN

Remarkably high mobility ultra-thin-film metal-oxide transistor with strongly overlapped orbitals

Received: 19 August 2015
Accepted: 02 December 2015
Published: 08 January 2016

Chen Wei Shih[1], Albert Chin[1], Chun Fu Lu[2] & Wei Fang Su[2]

High mobility channel thin-film-transistor (TFT) is crucial for both display and future generation integrated circuit. We report a new metal-oxide TFT that has an ultra-thin 4.5 nm SnO_2 thickness for both active channel and source-drain regions, very high 147 cm^2/Vs field-effect mobility, high I_{ON}/I_{OFF} of 2.3×10^7, small 110 mV/dec sub-threshold slope, and a low V_D of 2.5 V for low power operation. This mobility is already better than chemical-vapor-deposition grown multi-layers MoS_2 TFT. From first principle quantum-mechanical calculation, the high mobility TFT is due to strongly overlapped orbitals.

The metal-oxide thin-film transistor (TFT)[1–20] is a revolutionary technology for displays due to its high mobility and simple process. The high mobility of zinc-oxide (ZnO)-based materials was attributed to the spatially spread metal ns orbitals with isotropic shape, which is possible to overlap the neighboring metal ns orbitals[7]. However, the high performance ZnO-based TFTs of InGaZnO[7], bi-layer InSnO/InGaZnO[11], InZnO[13], and GaZnON[18] compounds usually contain Indium (In) or Gallium (Ga), which are rare elements in earth's crust. In addition, device performance is sensitive to the moisture degradation and atomic composition of these compound. Alternatively, high mobility, high transistor on-current (I_{ON}), and low off-current (I_{OFF}) TFTs are found in two-dimensional metal-chalcogenide[21–28]. However, chemical vapor deposition (CVD)-grown MoS_2[25–28] shows a considerably lower mobility compared with peeled-off flakes from crystals[21–28]. To further increase the display pixel density and drive organic light-emitting diodes (OLED), higher mobility and I_{ON} than those of ZnO-based TFTs are needed. The low DC and switching power consumptions are other technological trends for displays that require a low I_{OFF} and low operation voltage. In this study, a remarkably high field–effect mobility (μ_{FE}) of 147 cm^2/Vs was demonstrated experimentally in tin-oxide (SnO_2) TFT. This TFT also showed a high I_{ON}/I_{OFF} of 2.3×10^7, low sub-threshold swing (*SS*) of 0.11 V/decade, low threshold voltage (V_T) of 0.27 V, low drive voltage of 2.5 V for low switching power, and ultra-thin layer with a thickness of 4.5 nm. Such ultra-thin thickness is comparable with that of multilayered MoS_2[27] for low DC standby power consumption. Notably, Sn (Group IV) has ns^2np^2 electron configuration and directive sp^3 orbitals, which differ from those of Zn[7]. According to first principle quantum-mechanical calculations, the considerably high μ_{FE} in SnO_2 TFT is caused by its overlapped s-orbitals even in an ns^2np^2 configuration.

Results

To increase the transistor I_{ON} and reduce the operation voltage, a high-dielectric-constant (high-κ) gate insulator[12,15] was used for the TFT. Figure 1(a) shows the current-voltage (*I-V*) and capacitance-voltage (*C-V*) characteristics of a gate capacitor with top Aluminum (Al) electrode, high-κ hafnium-oxide (HfO_2), and bottom n^+-Si. In the Al/HfO_2/n^+-Si capacitor, a small leakage current of 5.7×10^{-7} A/cm^2 at 2 V was obtained at a capacitance density of 0.38 μF/cm^2. The high capacitance density yielded a low equivalent-oxide-thickness (EOT) of only 9.1 nm, which was due to the high-κ HfO_2 with a κ of 17. Figure 1(b) shows the transistor's drain current versus gate voltage (I_{DS}-V_{GS}) characteristics of the SnO_2/HfO_2 TFTs with 4.5 ~ 20 nm thick SnO_2. The device with thick 20 nm SnO_2 failed to show proper pinch off I_{OFF} due to very high conductivity, although the device has very high I_{ON}. The device with 4.5 nm thick SnO_2 shows the best I_{ON}/I_{OFF} performance. Figure 1(c,d) show the transistor's drain current versus drain voltage (I_{DS}-V_{DS}), I_{DS}-V_{GS}, and μ_{FE}-V_{GS} characteristics of the SnO_2/HfO_2 TFT with 4.5 nm thick SnO_2, respectively. The device was operated in the enhancement mode of an n-channel metal-oxide-semiconductor field-effect transistor (nMOSFET) at a low operation voltage of 2.5 V. The device also showed a high I_{ON}/I_{OFF} of 2.3×10^7, low *SS* of 110 mV/decade, and low V_T of 0.27 V. The V_T was extracted from the intercept of the linear $I_{DS}^{1/2}$-V_{GS} curve in a saturation region. A high I_{ON} is crucial to drive the OLED and increase the display pixel density, whereas a

[1]Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan. [2]Depatment of Materials Science & Engineering National Taiwan University, Taipei 10617, Taiwan. Correspondence and requests for materials should be addressed to A.C. (email: achin@faculty.nctu.edu.tw)

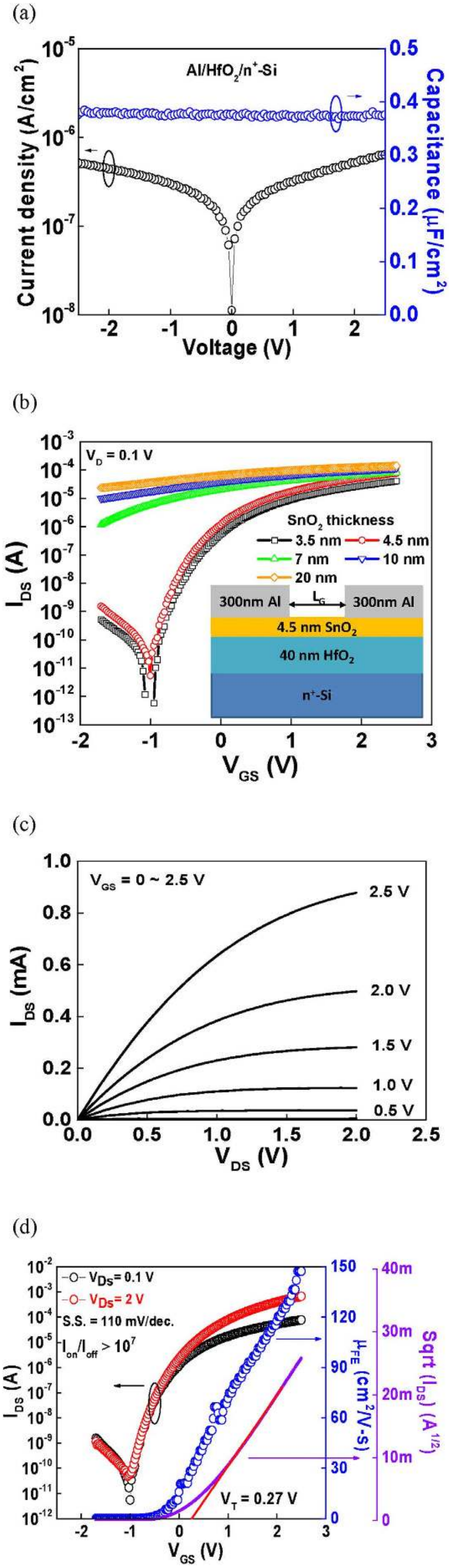

Figure 1. (**a**) *I-V* and *C-V* characteristics of gate capacitor, (**b**) I_{DS}-V_{GS} characteristics of Al/SnO_2/HfO_2/n^+-Si TFTs with 20 ~ 3.5 nm SnO_2 layers, (**c**) I_{DS}-V_{DS} and (**d**) I_{DS}-V_{GS}, μ_{FE}-V_{GS} and Sqrt(I_{DS})-V_{GS} characteristics of Al/SnO_2/HfO_2/n^+-Si TFTs at 4.5 nm SnO_2 thickness. The gate length is 50 μm.

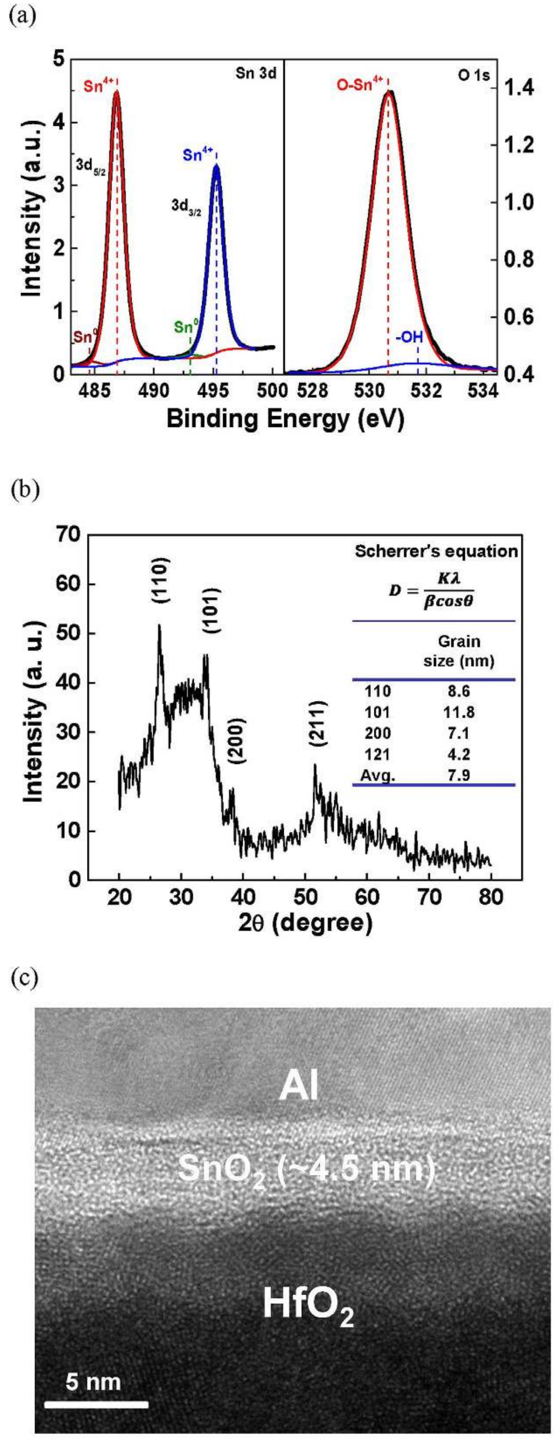

Figure 2. (**a**) XPS, (**b**) XRD, and (**c**) TEM analysis of SnO_2 formed on HfO_2/n^+-Si. The SnO_2 thickness is 20 nm for XPS and XRD analysis, while 4.5 nm for TEM.

low I_{OFF} is required to reduce the DC standby power. The low *SS* with the mean value and standard deviation of 100.2 ± 19.4 mV/decade indicates the good oxide/semiconductor interface to turn on the transistor fast. The I_{ON} showed an inversely proportional relation with gate length in a wide gate length TFT, a typical method to extract mobility correctly for Si MOSFET and metal-gate/high-κ MOSFET[29–31]. A remarkably high μ_{FE} of 147 cm^2/Vs is obtained with the mean value and standard deviation of 141.6 ± 11.5 cm^2/Vs, which is higher than that of ZnO-based TFTs[3–20] and even higher than that of a CVD-grown multilayered MoS_2 MOSFET[21–24]. To reach high mobility, epitaxial growth of crystalline MoS_2 on a crystal substrate is needed. Unfortunately, the mobility is lower for CVD-grown MoS_2[25–28] than peeled-off flakes from crystals[21–28]. The lattice mismatch caused defects are the other major concern for circuit yield. In contrast, high mobility SnO_2 TFT is achievable on the amorphous substrate

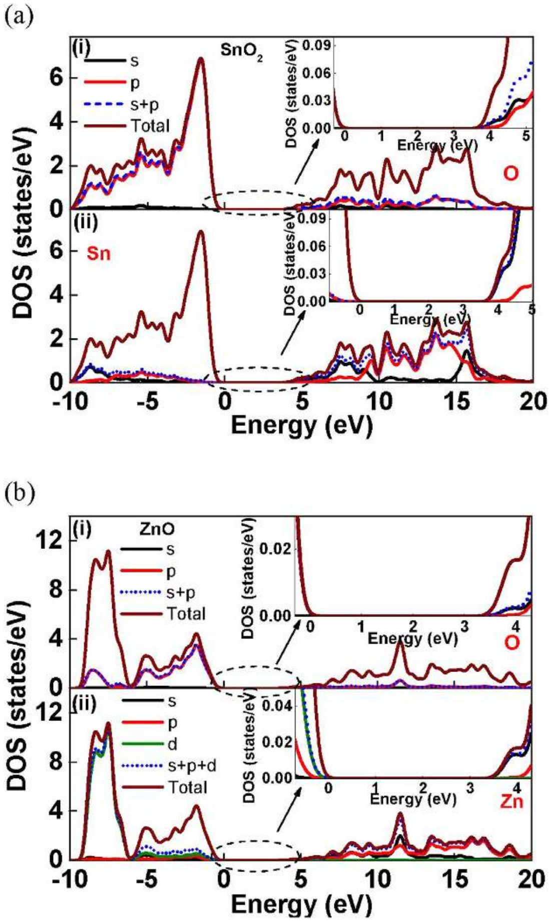

Figure 3. (**a**) DOS of (i) O, and (ii) Sn in SnO_2, and (**b**) DOS of (i) O, and (ii) Zn in ZnO.

and free from lattice-mismatch defects. Such metal-oxide has already been used to manufacture TFT circuit for display. It is crucial to notice that the mobility of metal-oxide increases with increasing carrier density[7]. In the 4.5-nm-thick SnO_2 TFT, the high mobility is due to the high V_G-induced carrier density[31] of ~10^{13} cm^{-2} to screen out charged defects. This is also supported by the higher mobility with larger V_G[7], where induced carrier density increases with V_G. In the thicker 7 ~ 20 nm SnO_2 devices with poor pinch off, the mobility is lowered by extra parallel conduction from non-depleted bulk SnO_2. The mobility is lowered in 3.5 nm SnO_2 TFT due to stronger roughness scattering from top surface. Here the SnO_2 surface roughness is 0.39 nm, close to the HfO_2 roughness of 0.41 nm.

The high mobility SnO_2 TFT was further investigated using material analysis. Figure 2(a) shows the X-ray photoelectron spectroscopy (XPS) spectra from the Sn 3d and O 1s core level of the SnO_2 thin film. The Sn 3d peak corresponded to the oxidation state of Sn^{4+}, and the O 1s peak was attributed to the O-Sn and O-H bonds. Thus, the chemical composition was determined to be $Sn^{4+}O_2^{2-}$. The X-ray diffraction spectroscopy (XRD) pattern in Fig. 2(b) reveals the presence of a rutile phase in SnO_2. An average grain size of 7.9 nm was obtained using the Scherrer's equation. Figure 2(c) shows the cross-sectional transmission electron microscopy (TEM) image of the SnO_2/HfO_2 stack. A relatively uniform SnO_2 layer with an ultra-thin thickness of 4.5 nm was observed.

To thoroughly understand the cause of the high mobility in SnO_2 TFT, first principle quantum-mechanical calculations were used to investigate the electronic structures of SnO_2 and ZnO; ZnO has been extensively studied using the localized density functional theory (DFT) to reveal the mechanism that leads to its high mobility. The structures of both SnO_2 and ZnO semiconductors were successfully obtained using local density approximation plus U (LDA+U) method with appropriate U^p and U^d value. The LDA+U method compensates for the under-estimation of the bandgap caused by a strong self-interaction by the DFT. The bandgaps of SnO_2 and ZnO were calculated to be 3.68 and 3.39 eV (Figure S1(a) and S1(b)), respectively, which are consistent with the experimental values of 3.6 and 3.4 eV, respectively. The contribution of each orbital in the conduction band minimum (CBM) of SnO_2 was investigated using density of state (DOS) analysis. The energy of valence band minimum was set to zero for convenience. As shown in Fig. 3(a), the upmost valence band was predominated by the O 2p orbitals, and the contribution from Sn was mostly from 5p orbitals. The lower conduction states near CBM were mostly derived from Sn 5s orbitals, whereas the O 2p orbitals contributed only in higher energy states. The Sn 4d orbitals did not give rise to the electron conducting property of SnO_2 because the antibonding interaction between Sn 4d and O 2p orbitals led only to the slight mixing of states at a deep valence band level. The DOS results of ZnO (Fig. 3(b)) were similar to those of SnO_2. The major difference between the valence bands of SnO_2 and ZnO is the contribution of d orbitals. The upper valence bands (from −6 to 0 eV) were composed of primarily of O 2p orbitals and slight mixing states from Zn 4s, 4p and 3d, whereas Zn 3d orbitals dominated in deeper states. In conduction band, Zn 4s was the major component near CBM while O 2p orbitals had little contribution at levels lower than 5 eV. Therefore, the high mobility of SnO_2 was attributed to the overlapping of s-orbitals, as with ZnO, although it had ns^2np^2 configuration. This is further supported by the charge density distribution of SnO_2 shown in Figure S2(a), which has highly overlapped orbitals similar with those of ZnO in Figure S2(b). The highly overlapped orbitals of SnO_2 is related to large atomic radius, one row below Zn in the periodic table. From the results of DOS and charge density distribution, the higher mobility than the state-of-the-art ZnO TFTs[32–33] is attributed to the highly overlapped s-orbitals of SnO_2.

The carrier effective mass is a major factor that may explain the higher mobility of SnO_2 than that of ZnO. The high electron mobility of n-type materials is caused by a deep curvature in CBM of band structure shown in Figure S1(a) and S1(b), which leads to a low effective mass of electrons. The calculated electron effective mass of SnO_2 was approximately 20% lighter than that of ZnO, indicating a faster electron transport in the SnO_2 conduction band.

In conclusion, this SnO_2 TFT device had a considerably high mobility, high I_{ON}/I_{OFF}, low *SS*, low operation voltage, and ultra-thin thickness. The low operation voltage is due to the high-κ gate dielectric with a high capacitance density. The low SS indicates the good gate dielectric and SnO_2 interface. The high I_{ON}/I_{OFF} is related to the high mobility to increase I_{ON} and the ultra-thin thickness to decrease I_{OFF}, where the high mobility is caused by strongly overlapped s-orbitals.

Methods

The SnO_2 TFTs were fabricated on a heavily doped n-type silicon (100) substrate. The 40-nm-thick high-κ gate HfO_2 and 20 ~ 3.5-nm-thick SnO_2 films were deposited by physical vapor deposition. Thicker 20 nm SnO_2 film was also deposited for X-ray photoelectron spectroscopy (XPS) and X-ray diffraction (XRD) pattern analysis. Then the high-κ layer and SnO_2 film was annealed at 400°C. Finally, the Al source-drain electrodes were thermally evaporated and patterned. The gate length and width are 50 ~ 150 μm and 500 μm, respectively. Therefore, the maximum process temperature for this device is 400°C. The fabricated devices were characterized by XPS, XRD, TEM, *C-V*, and *I-V* measurements. All quantum-mechanical calculations were performed by Cambridge Sequential Total Energy Package (CASTEP) code. Structural optimization was performed on each model prior to calculating their electrical properties. The LDA+*U* method is known to correct the strong correlation of metal oxides and is proven to be quite effective for ZnO. The calculations were carried out by using generalized gradient approximation (GGA) with LDA+*U*.

References

1. Boesen, G. F. & Jacobs, J. E. Comparison between the oscillating limiter and the first-order phase-locked loop. *Proceedings of IEEE* **12,** 2094 (1968).
2. Prins, M. W. J. *et al.* A ferroelectric transparent thin-film transistor. *Appl. Phys. Lett.* **68,** 3650 (1996).
3. Nomura, K. *et al.* Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor. *Science* **300,** 1269 (2003).
4. Hoffman, R. L., Norris, B. J. & Wager, J. F. ZnO-based transparent thin-film transistors. *Appl. Phys. Lett.* **82,** 733 (2003).
5. Carcia, P. F., McLean, R. S., Reilly, M. H. & Nunes, G. Transparent ZnO thin-film transistor fabricated by rf magnetron sputtering. *Appl. Phys. Lett.* **82,** 1117 (2003).
6. Masuda, S. *et al.* Transparent thin film transistors using ZnO as an active channel layer and their electrical properties. *J. Appl. Phys.* **93,** 1624 (2003).
7. Nomura, K. *et al.* Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **432,** 488 (2004).
8. Presley, R. E. *et al.* Tin oxide transparent thin-film transistors. *J. Phys. D-Appl. Phys.* **37,** 2810 (2004).
9. Fortunato, E. M. C. *et al.* Fully transparent ZnO thin-film transistor produced at room temperature. *Adv. Mater.* **17,** 590 (2005).
10. Iwasaki, T. *et al.* Combinatorial approach to thin-film transistors using multicomponent semiconductor channels: An application to amorphous oxide semiconductors in In–Ga–Zn–O system. *Appl. Phys. Lett.* **90,** 242114 (2007).
11. Kim, S. I. *et al.* High performance oxide thin film transistors with double active layers. *IEDM Tech. Dig.* **73** (2008).
12. Su, N. C., Wang, S. J. & Chin, A. High-performance InGaZnO thin-film transistors using HfLaO gate dielectric. *IEEE Electron Device Lett.* **30,** 1317 (2009).
13. Park, J. C. *et al.* High performance amorphous oxide thin film transistors with self-aligned top-gate structure. *IEDM Tech. Dig.* **191** (2009).
14. Kamiya, T., Nomura, K. & Hosono, H. Present status of amorphous In–Ga–Zn–O thin-film transistors. *Sci. Technol. Adv. Mater.* **11,** 044305 (2010).
15. Su, N. C. *et al.* Low-voltage-driven flexible InGaZnO thin-film transistor with small subthreshold swing. *IEEE Electron Device Lett.* **31,** 680 (2010).
16. Zan, H. W., Tsai, W.-W., Chen, C.-H. & Tsai, C.-C. Effective mobility enhancement by using nanometer dot doping in amorphous IGZO thin-film transistors. *Adv. Mater.* **23,** 4237 (2011).
17. Fortunato, E., Barquinha, P. & Martins, R. Oxide semiconductor thin-film transistors: A review of recent advances. *Adv. Mater.* **24,** 2945 (2012).
18. Kim, T. S. *et al.* High performance gallium-zinc oxynitride thin film transistors for next-generation display applications. *IEDM Tech. Dig.* **660** (2013).
19. Lee, E. *et al.* Nanocrystalline ZnON; High mobility and low band gap semiconductor material for high performance switch transistor and image sensor application. *Scientific Reports* **4,** 4948 (2014).
20. Bak, J. Y. *et al.* Origin of degradation phenomenon under drain bias stress for oxide thin film transistors using IGZO and IGO channel layers. *Scientific Reports* **5,** 7884 (2015).
21. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. Single-layer MoS_2 transistors. *Nature Nanotech.* **6,** 147 (2011).
22. Kim, S. *et al.* High-mobility and low-power thin-film transistors based on multilayer MoS_2 crystals. *Nature Commun.* **3,** 1011 (2012).
23. Das, S., Chen, H. Y., Penumatcha, A. V. & Appenzeller, J. High performance multilayer MoS_2 transistors with scandium contacts. *Nano Lett.* **13,** 100 (2013).
24. Ganatra, R. & Zhang, Q. Few-layer MoS_2: A promising layered semiconductor. *ACS Nano* **8,** 4074 (2014).
25. Lee, Y. H. *et al.* Synthesis of large-area MoS_2 atomic layers with chemical vapor deposition. *Adv. Mater.* **24,** 2320 (2012).
26. Wu, W. *et al.* High mobility and high on/off ratio field-effect transistors based on chemical vapor deposited single-crystal MoS_2 grains. *Appl. Phys. Lett.* **102,** 142106 (2013).

27. Chen, M. C. *et al.* Hybrid Si/TMD 2D electronic double channels fabricated using solid CVD few-layer-MoS_2 stacking for V_{th} matching and CMOS-compatible 3DFETs. *IEDM Tech. Dig.* **808** (2014).
28. Kang, K. *et al.* High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature* **520,** 656 (2015).
29. Sun, S. C. & Plummer, J. D. Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces. *IEEE Trans. Electron Devices* **8,** 1497 (1980).
30. Cheng, C. F. *et al.* Very low V_t [Ir-Hf]/HfLaO CMOS using novel self-aligned low temperature shallow junctions. *IEDM Tech. Dig.* **333** (2007).
31. Liao, C. C. *et al.* Metal-gate/high-κ/Ge nMOS at small CET with higher mobility than SiO_2/Si at wide range carrier densities, *IEEE Electron Device Lett.* **34,** 163 (2013).
32. Chang, S. J. *et al.* Mobility behavior and models for fully depleted nanocrystalline ZnO thin film transistors. *Solid State Electronics* **90,** 134 (2013).
33. Bayraktaroglu, B. & Leedy, K. Self-assembled nanocrystalline ZnO thin film transistor performance optimization for high speed applications. *Turk J Phys* **38,** 375 (2014).

Acknowledgements

This paper's publication was supported in part by Ministry of Science and Technology of Taiwan. We would like to thank the computing time support from National Taiwan University of Science & Technology and National Center for High-performance Computing.

Author Contributions

C.W.S. did the experiments; A.C. supervised the experiments and wrote the main manuscript text; C.F.L. and W.F.S. did the quantum-mechanical calculations. All authors reviewed the manuscript.

Additional Information

Supplementary information accompanies this paper at http://www.nature.com/srep

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Wei Shih, C. *et al.* Remarkably high mobility ultra-thin-film metal-oxide transistor with strongly overlapped orbitals. *Sci. Rep.* **6**, 19023; doi: 10.1038/srep19023 (2016).