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# Reproducibility Data on SUMMiT

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## ABSTRACT

SUMMiT (Sandia Ultra-planar Multi-level MEMS Technology) at the Sandia National Laboratories' MDL (Microelectronics Development Laboratory) is a standardized MEMS (Microelectromechanical Systems) technology that allows designers to fabricate concept prototypes. This technology provides four polysilicon layers plus three sacrificial oxide layers (with the third oxide layer being planarized) to enable fabrication of complex mechanical systems-on-a-chip.

Quantified reproducibility of the SUMMiT process is important for process engineers as well as designers. Summary statistics for critical MEMS technology parameters such as film thickness, line width, and sheet resistance will be reported for the SUMMiT process. Additionally, data from Van der Pauw test structures will be presented.

Data on film thickness, film uniformity and critical dimensions of etched line widths are collected from both process and monitor wafers during manufacturing using film thickness metrology tools and SEM tools. A standardized diagnostic module is included in each SUMMiT run to obtain post-processing parametric data to monitor run-to-run reproducibility such as Van der Pauw structures for measuring sheet resistance.

This characterization of the SUMMiT process enables design for manufacturability in the SUMMiT technology.

Keywords: Microelectromechanical Systems; MEMS; Foundry; Surface Micromachining; Polysilicon mechanical structures

## 1. INTRODUCTION

SUMMiT is a four level polysilicon surface micromachining fabrication technology developed by Sandia National Laboratories in Albuquerque, New Mexico. Sandia National Laboratories utilizes the SUMMiT process for agile prototyping as part of the SAMPLES program. The SAMPLES program (Sandia Agile MEMS Prototyping, Layout Tools, Education and Services program) educates designers on the SUMMiT process, design and analysis tools, design rules and restrictions, and provides design submission instructions for participation in agile prototyping at Sandia National Laboratories*[2].

Each reticle field for SUMMiT consists of 9 modules as shown in Figure 1. Eight of these modules are available for designers. Module #7 is reserved for the standard set of diagnostic test structures and is considered the diagnostic module.

Run-to-run reproducibility on every SUMMiT lot is monitored by data acquired from the diagnostic module both during processing (visual inspections, SEM analysis, etc.) and post processing (electrical measurements). A sample diagnostic module is shown in Figure 2. In addition, monitor wafers are run with every film deposition for SUMMiT, and they are measured for film thickness and uniformity.

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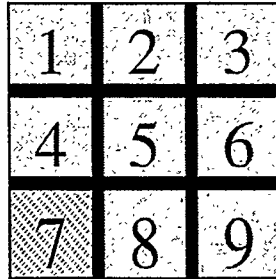document.**

**Figure 1.** SUMMiT reticle field. Module # 7 is the diagnostic module, and the other modules are available for designers. This reticle field is stepped 69 times across a 150 mm wafer.
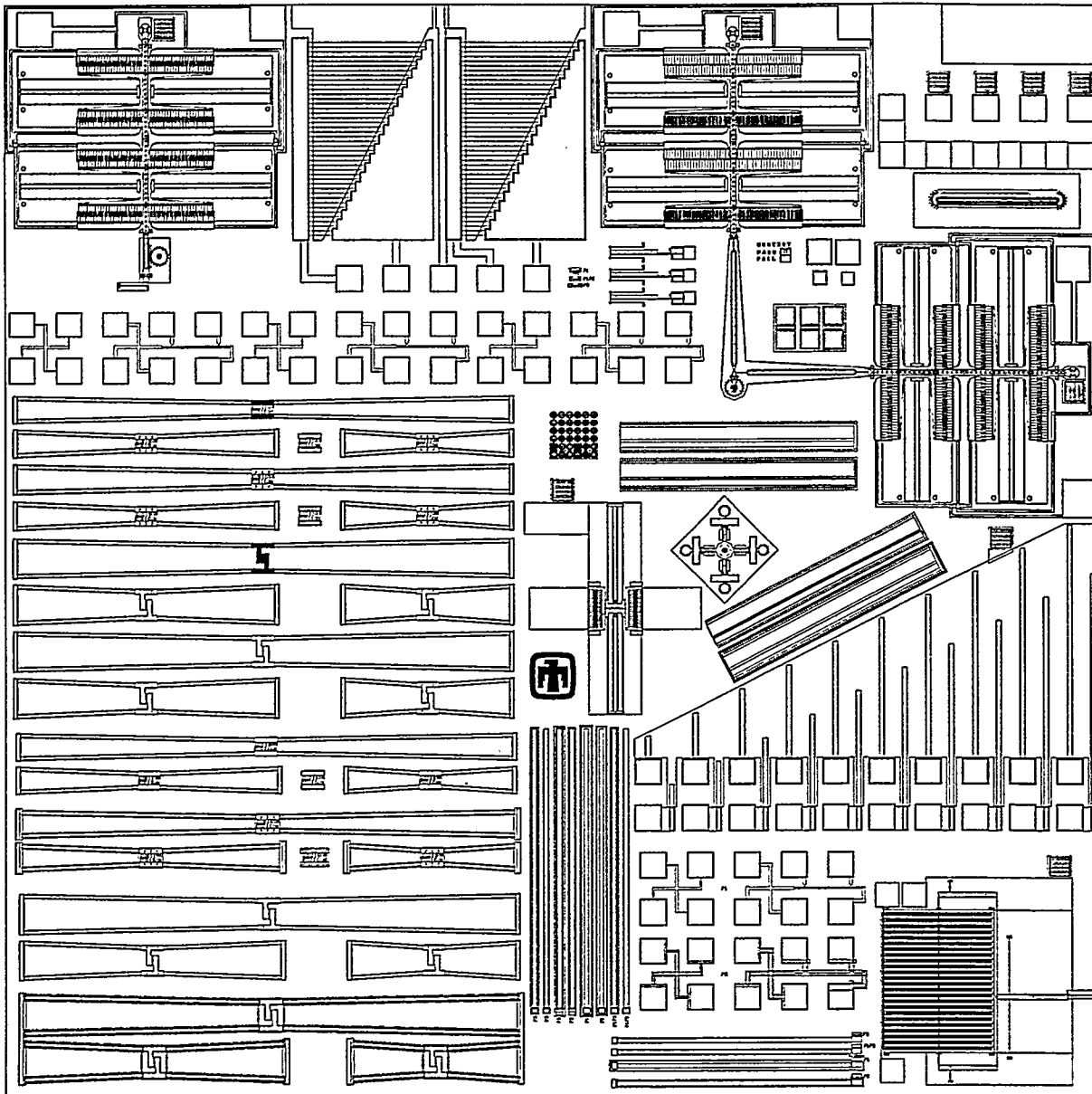


**Figure 2.** AutoCAD image of the diagnostic module, Module # 7. Sheet resistance data are measured from the Van der Pauw test structures of this module.

## 2. SUMMIT FILM THICKNESS

SUMMiT is unique in that it is the only MEMS foundry that offers three levels of structural polycrystalline silicon (poly), an electrical poly level that is isolated from the silicon substrate, and is fabricated using integrated circuit processing techniques. A cross-section showing each layer is provided in Figure 3 where the three structural polysilicon layers are called MMPoly1, MMPoly2, and MMPoly3, while MMPoly0 serves as a ground plane and is typically used for electrical interconnects.

The nitride / oxide layer provides electrical isolation of MMPoly0 from the substrate. During the final release, MMPoly0 and the silicon nitride layer protects the silicon dioxide from being etched. The three layers of sacrificial oxides (SACOX1, SACOX2, and SACOX3) are removed during the release to free the mechanical polysilicon structure.

The targeted thickness for each film is indicated in the figure and will be used as comparison with the measured thickness of the films. A cross section of an experimental SUMMiT wafer is shown in Figure 4 indicating the four poly layers.
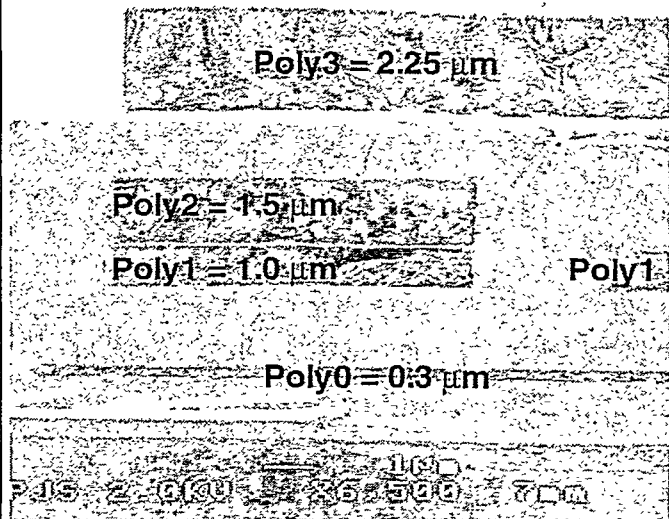


Figure 3. Cross-section of the SUMMiT process. There are 3 structural layers, 1 ground/interconnect layer, and 3 sacrificial oxide films.

Figure 4. A cross-sectional SEM (Scanning Electron Microscope) of an experimental wafer from SUMMiT.

### 2.1 Polysilicon Film Thickness (MMPoly0, MMPoly1, MMPoly2, MMPoly2/1 Laminate, and MMPoly3) Data

Here, the thickness of MMPoly0, MMPoly1, MMPoly2, MMPoly2/1 laminate, and MMPoly3 polysilicon films are reported. To illustrate the importance of film thickness, consider the deflection of a simple cantilever beam as shown in Figure 5 where P is the applied point load, L is the length of the beam, t is the thickness of the beam, and δ is the deflection of the beam.
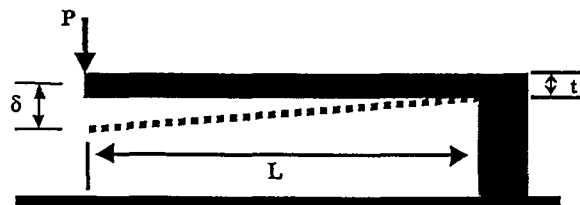


Figure 5. Perpendicular deflection of a cantilever beam with respect to the substrate. P = applied point load, L = the length of the beam, δ = deflection of the beam, t = thickness of the beam, and w = width of the beam (not indicated in figure).

The deflection of the beam[1] is given in Equation 1,

$$\delta = \frac{PL^3}{3EI}$$

(1)

where E is Young's Modulus and I is the area moment of inertia. For a deflection that is perpendicular to the substrate, $I_x$ is given in Equation 2 where t is the thickness of the beam and w is the width of the beam.

$$I_x = \frac{wt^3}{12}$$

(2)

Therefore, the deflection is a cubic function of the polysilicon film thickness implying high sensitivity to thickness variation. Referring to Figure 3 for the targeted poly thickness, the measured poly film thickness for 11 SUMMiT lots are shown in Figures 6, 7, 8, 9, and 10. Uniformity is defined as the standard deviation divided by the mean and multiplied by 100 to obtain a percentage.
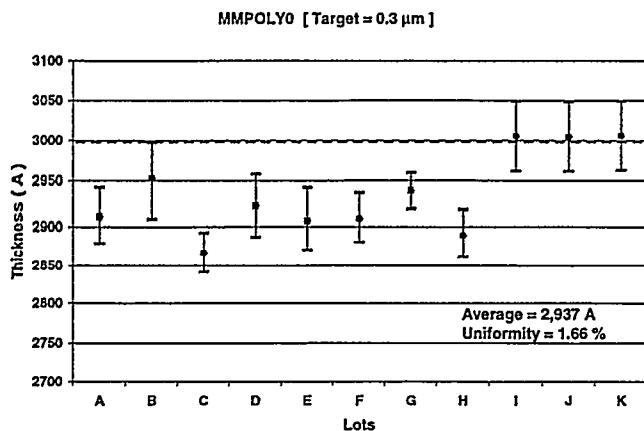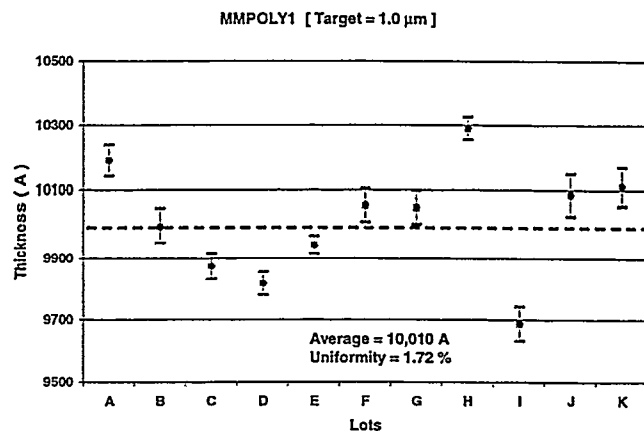
MMPOLY0 [ Target = 0.3 µm ]



Figure 6. Trend Chart for the thickness of the MMPoly0 layer. Error bars indicate one sigma variation of the three measured monitor wafers. The targeted thickness is 0.3 µm. For n = 11, the mean is 2937 Å, and the uniformity (1 σ) is 1.66 %.

MMPOLY1 [ Target = 1.0 µm ]



Figure 7. Trend Chart for the thickness of the MMPoly1 layer. Error bars indicate one sigma variation of the three measured monitor wafers. The targeted thickness is 1.0 µm. For n = 11, the mean is 10,010 Å, and the uniformity (1 σ) is 1.72 %.
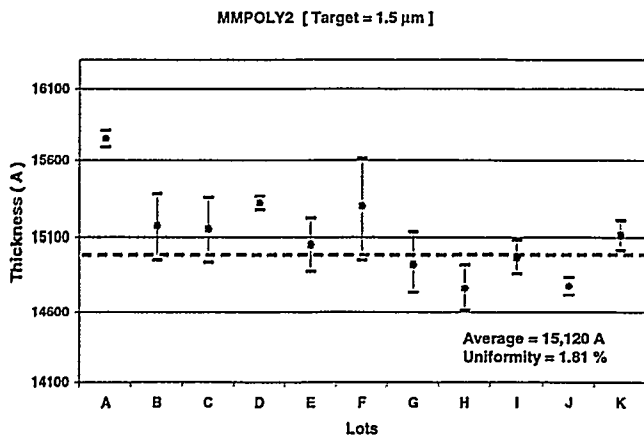
MMPOLY2 [ Target = 1.5 µm ]



Figure 8. Trend Chart for the thickness of the MMPoly2 layer. Error bars indicate one sigma variation of the three measured monitor wafers. The targeted thickness is 1.5 µm. For n = 11, the mean is 15,120 Å, and the uniformity (1 σ) is 1.81 %.

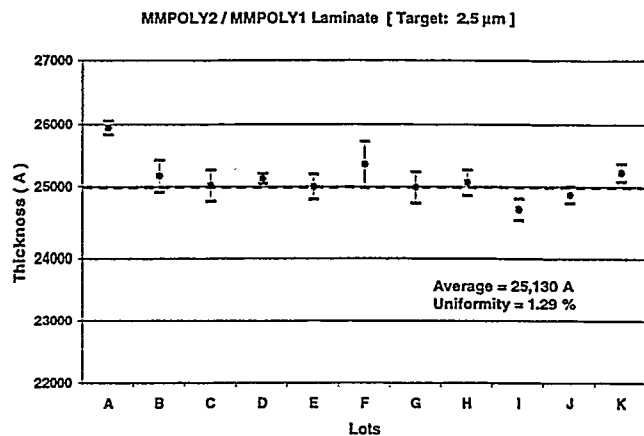MMPOLY2 / MMPOLY1 Laminate [ Target: 2.5 µm ]



Figure 9. Trend Chart for the thickness of the MMPoly2 / MMPoly1 laminate layer. Error bars indicate one sigma variation of the three measured monitor wafers. The targeted thickness is 2.5 µm. For n = 11, the mean is 25,130 Å, and the uniformity (1 σ) is 1.29 %.
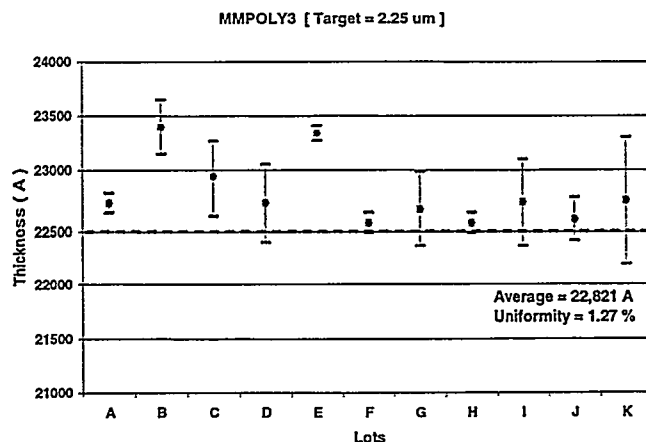
MMPOLY3 [ Target = 2.25 um ]



**Figure 10.** Trend Chart for the thickness of the MMPoly3 layer. Error bars indicate one sigma variation of the three measured monitor wafers. The targeted thickness is 2.25 μm. For n = 11, the mean is 22,821 Å, and the uniformity (1 σ) is 1.27 %.

Each poly film is deposited using a low pressure chemical vapor deposition (LPCVD) process. Film thickness and uniformity are recorded from three monitor wafers that are placed in a quartz boat during deposition. Process wafers are placed between these monitor wafers during deposition. After the deposition, the monitor wafers are annealed. The monitor wafers are next placed in metrology tools for measurements. Thick poly films (typical tool thickness range: <40 Å up to 4 microns) are measured in a Prometrix FT-650 spectrophotometer tool (accuracy within ± 1% of NIST certified range[ 1 σ ] thickness). Thin poly films (typical tool thickness range: <50 Å to 10,000 Å) are measured using a Rudolph Focus-3 ellipsometer tool (thickness accuracy: = ± 3Å at 500, 1000, 2000 Å).

The as-deposited polysilicon film stress is compressive, and after the anneal, the stress is minimal (less than 15 MPa)[2]. The stress relief mechanism is due to a volume contraction when the amorphous film recrystallizes into a polycrystalline state[2,3]. For SUMMiT, there are preliminary data[4] indicating that the Poly3 film is slightly compressive at approximately -3 MPa. Also, we have observed that the residual stress for the MMPoly2/MMPoly1 laminate stack is slightly tensile at approximately +2 MPa.

## 2.2 Sacrificial Oxide Film Thickness (SACOX1, SACOX2, and SACOX3) Data

Here, the thickness of the SACOX1, SACOX2, and SACOX3 layers are reported. An example of the importance of the thickness of the SACOX layers would be the fabrication of a parallel plate capacitor. The capacitance of a parallel plate capacitor[5], C, is shown in Equation 3 where ε is the permittivity of the dielectric, A is the area of each plate, and t is the separation between plates, or equivalently the SACOX thickness.

$$C = \varepsilon \frac{A}{t}$$
(3)

As with the polysilicon films, each sacrificial oxide film is deposited using LPCVD processes except for SACOX3. Again, monitor wafers (placed at the top, center, and bottom) of the quartz boat are measured. The monitor wafers are measured directly after deposition using a Prometrix SpectraMap for SACOX1 and the Rudolph ellipsometer for SACOX2.

The thickness presented in Figures 11 and 12 are for SACOX1 and SACOX2 as-deposited films.
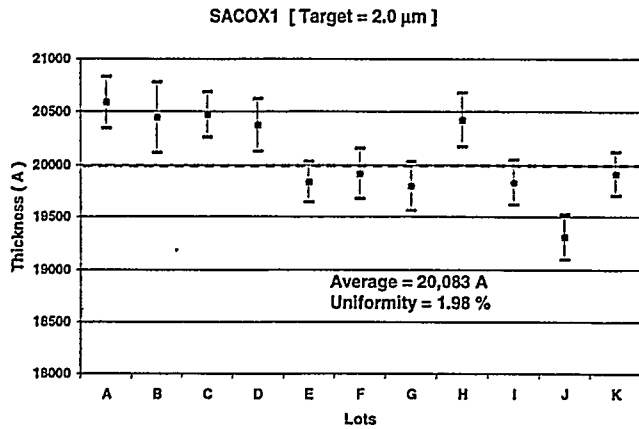
**SACOX1 [ Target = 2.0 µm ]**

**SACOX2 [ Target = 0.5 µm ]**

**Figure 11.** Trend Chart for the thickness of the SACOX1 layer. Error bars indicate one sigma variation of the three measured monitor wafers. The targeted thickness is 2.0 µm. For n = 11, the mean is 20,083 Å, and the uniformity (1 σ) is 1.98 %.
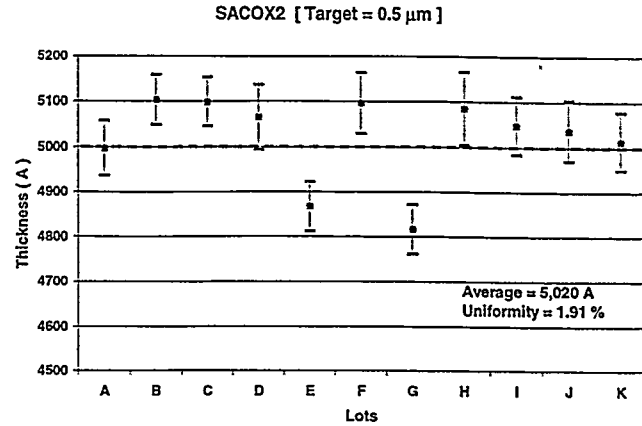
**Figure 12.** Trend Chart for the thickness of the SACOX2 layer. Error bars indicate one sigma variation of the three measured monitor wafers. The targeted thickness is 0.5 µm. For n = 11, the mean is 5,020 Å, and the uniformity (1 σ) is 1.91 %.

In the case of SACOX3, the thickness variation from lot-to-lot is slightly greater due to pattern density effects during planarization by CMP (Chemical-Mechanical Polishing). In general, narrow features that are isolated planarize quicker than wide, high-density patterns[6]. Variations caused by pattern density for SUMMiT are generally ± 0.3 µm. Recently implemented, ellipsometer test structures are being utilized to record the thickness immediately after CMP.

The post-planarization thickness of SACOX3 is a function of which films are below it in the stack. The thickness reported is represented by the stack shown in Figure 3. In another case, the test structure cross section shown in Figure 13 represents the thickest case for SACOX3. SACOX3 is the thickest where a SACOX3 anchor etch down to the MMPoly2 layer is allowed (valid for designs that pass the SUMMiT Design Rule Checker). The SUMMiT design rule checker (DRC) provides SUMMiT designers with design rules (width, spacing, and overlap) to prevent designs from causing process related problems. The rules are determined by the resolution and registration of photolithography, selectivity of etches, underlying topography (to prevent stringer formation), and necessity to anchor structures during the release etch (to prevent "floaters"). For this case, we are trying to prevent floaters during the release etch by allowing MMPoly3 to anchor to MMPoly2. Since the oxide is thickest here, the SACOX3 anchor etch down to MMPoly2 is timed accordingly to etch through the entire film. Thickness data acquired from these new test structures will be reported in the future. The SUMMiT anchor etch is sufficiently overetched to compensate for SACOX3 variations in order to provide a suitable anchor between MMPoly3 and MMPoly2 (within the SUMMiT design rules).

Preliminary measured data indicates that the SACOX3 thickness above a MMPoly2 / MMPoly1 laminate stack similar to Figure 13 but with MMPoly0 present is ~ 2.0 µm.



| SACOX3 | ~ 2.3 µm (CMP) |
|---|---|
| MMPoly2 | 1.5 µm |
| MMPoly1 | 1.0 µm |
| SACOX1 | 2.0 µm |
| Silicon Nitride | 0.80 µm |
| Silicon Dioxide | 0.63 µm |
| Silicon Wafer | |

**Figure 13.** SACOX3 thickness above a valid set of films. SACOX3 immediately before MMPoly3 deposition for this case is 2.3 ± 0.3 µm.

## 2.3 Thermal Oxide / Low Stress Nitride Film Thickness Data

The thickness of the thermal oxide (or silicon dioxide as labeled in Figure 3) and low stress nitride is reported here. The thermal oxide and low stress nitride films are used to isolate MMPoly0 from the substrate. The low stress nitride layer is required in addition to the thermal oxide layer because the nitride layer protects the thermal oxide layer during the long release wet etch in a HF rich solution. As with the sacrificial oxide layers, the thermal oxide and low stress nitride layer thickness are important in the calculation of capacitance (in this case, parasitic capacitance).

The thickness presented in Figures 14 and 15 are for the thermal oxide and the low stress nitride layers.
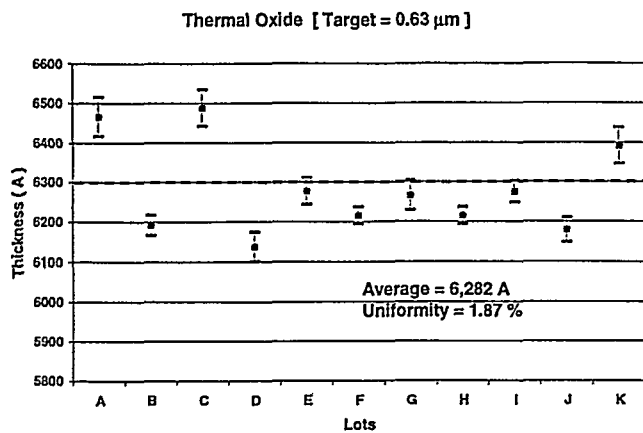
**Thermal Oxide [ Target = 0.63 µm ]**

**Low Stress Nitride [ Target = 0.8 µm ]**

**Figure 14.** Trend Chart for the thickness of the thermal oxide layer. Error bars indicate one sigma variation of the three measured monitor wafers. The targeted thickness is 0.63 µm. For n = 11, the mean is 6,282 Å, and the uniformity (1 σ) is 1.87 %.
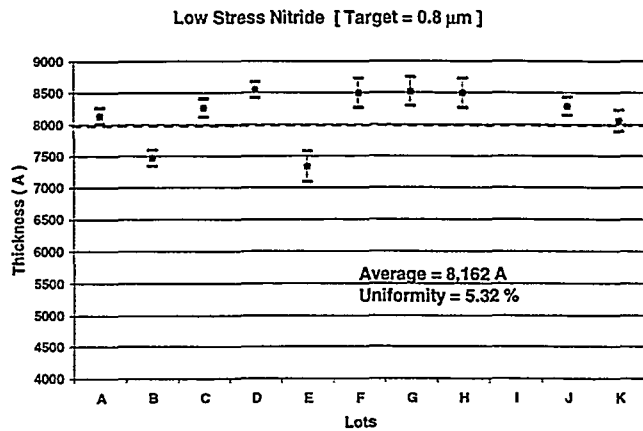
**Figure 15.** Trend Chart for the thickness of the low stress nitride layer. Error bars indicate one sigma variation of the three measured monitor wafers. The targeted thickness is 0.5 µm. For n = 10, the mean is 8,162 Å, and the uniformity (1 σ) is 5.32 %.

## 3. SHEET RESISTANCE

The sheet resistance is important, for example, to make conductive poly pads for probing. The sheet resistance for each poly layer is measured post-process after the release etch. The Van der Pauw test structure that is used is shown in Figure 16. The sheet resistance data are shown in Figures 17, 18, 19, 20, and 21.
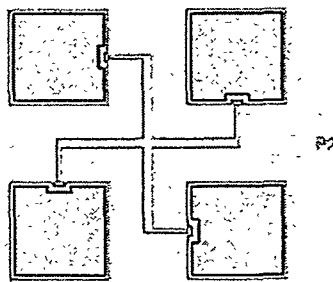
**Figure 16.** Van der Pauw test structure for measuring sheet resistance.
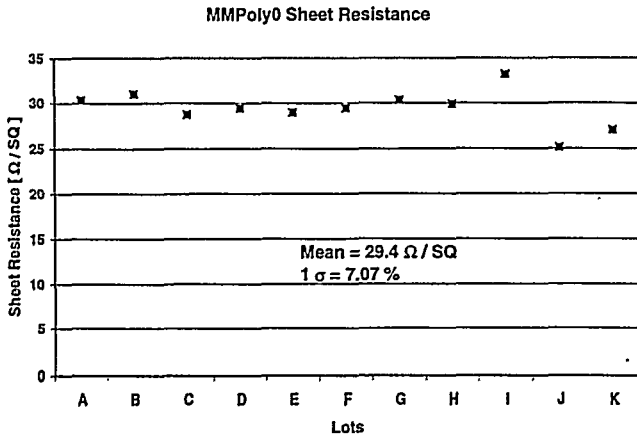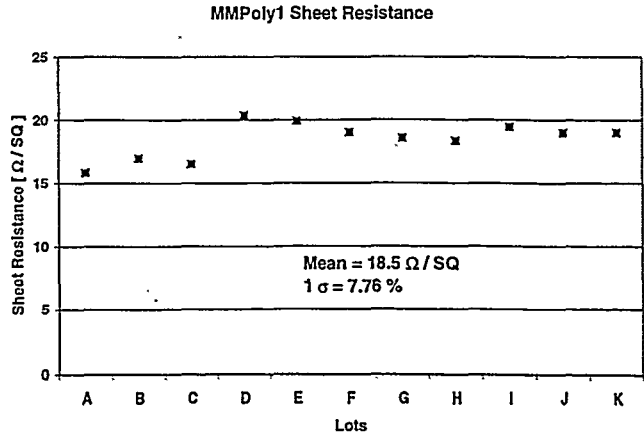
**MMPoly0 Sheet Resistance**



**Figure 17.** Trend Chart for the MMPoly0 layer sheet resistance. Each plotted point is the average sheet resistance from at least two measured sites. For the 11 SUMMiT lots (n = 11), the mean is 29.4 $\Omega$ / SQ, and 1 $\sigma$ is 7.07 %.

**MMPoly1 Sheet Resistance**



**Figure 18.** Trend Chart for the MMPoly1 layer sheet resistance. Each plotted point is the average sheet resistance from at least two measured sites. For the 11 SUMMiT lots (n = 11), the mean is 18.5 $\Omega$ / SQ, and 1 $\sigma$ is 7.76 %.
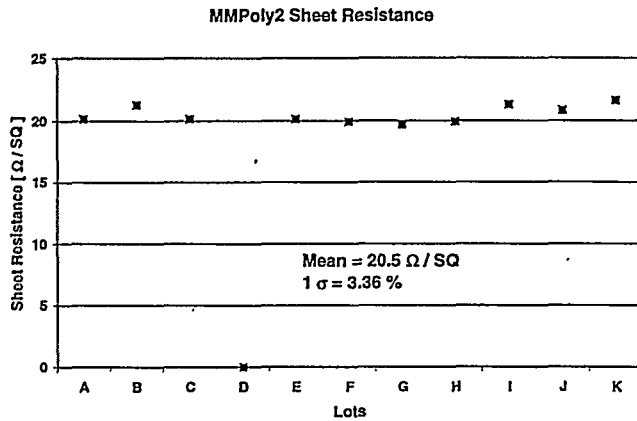
**MMPoly2 Sheet Resistance**



**Figure 19.** Trend Chart for the MMPoly2 layer sheet resistance. Each plotted point is the average sheet resistance from at least two measured sites. For the 10 SUMMiT lots (n = 10), the mean is 20.5 $\Omega$ / SQ, and 1 $\sigma$ is 3.36 %.

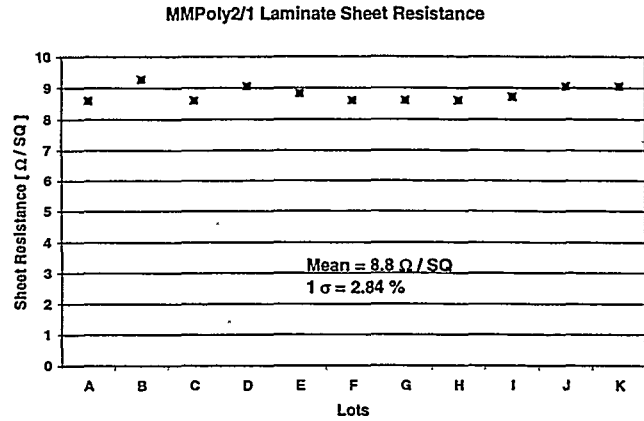**MMPoly2/1 Laminate Sheet Resistance**



**Figure 20.** Trend Chart for the MMPoly2/1 laminate layer sheet resistance. Each plotted point is the average sheet resistance from at least two measured sites. For the 11 SUMMiT lots (n = 11), the mean is 8.8 $\Omega$ / SQ, and 1 $\sigma$ is 2.84 %.
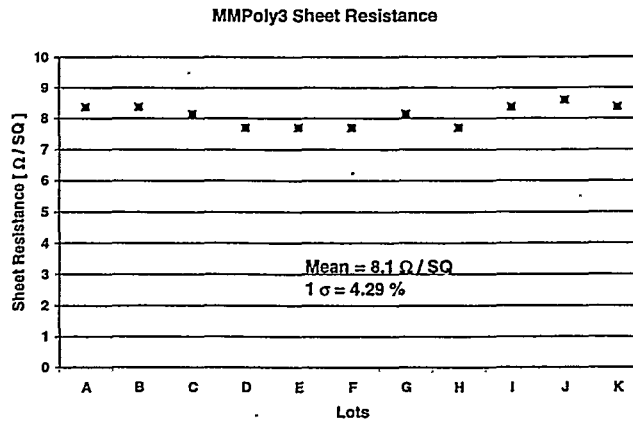
**MMPoly3 Sheet Resistance**



**Figure 21.** Trend Chart for the MMPoly3 layer sheet resistance. Each plotted point is the average sheet resistance from at least two measured sites. For the 11 SUMMiT lots (n = 11),, the mean is 8.1 $\Omega$ / SQ, and 1 $\sigma$ is 4.29 %.

The sheet resistance, $R_s$, for a conductor is shown in Equation 4 where $\rho$ is the specific resistivity and t is the thickness of the conductor. The resistivity for a n-type semiconductor is shown in Equation 5 where q is the electron charge ($1.60 \times 10^{-19}$ C), and $N_d$ is the impurity doping concentration. Phonon scattering and ionized impurity scattering are the two scattering mechanisms that dominate in a semiconductor an room temperature[7]. For single crystal Si at T = 300° K, the intrinsic electron mobility in silicon is $\mu_n$ = 1350 cm$^2$ / V-sec.

$$R_s = \frac{\rho}{t} \tag{4}$$

$$\rho = \frac{1}{q\mu_n N_d} \tag{5}$$

In polysilicon, two mechanisms cause the resistivity of doped polysilicon to be higher than doped silicon (except at very high dopant concentrations): 1) dopants such as P segregate to the grain boundaries where they do not produce free carriers, and 2) grain boundaries are abundant with incomplete bonds, which traps some free carriers thereby decreasing mobility[8].

If the non-idealities are neglected and assumming complete ionization of the impurity atoms, then Equations 4 and 5 could be used to roughly approximate the impurity doping concentrations in the polysilicon films to be in the order of $10^{18}$ -- $10^{19}$ cm$^{-3}$ with electron mobilities ranging from 200 to 500 cm$^2$ / V-sec. Since electron and hole mobilities are a function of the impurity concentrations, $\mu_n$ and $N_d$ are unknowns, a trial and error approach was used with the electron and hole mobilities versus impurity concentrations figures as reported by Sze[9]. Again, the data is an approximation neglecting the effects of grain boundaries.

## 4. LINEWIDTHS

The linewidth is important for devices that are actuated in-plane. The area moment of inertia for the cantilever beam $I_y$ as shown in Figure 22 is given in Equation 6. Therefore, the deflection in this case (see Equation 1) is a cubic function of the width of the cantilever beam. Linewidth variations could strongly affect the calculated deflection.
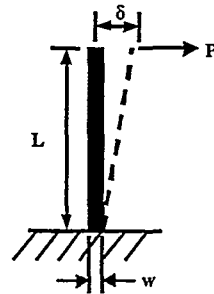


Figure 22. Deflection of a cantilever beam parallel to the substrate. P = applied point load, L = the length of the beam, $\delta$ = deflection of the beam, t = thickness of the beam (not indicated in figure), and w = width of the beam.

$$I_y = \frac{w^3 t}{12} \tag{6}$$

For a line defined in AutoCAD for SUMMiT reticles, 0.05 μm is loss per edge on the photoresist due to an exposure bias in photolithography. This bias (or overexposure) is intended to provide SUMMiT with flexibility caused by topography inherent with MEMS fabrication.

The trend charts presented in Figures 23 and 24 are for the MMPoly2/1 laminate and MMPoly3 linewidths. The linewidths are measured using the Hitachi S-6000 CD SEM (down to 2 μm pitch ± 0.010 μm).

**MMPoly2/1 Laminate Line Width [ Target = 1.8 μm ]**



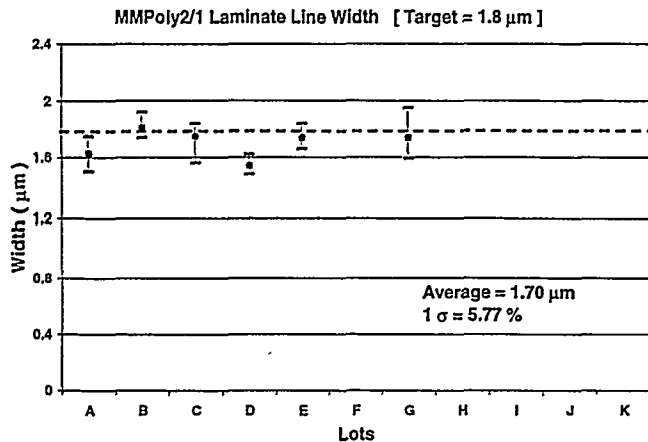**MMPoly3 Line Width [ Target = 2.0 μm ]**



**Figure 23.** Trend Chart for the line width of the MMPoly2/1 laminate layer. Error bars indicate the range of the two measured process wafers per lot. Missing data for lots are intentionally omitted because the line widths of the omitted lots were measured at different sites with different line widths. The targeted line width is 1.8 μm. For n = 6, the mean is 1.70 μm, and 1 σ is 5.77 %.
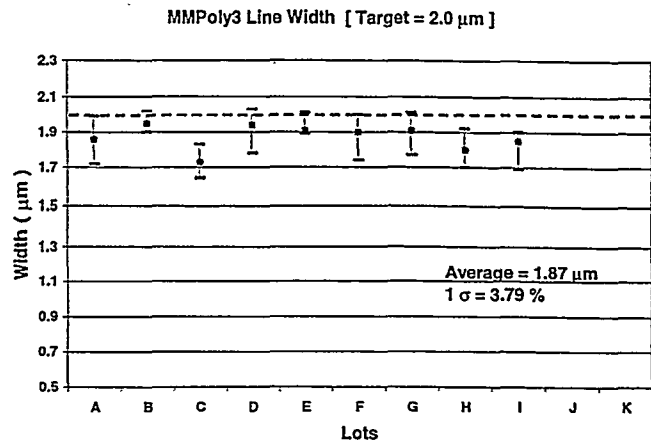
**Figure 24.** Trend Chart for the line width of the MMPoly3 layer. Error bars indicate the range of the two measured process wafers per lot. Missing data for lots are intentionally omitted because the line widths of the omitted lots were measured at different sites with different line widths. The targeted line width is 2.0 μm. For n = 9, the mean is 1.87 μm, and 1 σ is 3.79 %.

## 5. CONCLUSIONS

Important data such as film thickness, sheet resistance, line width, and resonant frequency have been reported. The average thickness and uniformity for MMPoly0, MMPoly1, MMPoly2, MMPoly2 / MMPoly1 laminate, and MMPoly3 are 2,937 Å (1.66 %), 10,010 Å (1.72 %), 15,120 Å (1.81 %), 25,130 Å (1.29 %), and 22,821 Å (1.27 %) respectively. The average thickness and uniformity for SACOX1, SACOX2, thermal oxide, and silicon nitride layer are are 20,083 Å (1.98 %), 5,020 Å (1.91 %), 6,282 Å (1.87 %), and 8,162 Å (5.32 %) respectively. The average sheet resistance and 1 σ variation for MMPoly0, MMPoly1, MMPoly2, MMPoly2 / MMPoly1 laminate, and MMPoly3 is 29.4 Ω / SQ (7.07 %), 18.5 Ω / SQ (7.76 %), 20.5 Ω / SQ (3.36 %), 8.8 Ω / SQ (2.84 %), and 8.1 Ω / SQ (4.29 %) respectively. The average measured line width and 1 σ variation at the bottom of the line of the MMPoly2 / MMPoly1 laminate and MMPoly3 layer is 1.70 μm (5.77 %) for a specified 1.8 μm line and 1.87 μm (3.79 %) for a specified 2.0 μm line respectively.

With this data in hand, MEMS engineers should be able to have a better understanding of their device performance prior to designing in the SUMMiT process.

For future work, we would like to report data from our other test structures.

## 6. ACKNOWLEDGEMENTS

## 7. REFERENCES

1. Gere & Timoshenko, *Mechanics of Materials, Third Edition*, PWS Publishing Company, 1990.
2. L. Ristic, F. A. Shemansky, M.L. Kniffin, and H. Hughes, *Sensor Technology and Devices*, "Chapter 4: Surface Micromachining Technology", Artech House, Boston, 1994.

3.  H. Guckel, J. J. Sniegowski, T. R. Christenson, "Fabrication of Micromechanical Devices from Polysilicon Films with Smooth Surfaces", *Sensors & Actuators*, **20**, pp. 117 – 122, 1989.
4.  B. D. Jensen, M. P. de Boer, S. L. Miller, "IMaP: Interferometry for Material Property Measurement in MEMS," IModeling and Simulation of Microsystems 1999, San Juan, Puerto Rico, April 19-21, 1999, pp. 206-209.
5.  H. D. Young, *University Physics, Eighth Edition*, Addison-Wesley Publishing Company, New York, 1992.
6.  D. L. Hetherington, J. J. Sniegowski, "Improved polysilicon surface-micromachined micromirror devices using chemical-mechanical polishing," International Symposium on Optical Science, Engineering, and Instrumentation, SPIE's 43rd Annual Meeting, San Diego, CA, July 22, 1998.
7.  D. A. Neamen, *Semiconductor Physics and Devices*, Richard D. Irwin, INC., Boston, Massachusetts, 1992.
8.  S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era, Volume 1 – Process Technology*, Lattice Press, California, 1986.
9.  S. M. Sze, *Physics of Semiconductor Devices, 2$^{nd}$ Edition*, Wiley-Interscience, New York, 1981.