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Reproducible memory effect in the leakage current of epitaxial ferroelectric/conductive perovskite heterostructures

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Leakage currents in epitaxial ferroelectric/perovskite-conductor heterostructures reproducibly show diode properties having hysteresis. The hysteresis appears in forward bias, which is positive for electron (n) type conductors and negative for hole (p) type conductors. The hysteresis is due to the increase of conductivity by the forward bias current, which exhibits the memory retention for more than an hour. The write and erase speeds of the diode and the origin of the effect are discussed. © *1995 American Institute of Physics.*

Carrier conduction through dielectrics or insulators, especially SiO_2, has been investigated by many authors.[1,2] Dielectric perovskite oxide films are expected to be used in the future in ultralarge scale integrate circuits such as dynamic random access memory.[3–6] In spite of its high dielectric constant, the perovksite dielectric is reported to show leakage current much larger than Si oxide. The leakage current is less evident in polycrystalline films than in quasiepitaxial films,[3] probably due to carrier trapping at grain boundaries, while it was much reduced in amorphous films.[4]

The conduction mechanism as well as other electric properties of dielectric perovskites have been discussed using films grown on metal electrode such as Pt.[3–6] However, transmission electron microscopy observations have revealed the existence of various disorders at the interface between the perovskite and the bottom metal electrode.[6] Recently, growth of epitaxial ferroelectric perovskite films on perovskite conductors was reported.[7] Due to its ability to reduce the disorders, we have applied this approach to re-examine basic properties of ferroelectric (or dielectric) perovskite films.[8] In this letter, we report on the conductive behaviors of epitaxial ferroelectric films of high crystallographic quality as well as on the first observation of reproducible memory effect in the leakage current at room temperature (RT). The result is compared with a similar memory effect observed at 4.2 K which was attributed to the modulation of the tunneling probability.[9]

$BaTiO_3$ (BTO) and $Pb_{1-y}La_yZr_{1-x}Ti_xO_{3\pm\delta}$ ($x=0-0.5$, $y=0-0.1$) (PLZT) films were epitaxially grown on (100) $SrTiO_3$ (STO) and (100) $SrTiO_3$ doped with 0.5 wt % Nb (STO:Nb) substrates and on $La_{2-x}Sr_xCuO_4$ (LSCO), $LaNiO_3$, (La,Sr) MnO_3, and $Nd_{2-x}Ce_xCuO_4$ (NCCO) films which were epitaxially grown on (100) STO. Details of surface morphology and crystallographic properties of the heterostructures using STO, STO:Nb, and LSCO as well as their deposition conditions are described elsewhere.[8,10] The heterostructures were grown mostly *ex situ* by a pulse laser deposition, because no quantitative difference in leakage current was observed between *in situ* and *ex situ* grown heterostructures. The thicknesses of the conductive layer and the ferroelectric layer were typically around 1000 and 2000 Å, respectively. The x-ray $\theta/2\theta$ scan showed that all heterostructures were c-axis oriented with strong diffraction intensity comparable to single crystals, and the x-ray pole figure showed that all layers were aligned inplane to the a axis of the substrate. No secondary phases were detected by the depth profile using Auger electron spectroscopy and x-ray diffractometry. Au electrodes with a surface area of 1 mm^2 were deposited on the heterostructures and the current-voltage (I-V) characteristics were measured by applying a dc voltage across the heterostructure where the conductive layer or the substrate was grounded. No *qualitative* difference was observed when Al films were used as an electrode instead of Au films. First, we present the results of the $Pb_{0.9}La_{0.1}Zr_{0.2}Ti_{0.8}O_3/La_{1.9}Sr_{0.1}CuO_4$ heterostructure.

Figure 1 shows typical hystereses at RT of PLZT/LSCO heterostructure obtained from 26 runs, where the voltage was first increased from zero, then decreased to the minimum, and subsequently increased to zero in each run in about 7 min. Each data point was obtained by averaging 5 data acquisitions in 2 s, where a waiting time of 0.3 s was introduced in each data acquisition to avoid an artificial hysteresis. Data in 4 runs of the total of 26 runs, which are the first 3 runs and 1 run just after a pause of 2 h, are indicated by dots, and the rest of data are shown by larger marks. The observed reproducibility indicted that the hystereses were not a consequence of insulator breakdown as in SiO_2 on Si. Equally reproducible I-V hystereses were found in PLZT/STO:Nb systems. On the other hand, the I-V hystereses observed in (PLZT+impurity phases)/Si structure were neither

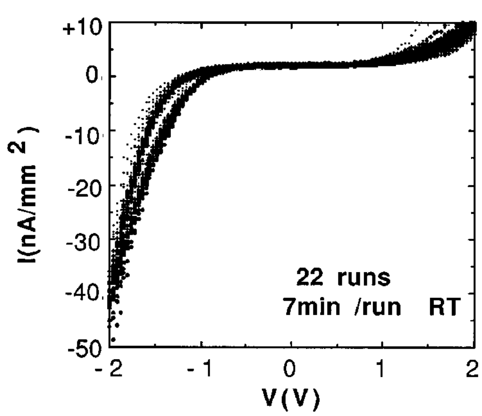

FIG. 1. I-V hystereses of 26 measurements, where data in 4 measurements before stabilization are shown by dots.

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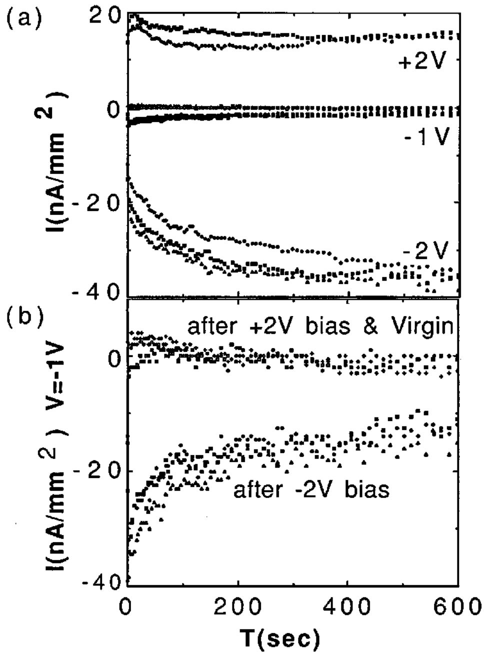

FIG. 2. (a) and (b) Time dependence of the diode currents at $V=-2$, -1, and $+2$ V (a) and its blow-up (b).

well defined nor reproducible. The I-V curve in Fig. 1 suggests that the large forward bias switched the diode to an on state and the large reverse bias returned the diode to an off state.

Figure 2(a) and 2(b) show the time dependence of the leakage current at fixed voltages (I-t curve), which clearly demonstrates the switching and the memory effects. In this measurement, constant biases of -1, -2, -1, $+2$, and -1 V were successively applied for 10 min at each bias as illustrated in Fig. 3(a). Here, the bias of -1 V can be regarded as a *read* bias. The I-t curves in three sets of such measurements are shown in Fig. 2(a). The conductivity was enhanced

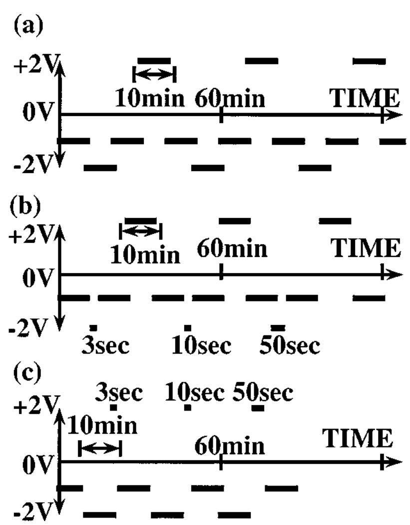

FIG. 3. Illustration of the bias application sequences used in Fig. 2(a), in the write speed test (Fig. 4) (b) and in the erase speed tests (c).

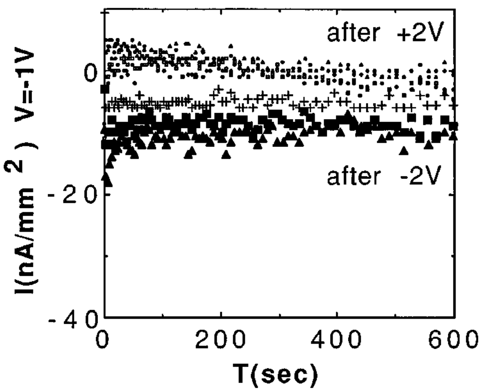

FIG. 4. I-t relations for different duration of the write biases (-2 V) and a fixed duration of the erase bias ($+2$ V). The currents after -2 V biases for 3, 10, and 50 s are indicated by +, ■, and ▲, respectively. The currents after $+2$ V biases are indicated by the small symbols.

reproducibly by the bias of -2 V and restored to the original value by the bias of $+2$ V as shown in Fig. 2(b) which is the blow-up of Fig. 2(a). The memory retention under the constant -1 V bias was estimated to be more than 1 h.

The I-t curves were measured by changing the duration of a bias of -2 V as shown in Fig. 3(b) to estimate the *write* speed and by changing the duration of a bias of $+2$ V as shown in Fig. 3(c) to estimate the *erase* speed. In the *write* test, the conductivity of the on state increased as the duration of the *write* bias increased, and it approached a saturated value at the duration of 50 s (Fig. 4). In the *erase* test, however, the conductivity at $V=-1$ V was the same as the value before the *write* bias (<2 nA/mm^2) and independent of the duration of the *erase* bias. Therefore, the *erase* speed is estimated to be less than a second.

It should be noted that the relaxation of the dipole moment and the trapping and detrapping of the carrier at the interface can apparently contribute to the current. However, the former was excluded since it could only explain for 1/10–1/100 of the total current at the *read* bias when integrated over the time. The latter was also excluded since the trapped carrier density was estimated from the data in Fig. 2(b) to be more than one carrier per area of 10 Å×10 Å and to be one per 1 Å×1 Å for some of other samples. Therefore, the I-V characteristic was analyzed using the mathematical models for typical conduction processes in insulators.[1] The strong temperature dependence observed by us excludes the tunneling mechanism. Moreover, we could not observe a reproducible I-V hysteresis in our heterostructures at 4.2 K. We think that our memory effect and that reported by Tamura *et al.*[9] are different phenomena. No model is available that can fit all the I-V characteristics observed in all systems studied. This is probably due to the different conduction mechanisms governing the ultralow leakage range (<0.1 nA/mm^2), the low leakage range (<100 nA/mm^2), and the high leakage range (1–10 μA/mm^2. Figure 5 shows a *replot* of one set of data of Fig. 1, which suggests that the Schottky emission was responsible for the conduction in the low leakage region as suggested for the $SrTiO_3$ film sandwiched by Pt.[5]

We have observed diodelike I-V characteristics and hys-

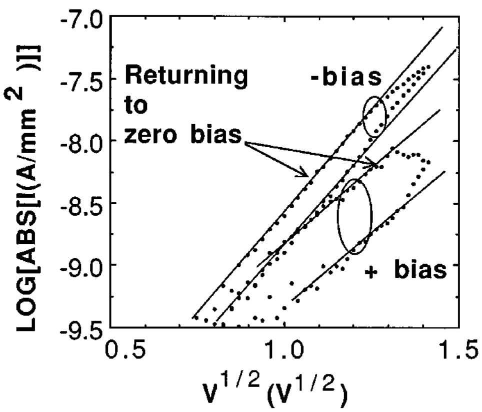

FIG. 5. Schottky plot of I-V relation in Fig. 1. The bars are guidance to the eye.

tereses in all heterostructures mentioned above, unless samples were leaky. The result can be summarized as follows: (1) Larger hysteresis appeared in the forward direction of the diode. (2) The polarity of the forward direction was positive for conductive layers having n-type carriers (NCCO, STO:Nb) and negative for those having p-type carriers (LSCO, $LaNiO_3$). This polarity dependence was observed to be opposite in few samples having large leakage current or to change after damage by large biases, but the I-V characteristics were not reproducible in these cases. (3) The higher the current at the forward bias, the larger the hysteresis. But the magnitude of hysteresis hardly depended on the magnitude of the bias voltage itself. (4) The reproducibility of hysteresis was better in samples with a good insulating property. (5) The I-V characteristics depended on the scan speed. (6) No qualitative differences were observed in the I-V characteristic in heterostructures having different ferroelectric materials. Further, the hysteresis was observed even if the ferroelectric layer did not show any trace of ferroelectric hysteresis at the voltage applied in the I-V measurement (e.g., BTO on STO:Nb).

Among the above results, especially, the slow *write* speed, and the insensitivity to the ferroelectric property and the bias voltage suggest that the memory effect is not a consequence of a change of the band structure caused by the ferroelectric switching of the polarization. The ions in the perovskite conductors including cuprates are known to be mobile, which was also suggested by a persistent photoconductivity[11] attributed to rearrangement of the oxygen. Therefore, a possible origin of the present memory effect may be electrically driven rearrangement or migration of ions at the interface which changes the Schottky barrier height as suggested by the parallel shift o the I-V curve after the *write* and the *erase* biases in Fig. 5, where the change of the barrier heights is estimated to be 18 meV for the negative bias and 31 meV for the positive bias. The temperature dependence, a more detailed analysis, and the conduction mechanisms will be reported elsewhere.

In conclusion, a novel memory effect was reported for leakage current in ferroelectric/conductive perovskites heterostructures at RT.

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