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Research on Characteristics of Audio DAC Sigma-Delta Modulator on Field Programmable Gate Array

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Introduction

The article describes a powerful digital audio digital-to-analogue converter (DAC) realized on field programmable gate arrays (FPGA). This allows managing without an analogue sound signal track and avoiding all accompanying problems in a personal computer sound system as in a sound card a digital signal is usually converted into an analogue signal and amplified by outside amplifiers. FPGAs help to achieve such project flexibility that one can finally explore dependency of sound signal quality parameters on a DAC's structure. Moreover, it becomes possible to realize the whole sound signal-processing scheme on one chip. This could be a variant of an application specific integrated circuit (ASIC).

The article presents the architecture of designed DAC on FPGA, results of an interpolator and a modulator modelling, as well as assessment of experimental research characteristics.

DAC architecture on FPGA

The structure of the offered DAC on FPGA is given in Fig. 1. It combines the following: an USB controller, an interpolator and a modulator both realized on the FPGA, a 1-bit DAC and an analogue low frequency filter.

A FPGA constitutes the main part of a DAC wherein realization of noise shaping loop (NSL) takes place when the main part of noise is being transferred into frequencies beyond the diapason which we are interested in. Its impact on a signal is that of a low frequency filter, whereas on quantization noise – that of a high frequency filter. This is performed by the Sigma Delta modulator. Opal Kelly XEM3001 was used as a prototype, which has not only a FPGA but also an USB controller.

An interpolator is needed in order to increase frequency of samples and suppress all side images between the main band and $OSR \cdot f_S$. This will improve the dynamic range of NSL (in our case – of ΣΔ modulator) and decrease the requirements of an analogue output filter.

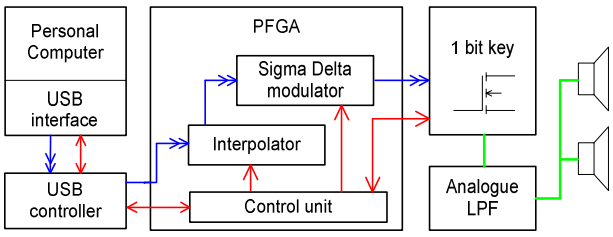

Fig. 1. Simplified structure of DAC on FPGA

The 1-bit key produces an analogue output changing from $-V_{supply}$ to $+V_{supply}$ out of logic levels changing in the interval 0÷3.3 V. The node was realized employing the TI TAS5152 chip. As the lowpass filter – a passive second-order LC filter. Its task is to pass the sound diapason and suppress higher frequencies. The filter is designed with MicroCap 7.14 programme.

The system will work exclusively on a specific programme which has a plugin written for it.

During the development of Winamp plugin the C language and National Instruments LabWindows programming package were used. Previously the Labview was used for a programme prototype, which is very comfortable when adjusting and synthesizing a microprogram on FPGA. Several programmes were developed in the Labview environment. The plugin was rewritten in the C language.

Simulation of interpolator

The simulation was performed with Matlab/Simulink package having integrated Xilinx System Generator and Xilinx ISE, and with Modelsim SE package. The major part of the FPGA resources are occupied not by Sigma Delta modulator but by the interpolator.

Fig. 2 presents the structural scheme of an audio interpolator, which is sometimes referred as an interpolational filter.

The finite input response (FIR) filter – of a low frequency halfband. The type of the design – equirripple. The search of the filter coefficients involved the use of the

Matlab fdatool, whereas for its implementation Xilinx ISE was used, applying the CORE Generator and combing all these in the low level. In this way the FPGA resources were spared because otherwise, when an attempt was made to realize in the high level using the Xilinx System Generator package, it was found out that such process would use almost one and a half times more systemic resources.

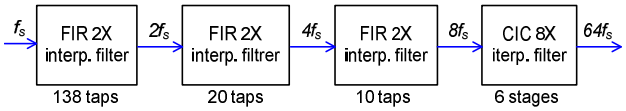

Fig. 2. Structure of the interpolator

The FIR filters multiplier-accumulator (MA) structure was rejected for two reasons:

1. Tests showed that MA filters required the Block RAM memory – only in this way their advantage was manifested against distributed-arithmetic (DA) filters.

2. Designed filters are of halfband, thus they could be realized enough effectively using also the DA structure. The structure spares accumulators that are indispensable in case of realization the modulator.

Characteristics of an 138th order magnitude response is given in Fig. 3. It is apparent that the quantization of coefficients barely had any influence.

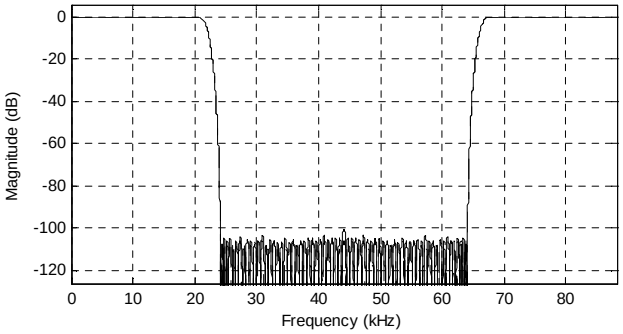

Fig. 3. Magnitude response of the 138th order FIR filter

Taking into consideration hardware resources, a CIC (Cascaded Integrator-Comb) is an effective interpolation or decimation filter, which is usually used in FPGAs. The structure of a filter is illustrated in Fig. 4. In case of an interpolator, firstly N differentiators then zeroes and finally N integrators are inserted.

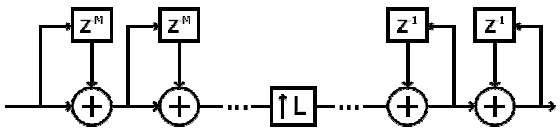

Fig. 4. Structure of CIC filter

After completion of the modelling, it was determined that requirements were met best by CIC filter with the amplitude transmission characteristics as shown in Fig. 5. Having chosen from parameters given, we reached a compromise between suppression of side images (as poles are selected inside of the images), small hardware resources (only 6 stages) and the low side throughput band suppression (see Fig. 6).

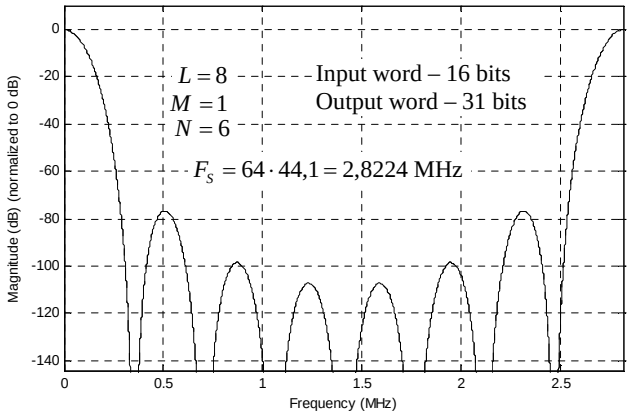

Fig. 5. Magnitude response of the CIC filter

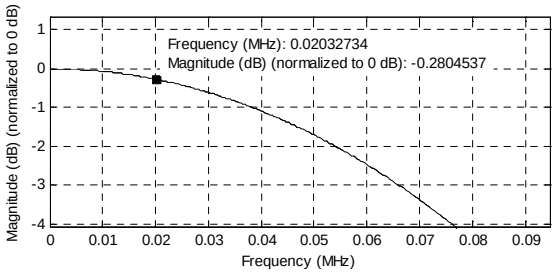

Fig. 6. Suppression of the CIC filter at the passband limit

Judging from the characteristics, it is evident that CIC imposes quite a considerable influence on the passband – CIC suppresses it. It often requires introducing compensation of the passband. However, as in this case the use is made of a small enough interpolation multiplier, the small suppression received remains satisfactory. Moreover, the use of an analogue Chebyshev filter in the output once again brings everything back into order.

The general characteristics of an interpolator signal transfer in the frequency range from 0 to $F_d/2$ is given in Fig. 7. The rounding of the characteristics in the area of the suppression range beginning is caused by the use of the Backman window.

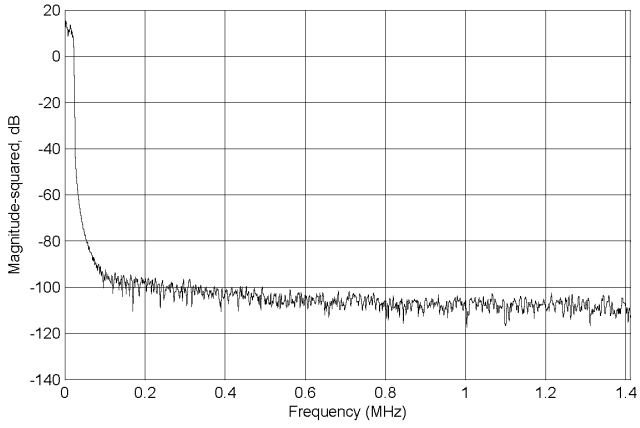

Fig. 7. Signal transfer characteristic of the interpolator

In order to decrease hardware resources, in all filters, where the need for the zero insertion occurs, not the zero but the preceding sample is being inserted. This constitutes the condition for improvement of filtrated characteristics.

Research on characteristics of modulator

The first stage in designing a ΣΔ modulator involves a synthesis of the noise transfer function (NTF). It was performed by way of application of [1] and selection of the output parameters:

1. The quantizer will be of 1 bit as the DAC design will be relatively powerful. A modulator of this kind is characterized by a greater linearity [2].

2. To increase the coefficient of efficiency, the discretization frequency should be:

$F_S = 44{,}1 \cdot 64 = 2{,}8224$ MHz

3. As music in computers is quantized with 16-bit words, the effective number of bits (ENOB) will be 16 [3].

4 Parameters of the modulator will be: OSR = 64 (over sampling ratio), N = 5 (modulator order).

After the synthesis of the primary NTF, next step is to select a CRFB (Cascade-of-resonators, feedback form) modulator structure and calculate the coefficients of the modulator.

A dynamic-range scaling was performed. The coefficients were then recalculated into the ABCD array. The array was then scaled and again recalculated into coefficients. The maximum level of the stable output was 0,56.

Fig. 8 presents the efficient signal and noise transmission functions calculated from the scaled ABCD array. The dependency of the signal noise ratio on the output signal level is showed in Fig. 9.

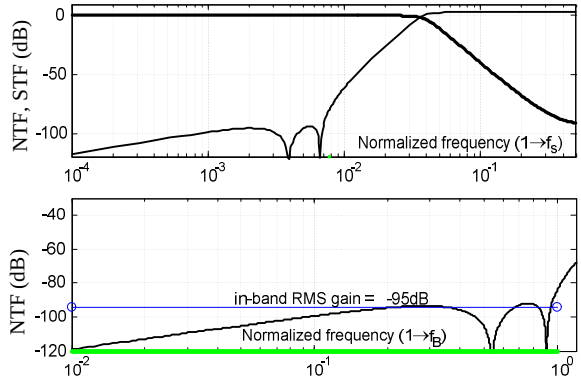

Fig. 8. Signal and noise transfer functions

Taken that the quantization noise power is $\sigma_e^2 = 1/3 = -4{,}8$ dB, then the quantization noise power shaped in the passband is:

$$\sigma_q^2 = \sigma_H^2 \sigma_e^2 / OSR = -95 - 4{,}8 - 10\log(64) \cong -118 \text{ dB}.$$

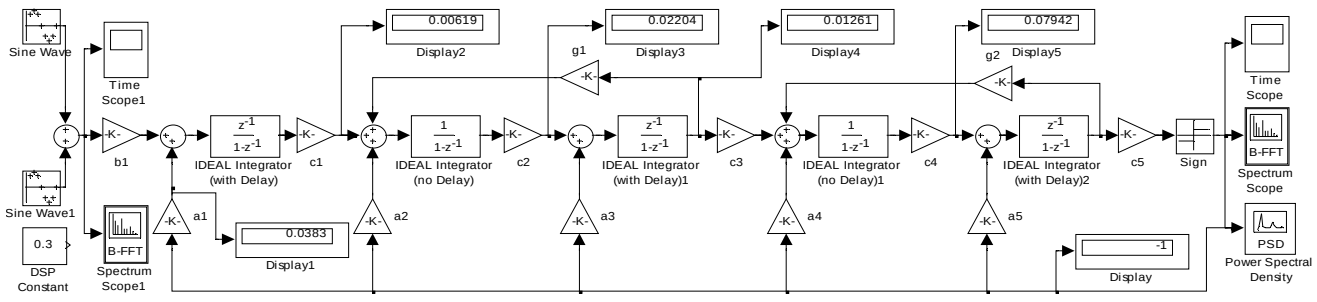

Fig. 11. 5th order Sigma-Delta modulator

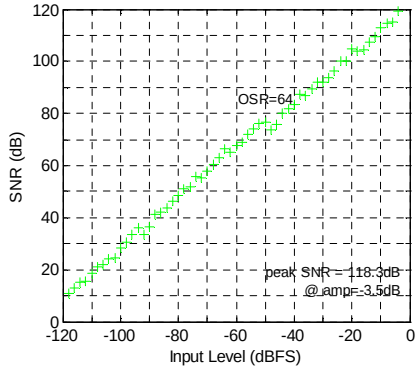

Fig. 9. Signal-to-noise ratio

Fig. 10 presents an output signal spectrum when a half-amplitude sinus signal operates in the input.

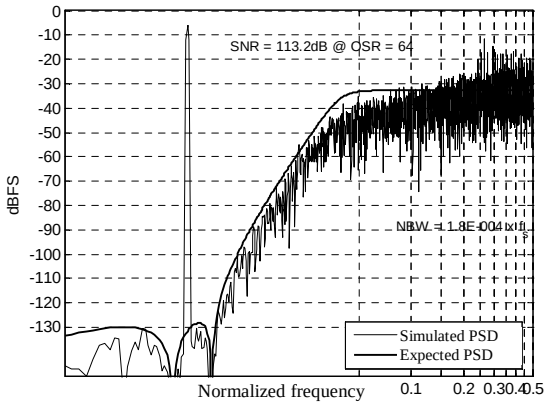

Fig. 10. Output power spectral density

The next step employed *SD Toolbax* 2 of Matlab. Although the real structure was modeled, in this case operations are performed with floating point numbers. A 5th order CRFB type Sigma Delta modulator is illustrated in Fig. 11. The modulator's output signal spectral density, after passing two sinus tones into the input, is given in Fig. 12. As can be seen from the latter graphical chart, when the sound signal frequency band was of 20 kHz, the modulator's effective number of bits was 16.

The Xilinx System Generator was employed in aggregating the ΣΔ modulator for the purpose of an experimental research. Then it was modeled again and exported into VHDL. The VHDL description as a black box was then imported into Simulink and the functionality was tested by yet another modeling before realization on the FPGA.

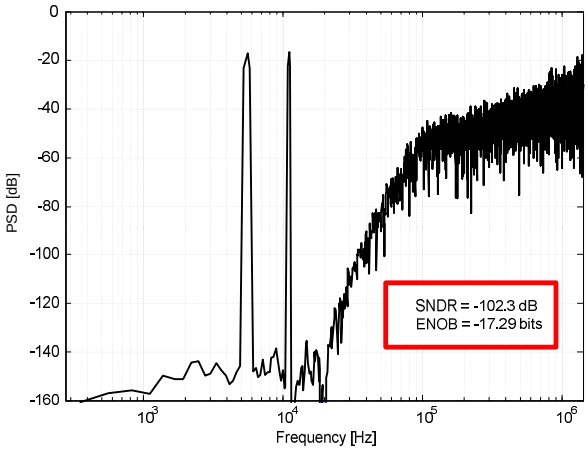

Fig. 12. Power spectral density

A two-channel DAC was realized on the Xilinx Spartan XC3S400-4PQ208 FPGA. Number of occupied slices was 3.464. Thus the result of the research was not worse than [4].

Conclusions

1. The architectural scheme of a designed audio Sigma Delta DAC on the FPGA whose application in a computer sound system allows sparing an analogue sound track and improving the sound quality was presented.

2. After modelling the audio interpolator filters transmission characteristics and the Sigma Delta modulator's quantization noise parameters, it was determined that requirements are met best by the CIC filter amplitude frequency characteristics when the interpolation multiplier is L = 8, the number of stages is N = 6, the input word length is 16 bits, the output word length is 31 bits, and the sampling frequency is 2.8224 MHz.

3. The results of the modulator modelling showed that when a sound signal frequency band is of 20 kHz the modulator's effective number of bits is 16, while the quantization noise power is minus 118dB. The modelling results are also proven by the experimental digital sound system research.

References

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V. Puidokas, A. J. Marcinkevičius. Research on Characteristics of Audio DAC Sigma-Delta Modulator on Field Programmable Gate Array // Electronics and Electrical Engineering. – Kaunas: Technology, 2008. – No. 5(85). – P. 97–100.

The original architectural scheme of a designed audio Sigma Delta DAC on the FPGA whose application in a computer sound system allows refusing of an analogue sound track and improving the sound quality is presented. Modelling results of the audio interpolator filters transmission characteristics and the Sigma Delta modulator's quantization noise parameters are given. It was determined that requirements are met best by a CIC filter amplitude frequency characteristics when the interpolation multiplier is L=8, the number of stages is N = 6, the input string length is 16 bits, the output string length is 31 bits, and the discretization frequency is 2.8224 MHz. The results of the modulator modelling showed that when a sound signal frequency band is of 20 kHz the modulator's effective number of bits is 16, while the quantization noise power is minus 118dB. The modelling results are also proven by the experimental research when a DAC has been realized with Xilinx Spartan XC3S400-4PQ208 on the array. Ill. 12, bibl. 4 (in English; summaries in English, Russian and Lithuanian).

В. Пуйдокас, А. И. Марцинкявичюс. Исследование характеристик аудио сигма – делта АЦП модулятора на программируемой логической матрице // Электроника и электротехника. – Каунас: Технология, 2008. – № 5(85). – С. 97–100.

Предсавлены результаты моделирования и исследования оригинальной аудиосистемы, в основу которой заложено Сигма-Дельта ЦАП на программируемой логической матрице. Применение данной системы позволяет в звуковом тракте компьютера аналоговую часть (кроме выходного усилителя) заменить цифровым блоком и этим улучшить качество звука. Представлены характеристики фильтров интерполятора и параметры шума Сигма-Дельта модулятора. Установлено, что наилучшие требования к амплитудно-частотной характеристике CIC фильтров удалетворяют параметры: коэффициент интерполяции L = 8, количество ступеней N = 6, длина цифрового слово 16 битов и частота дискретизации 2,8224 МГц. Исследование модулятора показало, что при полосе частот звукового сигнала 20 кГц, число эффективных разрядов – 16 мощность шума квантования минус 118 дБ. Экспериментальное исследование на Xilinx Spartan XC3S400-4PQ208PL подтвердило результаты моделирования системы. Ил. 12, библ. 4 (на английском языке; рефераты на английском, русском и литовском яз.).

V. Puidokas, A. J. Marcinkevičius. Garso moduliatoriaus Sigma-Delta SAK su lauku programuojama logine matrica charakteristikų tyrimas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2008. – Nr. 5(85) – P. 97–100.

Pateikta originali garso moduliatoriaus Sigma Delta SAK su LPL matrica (*angl*. FPGA) sandaros schema, kurią naudojant kompiuterio garso sistemoje galima atsisakyti analoginio garso trakto ir pagerinti garso kokybę. Pateikti garso interpoliatoriaus filtrų perdavimo charakteristikų ir Sigma Delta moduliatoriaus signalo ir triukšmo parametrų modeliavimo rezultatai. Nustatyta, kad geriausiai reikalavimus tenkina pakopinio diferenciatorių integratorių (*angl*. CIC) filtro dažninė amplitudės charakteristika, kai interpoliacijos daugiklis L = 8, pakopų skaičius N = 6, įėjimo žodžio ilgis – 16 bitų ir diskretizacijos dažnis – 2,8224 MHz. Moduliatoriaus tyrimo rezultatai parodė, kad, esant garsinio signalo dažnio juostai 20 kHz, efektyvus bitų skaičius – 16, kvantavimo triukšmo galia minus 118 dB. Modeliavimo rezultatus patvirtina ir eksperimentinis tyrimas, kai SAK realizuotas Xilinx Spartan XC3S400-4PQ208PL LPL matricoje. Il. 12, bibl. 4 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).