Research on High Efficiency and High Density 48 V-5 V Multi-Resonant Switched Capacitor Converter

Zhuxuan TIAN, Yueshi GUAN, Wei WANG, and Dianguo XU

Abstract—**Multi-resonant switched capacitor converter can make efficient use of active and passive components, and has two characteristics of high efficiency and highly power density. Therefore, we propose a 9∶1 cascaded multi-resonant switched capacitor converter and further explore ways to improve the performance of the converter in this paper. On the one hand, by analyzing the coupling relationship between the first and second circuit topology, we propose a method to reduce the intermediate decoupling capacitance. On the other hand, by adjusting the dead time of the control signal, the zero-voltage switch (ZVS) of most switching devices is realized, and the efficiency of the converter is improved. Therefore, a 48 V–5 V resonant converter prototype with rated power of 120 W, power density of 330 W/in^3, peak efficiency of 98.1% and maximum output current of 23.7 A is designed in this paper. From 20% to full load, the efficiency is always maintained at more than 92% (including driving loss), and most of the loss is reflected in the conduction path, reflecting great optimal space and application potential.**

Index Terms—**Data center, multi-resonance, resonant converter, switched capacitor.**

I. Introduction

With the continuous development of computing science, the amount of user data through cloud servers is also increasing, which promotes the continuous expansion of the capacity of data centers. For data centers, the increase in capacity will directly lead to a significant increase in power consumption [1]. Therefore, the optimization of data center power system has also become an important link in the development process of computing science. Generally speaking, the optimization of the power system is nothing more than improving its overall working efficiency, which is mainly reflected in two aspects: one is to improve the conversion efficiency of the converter itself, and the other is to reduce the loss of energy in the transmission path. It is also required that the converter can be placed as close as possible to the power supply chip to shorten the energy transmission path [2]. In order to achieve this purpose while avoiding the influence on the normal operation of the chip due to the installation of the power supply, the volume of the power supply system needs to be as small as possible. Therefore, high efficiency and high power density have also become two major requirements for the future development of data center power supply systems.

In response to the above two requirements, Google proposed a 48 V bus architecture, which is expected to be applied to the next generation of data centers. The core idea of the 48 V bus architecture is to reduce the 48 V voltage to the point-of-load voltage, and this process often requires an intermediate bus converter and a voltage regulator (VR) [3], [4]. The voltage level of the intermediate bus converter is usually set to 12 V. But the intermediate voltage of 12 V tends to cause greater stress to the first-stage point-of-load (PoL) converter to reduce voltage to 1 V [5]. Therefore, this paper proposes a multi-resonant switched capacitor converter with a step-down ratio of 9∶1 to achieve a lower intermediate voltage of 5 V. The converter could not only reduce the pressure of the first-stage converter but also achieve the two requirements of high efficiency and high power density at the same time.

Scholars had explored a number of step-down topologies from 48 V to intermediate bus voltages in past few years. One of the typical converters is the Buck converter, but the Buck converter contains an output inductance, which often limits the further improvement of the converter's power density. Another type of typical converters is LLC resonant converter, which has two advantages: high step-down ratio and electrical isolation. But the converter contains a transformer, which makes the design process complex, low power density and high cost [6], [7].

Among passive components, capacitors have extremely high energy density [8], so capacitor-based resonant switched capacitor topologies have received more and more attention in recent years. In this type of converter, most of the energy is transferred through the capacitor, so the energy transfer rate is faster and the power density is higher. By introducing an inductance, an LC resonant cavity is formed to realize soft switching. So, resonant switched capacitor converter can achieve high efficiency while satisfying high power density.

Fig. 1 shows the proposed multi-resonant switched capacitor circuit topology with a step-down ratio of 9∶1. The voltages labeled in the Fig. 1 represent the voltage ratings of the resonant capacitors. The topology adopts a two-stage structure. The stage

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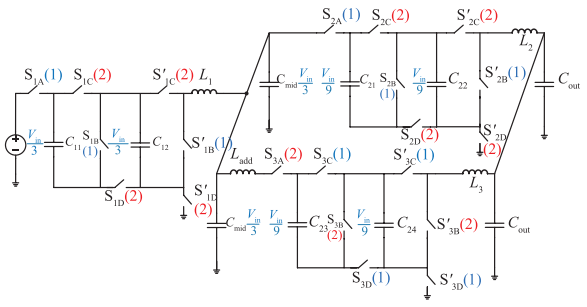


Fig. 1. A 48-to-5 V multi-resonant switched capacitor converter.

is a single-phase 3∶1 converter to reduce the voltage stress on the input side. The second stage is a two-phase 3∶1 converter in parallel to reduce the current stress on the output side. At the same time, power inductors are introduced at the output terminals of all stages to realize LC resonance and make all switching devices zero current switching (ZCS). Then, by adjusting the driving signal, the ZVS of most of the switching is realized and the overall efficiency is improved [9], [10]. At the coupling of the two stages, the interleaved operation of the second stage and the synchronous resonance method make the two stages work in a semi-coupled mode, which reduces the decoupling capacitance value and further improves the power density [11], [12].

This paper proposes a new 9∶1 multi-resonant switched capacitor converter, which can realize the ZCS of all switches and the ZVS of most of the switches through the reasonable parameter design, with extremely high working efficiency (peak efficiency of 98.1%) and power density (330 W/in^3).

II. Working Principle

A. Resonance Analysis

The working principle of the multi-resonant switched capacitor converter is shown in Fig. 1. As mentioned, it can be regarded as a cascade of two basic switched capacitor with a step-down ratio of 3∶1. Meanwhile, the converter can also be regarded as a switched capacitor with a step-down ratio of 9∶1, in which the soft charging of the capacitor is realized by adding an inductor. As shown in Fig. 2, due to the influence of resonance, the current presents a sinusoidal pulsation, and the switch turns off when the current resonates to zero. So all switches can achieve ZCS.

Without considering the realization of ZVS, the control signal is a group of square waves with 33% duty cycle and complementary phase. The switches of the cascaded multi-resonant switched capacitor converter can be divided into two groups according to the control signal. And the two groups of switches work in a complementary form. Therefore, the converter operates in two working modes as shown in Fig. 3 during the normal working process. In each working mode, the capacitor will be LC quasi-resonant with the inductor after being equivalent in series and parallel to achieve ZCS.

In the first mode, there are a total of 3 resonators, C_{11} and C_{12} are connected in series with L_1 to series resonate, C_{21} and C_{22} are connected in series with L_2 to series resonate, and C_{23}

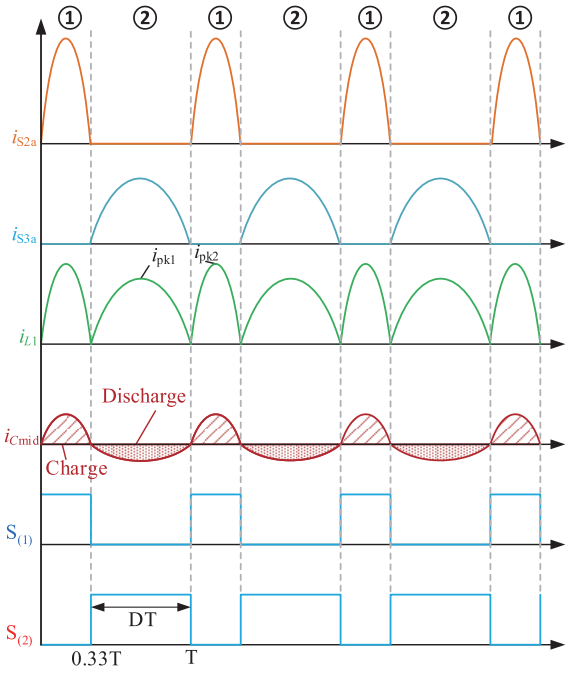


Fig. 2. Working waveform of multi-resonant switched capacitor converter.

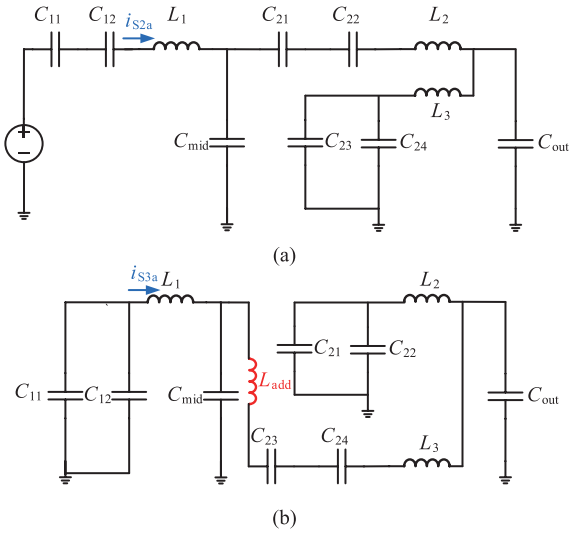


Fig. 3. Operating modes of multi-resonant switched capacitor converters.

and C_{24} are series resonated with L_3. Therefore, according to the series resonance calculation formula, the following three resonance frequencies can be obtained

$$\begin{cases} f_1 = \dfrac{1}{2\pi\sqrt{L_1 \dfrac{C_{11}C_{12}}{C_{11}+C_{12}}}} \\ f_2 = \dfrac{1}{2\pi\sqrt{L_2 \dfrac{C_{21}C_{22}}{C_{21}+C_{22}}}} \\ f_3 = \dfrac{1}{2\pi\sqrt{L_3(C_{23}+C_{24})}} \end{cases}. \tag{1}$$

In the same way, we can also obtain the resonance frequencies corresponding to the three resonant cavities of the second mode by performing the resonance analysis on the second mode.

$$\begin{cases} f_1' = \dfrac{1}{2\pi\sqrt{L_1(C_{11}+C_{12})}} \\ f_2' = \dfrac{1}{2\pi\sqrt{L_2(C_{21}+C_{22})}} \\ f_3' = \dfrac{1}{2\pi\sqrt{(L_3+L_{\text{add}})\dfrac{C_{23}C_{24}}{(C_{23}+C_{24})}}} \end{cases} \tag{2}$$

By controlling the on and off time of the switch, the state converts when the current resonates to the zero, thereby creating the ZCS condition and reducing the switching loss. At the same time, due to the existence of the inductance, the capacitor can achieve automatic voltage equalization during the charging and discharging switching process, realize soft-charging, and reduce energy loss.

B. Cascaded Structure Analysis

For a traditional cascaded resonant converter, a sufficiently large intermediate capacitor C_{mid} is required to realize the decoupling between the first stage and the second stage. The intermediate capacitor needs taking up too much space and using too many components during board fabrication. Therefore, by reducing the intermediate decoupling capacitance, the power density of the resonant converter can be further improved and the cost can be reduced.

In order to achieve the above goals, this work adopts an interleaved parallel structure. S_{2A} and S_{3A} in the second stage are complementary conductive. And part of the current flowing into the decoupling capacitor is transferred to the second stage. Therefore, under the interleaved parallel, the first and second stage operate in a semi-coupled state, which reduces the decoupling requirements. So, it can use smaller decoupling capacitors to ensure the normal operation of the circuit.

On this basis, if the ZCS of all switches are realized, it is necessary to ensure that each unit in the topology is in a quasi-resonant state in each operating mode. The current is just resonant for half a cycle to zero at this time. Therefore, in the same mode, the resonant frequencies corresponding to the first and second stages of the circuit are exactly equal, it can be seen that: $f_1 = f_2 = f_3$, $f'_1 = f'_2 = f'_3$. In order to facilitate subsequent parameter design, here we set $C_{23} = C_{24}$, $C_{11} = C_{12} = C_{21} = C_{22}$. Bringing them into (1) can get

$$\begin{cases} L_1 = L_2 \\ L_1 C_{11} = 4L_3 C_{23} \end{cases}. \tag{3}$$

By observing the expression forms of f_1 and f'_1, it can be directly obtained:

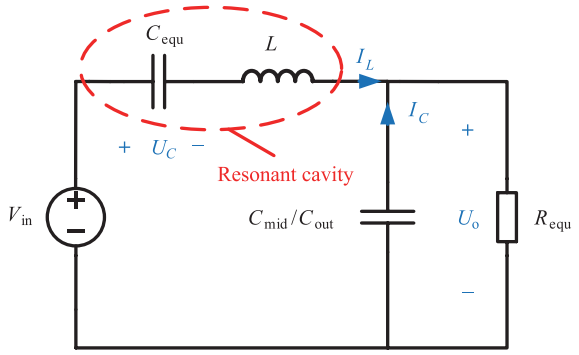


Fig. 4. Simplified schematic diagram of resonant switched capacitor converter.

$$f_1 = 2f'_1. \tag{4}$$

It should also be noted that in mode 2, the resonant frequency of the resonant cavity containing L_3 is reduced due to the reduced equivalent capacitance. Therefore, it is necessary to add an additional inductor L_{add} as shown in Fig. 3(b) before S_{3A} to meet the resonant frequency condition without affecting the normal operation of the first mode:

$$(L_3 + L_{\text{add}})C_{23} = 4L_2C_{21}. \tag{5}$$

Bringing (3) into (5) can be further simplified: $L_{\text{add}} = 15L_3$.

C. Decoupling Capacitor Selection

For a converter with a general two-stage structure, the larger the decoupling capacitance is, the more conducive it is to eliminate the mutual interference between the two stages. And it is more conducive to the normal operation of the circuit topology. However, as mentioned in the previous section, with the increase of the decoupling capacitor, the corresponding physical volume also increases, which adversely affects the power density and cost of the converter. Therefore, in this work, the selection principle of the decoupling capacitor is to improve the overall power density and reduce the manufacturing cost as much as possible. It could select the minimum value of the decoupling capacitor on the basis of satisfying the basic working requirements of the circuit.

The circuit topology shown in Fig. 4 can be obtained by disassembling and simplifying each 3∶1 basic step-down unit in the topology shown in Fig. 1. Among them, C_{equ} is the equivalent capacitance participating in the main resonance in the basic step-down unit; L is the resonant inductance of each unit; R_{equ} is the equivalent impedance of the subsequent circuit; the value of V_{in} changes according to the different circuit modes (When resonant capacitors are connected in parallel, $V_{\text{in}} = 0$ V; When resonant capacitors are connected in series, $V_{\text{in}} = 48$ V).

In order to ensure the normal operation of the circuit, for the decoupling capacitor, the maximum value of the charge that the capacitor can hold should be greater than the amount of charge flowing into the capacitor due to the mismatch between the first and second stages in a single cycle. Therefore, in order to calculate the amount of charge flowing into the capacitor,

it is necessary to obtain the instantaneous value of the current in the first and second stages. In this work, the current is equal to the inductor current. The equation of state for the circuit is shown in Fig. 4.

$$\begin{cases} \dfrac{\mathrm{d}I_L}{\mathrm{d}t}L + U_C + U_\mathrm{O} = V_\mathrm{in} \\ \dfrac{\mathrm{d}U_C}{\mathrm{d}t}C = I_L \\ I_L = -\dfrac{\mathrm{d}U_\mathrm{O}}{\mathrm{d}t}C + \dfrac{U_\mathrm{O}}{R} \end{cases} \tag{6}$$

Solving the simultaneous equations yields the differential equation for the inductor current:

$$LC\frac{\mathrm{d}^2 I_L}{\mathrm{d}t^2} - \frac{L}{R}\frac{\mathrm{d}I_L}{\mathrm{d}t} + \frac{V_\mathrm{in}}{R} - \int\frac{I_L}{RC} = 0. \tag{7}$$

Bring the design parameters into (7) and use the mathematical calculation software to obtain that the currents flowing through the inductors L_1, L_2, and L_3 are I_{L1}, I_{L2}, and I_{L3}, respectively. From this, the maximum flow into or out of the decoupling capacitor in a single cycle can be calculated. The amount of charge (the area of the shaded part shown in Fig. 3) corresponding to (8), Q_1 and Q_2 are the amount of charge during charging and discharging, respectively:

$$\begin{cases} Q_1 = \int_0^{0.33T} I_{L2} - \int_0^{0.33T} I_{L1} \\ Q_2 = \int_{0.33T}^{T} I_{L1} - \int_{0.33T}^{T} I_{L3} \end{cases}. \tag{8}$$

Therefore, the decoupling capacitor should satisfy (U_mid is the voltage across the decoupling capacitor):

$$C_\mathrm{mid} \geqslant \frac{\max(Q_1, Q_2)}{U_\mathrm{mid}}. \tag{9}$$

However, the value of C_mid can't be too large. When it's value is close to C_{12} and C_{11}, C_mid will participate in LC resonance and offset the resonance point. Therefore, when determining C_mid, we should make C_mid far less than C_{12} under the condition of satisfying (9). According to the simulation analysis, under the condition of guaranteed coupling operation, the upper limit range of C_mid is shown in (10).

$$C_\mathrm{mid} \leqslant 0.2C_{11} \tag{10}$$

In the hardware circuit of this paper, $C_\mathrm{mid} = 0.1C_{11}$ is finally selected.

III. Zero Voltage Switching

In general, the way to achieve ZVS is to add additional passive components to generate voltage resonance, and switch

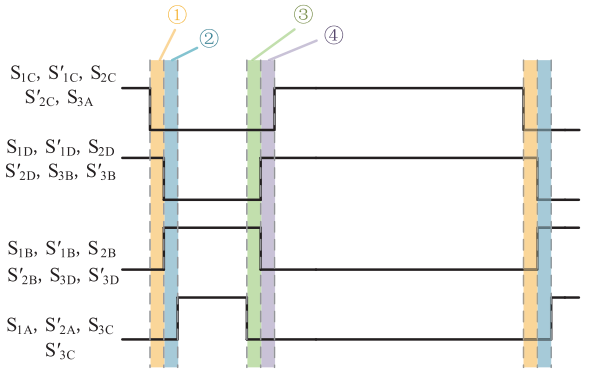


Fig. 5. Control signal under ZVS operating conditions.

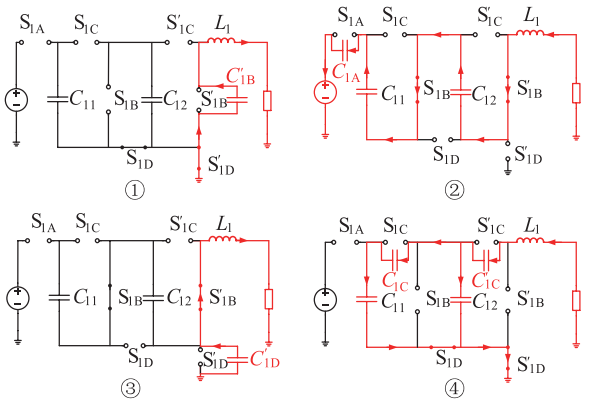


Fig. 6. Working mode during switch switching.

state changes when the voltage reaches zero. In this work, only by changing the dead time and phase relationship of the control signal, the resonant inductor can be used to release the charge stored in the parasitic capacitance between the drain and source of the switch to realize ZVS. Taking the first stage topology as an example, the timing sequence corresponding to the control signal is shown in Fig. 5.

According to the control signal shown in Fig. 5, the circuit mode at the switching moment of the switch can be correspondingly obtained as shown in Fig. 6. Among them, C_{1A}, C_{1C}, C'_{1B}, C'_{1C}, and C'_{1D} represent the parasitic capacitances C_{ds} at both ends of the drain-source stages of the switching S_{1A}, S_{1C}, S'_{1B}, S'_{1C}, and S'_{1D}, respectively.

When entering mode ① , the current of the resonant inductor flows from left to right. Since S'_{1C} is turned off, the inductor current cannot change abruptly, so the current is through C'_{1B}. Before freewheeling, the circuit topology shows that the voltage across C'_{1B} is positive at the top and negative at the bottom. Therefore, during the freewheeling process, the voltage of C'_{1B} gradually drops. When the voltage drops to zero, the inductor current passes through the parasitic body diode contained in S'_{1B} until to zero. In case of ignoring the voltage drop of the diode, in the freewheeling stage of the diode, the voltage across S'_{1B} is always zero, and the ZVS condition is satisfied when it is turned on during this period.

When S'_{1B} is turned on, turn on the S_{1B} and turn off the S_{1D} and S'_{1D}. At this time, the circuit enters the mode ② ,

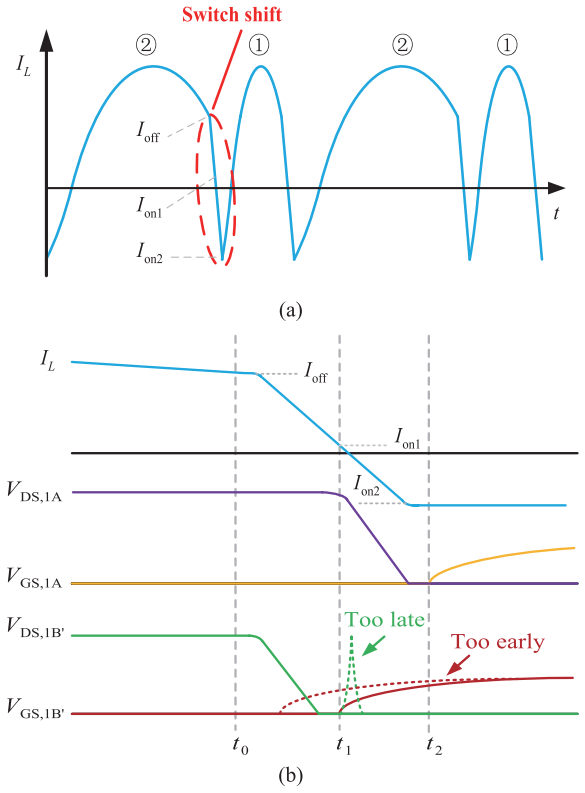


Fig. 7. (a) Inductor current waveform. (b) Detailed view at the ZVS switching moment.

and the inductor current continues to decrease after the zero-crossing point and eventually reverse. As shown in Fig. 6, the inductor current freewheels through C_{1A} after the reverse flow. Before the freewheeling, the polarity of the voltage across C_{1A} is positive on the left and negative on the right. Therefore, the voltage across C_{1A} continues to drop during the reverse freewheeling process of the inductor current. The inductor current freewheels through the body diode after the voltage is reduced to zero. Turn on S_{1A} in the body diode freewheeling stage to complete ZVS with S'_{1B}. Similarly, according to Fig. 6, it can be obtained that S_{1C}, S'_{1C}, and S'_{1D} can realize ZVS in the freewheeling stage. According to the realization principle of ZVS, the inductor current can be obtained as shown in Fig. 7(a). The partially amplified waveform of the current and voltage during the switching process is shown in Fig. 7(b).

In fact, when using this method to implement ZVS, additional attention should be paid to the following two key elements:

(1) The moment of turning on MOSFET

As mentioned before, only the switch is turned on when the body diode freewheels, can the ZVS condition be satisfied. As shown in Fig. 7(b), when S'_{1B} is turned on too early, the parasitic capacitor voltage at both ends of the drain and source of the switch has not yet dropped to zero. The voltage and current waveforms still overlap during the switching process, resulting in switching loss. When the switch turns on too late, the current of the resonant inductor is reversed due to the influence of the reverse voltage. But the switching state of the switch in the circuit has not changed. So, the freewheeling loop remains the same. Therefore, the parasitic capacitance of S'_{1B} is switched from discharging to charging at this time. The parasitic capacitance voltage at both ends of the drain and source rises again to form a voltage spike, which increases with charging time. The voltage and current waveforms overlap again to generate switching loss.

(2) Inductance value

The ZVS technology mentioned in this paper is essentially to release the parasitic capacitance energy between the drain and source of the switch. Then, it could make parasitic capacitance to maintain a state without energy storage during the turn-on process. Therefore, it is necessary to ensure that the inductance is large enough to store enough energy to charge and discharge the parasitic capacitor. Two constraints of inductance are obtained:

$$LI_{off}^2 > C_{sum\_oss}V_{out}^2, \tag{11}$$

$$LI_{on}^2 > C_{sum\_oss}V_{out}^2. \tag{12}$$

Among them, C_{sum_out} is the sum of all parasitic capacitances involved in the process of realizing ZVS, which is generally calculated directly by means of integration.

$$C_{sum\_oss} = \frac{Q_{sum\_oss}}{V_{out}} = \frac{\sum\int C_{oss}(v)\mathrm{d}v}{V_{out}} \tag{13}$$

It can be obtained from (11) and (12) that when the capacitor energy is fixed, larger turn-off and turn-on currents and inductance values are required to meet the energy requirement. For the fixed L case, we can also get the limit range of the turn-off and turn-on currents.

$$\min(I_{on}, I_{off}) > \sqrt{\frac{C_{sum\_oss}V_{out}^2}{L}} \tag{14}$$

Therefore, it can be seen from the above formula that the realization of ZVS has minimum requirements for the absolute value of the turn-on and turn-off currents. But the realization of ZVS also leads to the fact that the inductor current cannot achieve ZCS during switching. In other words, the current is not zero when the switch is turned off but a relatively small value. At the expense of the ZCS, most switching devices are realized ZVS.

This feature does not mean that the sacrifice is worthwhile in any case. When the circuit is under light load operation, the switching loss generated by the switches is mainly due to the energy storage of the parasitic capacitor between the drain and source. Therefore, at this time, sacrificing ZCS to realize the ZVS of device can significantly improve the circuit operation efficiency. When the circuit is under heavy load operation, the parasitic capacitor loss accounts for a small proportion of the total switching loss. At this time, performing incomplete "ZCS" to achieve ZVS of the switches increases the total switching loss and reduce the circuit efficiency. Therefore, when the

TABLE I
SWITCH VOLTAGE/CURRENT STRESS OF THE PROPOSED CONVERTER

Switch	Voltage stress	Current stress(peak)
S_{1A}	$2V_{in}/3$	$I_{out}/2$
S_{1B}, S'_{1B}, S'_{1C}, S'_{1D}	$V_{in}/3$	$I_{out}/2$
S_{1C}, S_{1D}	$V_{in}/3$	$I_{out}/4$
S_{2A}, S_{3A}	$2V_{in}/9$	$I_{out}/2$
S_{2B}, S'_{2B}, S'_{2C}, S'_{2D}, S_{3B}, S'_{3B}	$V_{in}/9$	$I_{out}/2$
S_{2C}, S_{2D}	$V_{in}/9$	$I_{out}/4$
S_{3C}, S_{3D}	$V_{in}/9$	I_{out}
S'_{3C}, S'_{3D}	$V_{in}/9$	$2I_{out}$

circuit is in normal operation, it is suitable to work under ZVS when load is light, and it is more suitable to work under ZCS when load is heavy. In view of this property, in the later optimization work, an additional current sensor can be added to the converter. By detecting the output current, the working state of the circuit can be judged, and the real-time switching of the working mode of the control signal can be realized, so that the converter can always operate in excellent efficiency.

IV. HARDWARE IMPLEMENTATION AND EXPERIMENTAL RESULTS

Based on the above analysis results, the hardware construction and experimental verification of the proposed multi-resonant switched capacitor converter are carried out. In order to facilitate the selection of switching devices, we obtain the switching stress of each MOSFET as shown in Table I.

The selection of the inductor and capacitor values in the circuit needs to meet the resonance conditions. In this work, the switching frequency is designed to 100 kHz. According to (4), the two resonant frequencies can be obtained as 75 kHz and 150 kHz. Then, according to (1) and (2), select the capacitance value as $C_{11} = C_{12} = C_{21} = C_{22} = 100$ μF, $C_{23} = C_{24} = 25$ μF. Therefore, the specific parameter values of each element in the topology can be obtained, as shown in Table II. Moreover, in order to reduce the conduction loss of the converter under heavy load conditions, a 4-layer inner and outer 2 oz copper thick printed circuit board (PCB) is used in this work.

The prototype picture is shown in Fig. 8. In order to make the heat dissipation of the converter more sufficient, the power devices are all on the front. And the driver chip is placed on the back using the gate-level voltage pump power supply scheme [13]−[16]. The radiator is close to the back of the PCB and corresponds to the switch location. In order to make the current distribution in the converter more uniform, a special design is made in the layout. The first stage is placed in the middle. Then, the second stage is placed symmetrically on both sides of the first stage. The eight copper strips shown in the Fig. 8 are the current clamp interface for current testing, which can meet the debugging requirements and reduce the additional conduction loss as much as possible.

In the experiment, the output current of the prototype is tested through the Tektronix TCP0030A current probe. Meanwhile, the efficiency curve when the output current of the prototype increases from 5 A to 23.7 A is finally obtained by reducing the load resistance successively as shown in Fig. 9. Without considering the loss of the drive circuit, the highest efficiency of the circuit is 98.1%, and the full-load efficiency is 93.06%. When the circuit is working normally, the total loss of the driver chip is 1.5 W. Therefore, considering the driving loss, the light-load efficiency is greatly reduced due to the smaller power. While under full-load conditions, the reduction in efficiency is small, and the maximum efficiency becomes 94.64%.

In this regard, we conduct a loss analysis on the experimental prototype. The experimental prototype creates an LC resonance by inductor, enabling all switches to achieve ZCS. Therefore, the switching losses of the topology are negligible, and only the switch, inductor conduction losses, drive losses, and pass losses are considered.

Among them, the calculation formula of the switch conduction loss is as (15).

$$P_{on} = I_{rms}^2 R_{DS(on)} \tag{15}$$

I_{rms} is the effective value of the current flowing through the switch, and $R_{DS(on)}$ is the on-resistance of the switch. The $R_{DS(on)}$ of the MOSFETs in the test prototype are 0.65 mΩ and 1.35 mΩ. Therefore, the conduction loss is 1.2 W at full load.

The conduction loss of the inductor is generally classified into two categories, namely: dc conduction loss and ac conduction loss. The calculation formula is as (16) and (17).

$$P_{DC} = I^2_{rms} R_{DCR} \tag{16}$$

$$P_{DC} = I^2_{rms} R_{ACR} \tag{17}$$

I_{rms} is the relative mean square (RMS) value of the inductor current. R_{ACR} is the RMS value of the ac component of the current. From the data sheet we get $R_{DCR} = 0.32$ mΩ and $R_{ACR} = 8$ mΩ. And the total conduction loss is 2.5 W at full load.

The size of the drive loss is only related to the characteristics of the MOSFET and the switching frequency. The calculation formula is as follows:

$$P_{drive} = Q_g U_g f. \tag{18}$$

Among them, Q_g is the gate charge of the switch tube, U_g is the driving voltage, and f is the operating frequency of the switch. The drive loss is a fixed value 1.5 W.

The experimental prototype, due to heat dissipation and current testing, introduces a large circuit resistance. The pass resistance is equivalent to R_{on}, and the calculation formula of the line loss is as follows:

$$P_{on} = I_{on}^2 R_{on} \tag{19}$$

Through the measurement of impedance analyzer, we get $R_{on} = 2$ mΩ. Therefore, the conduction loss made by circuit

TABLE II
PROTOTYPE PARAMETERS

Components	Manufacture and part number	Parameters
1st stage MOSFET	Infineon, IQE013N04LM6CGATMA1	40 V, 1.1 mΩ
	Infineon, IQE006NE2LM5CGATMA1	25 V, 0.65 mΩ
2nd stage MOSFET	Infineon, IQE006NE2LM5CGATMA1	25 V, 0.65 mΩ
Resonant inductors	Coilcraft SLR4040-220LE	22 nH*, 78 A Isat
	Coilcraft XAL6030-331MEC	330 nH*, 30 A Isat
1st stage flying capacitor C_{11}	SANYEAR C0805X5R106K500NT	10×10 μF±10%, 50 V, X5R, 0805
2nd stage flying capacitor C_{23}	SAMSUNG CL21A475KBQNNNE	5×4.7 μF±10%, 50 V, X5R, 0805
Gate driver	Analog Devices, LTC4440-5	80 V, high-side
Bootstrap diode	Infineon, BAT6402VH6327XTSA1	40 V, Schottky

*The inductance value here refers to the nominal value when it is not saturated. In actual use, the decrease in inductance value due to inductance saturation should also be considered.

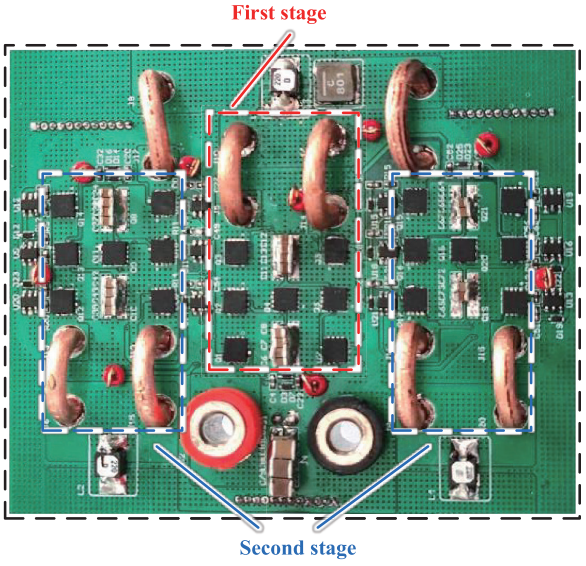


Fig. 8. Experimental prototype (the volume of the power part is 0.36 in^3).

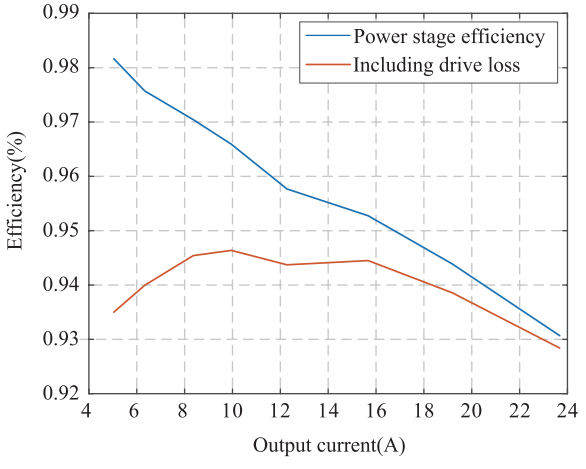


Fig. 9. Curve of resonant converter efficiency with output current.

resistance is 3.8 W at full load.

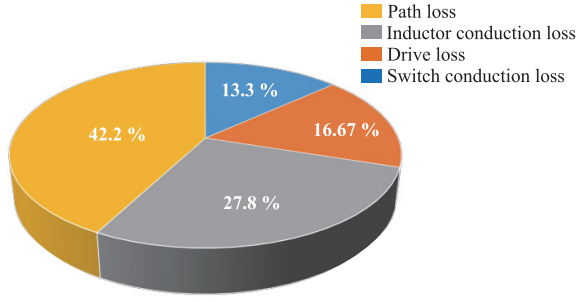


Fig. 10. Loss analysis pie chart.

Under full load conditions, calculate the theoretical value and percentage of the loss of each component according to the above formula as shown in Fig. 10.

As shown in the Fig. 10, under full load conditions, the main loss of the prototype is reflected in the path loss and inductance loss, accounting for 70% of the total loss. The losses of both parts are proportional to the square of the output current. So, the efficiency curve without the drive loss has a relatively large drop and gradually becomes flat near the full load power. For the experimental prototype, the path loss in the hardware experimental circuit has a significant impact on the work efficiency. Therefore, the efficiency can be greatly improved by reducing the conduction losses of the circuit. In the follow-up work, we will focus on the optimization of circuit on-resistance to further improve work efficiency.

During the working process of the converter, most of the energy loss is reflected in the conduction path. The conduction path is equally divided into the entire converter, with sufficient heat dissipation area. Therefore, the experimental prototype built in this experiment does not require a complicated heat dissipation design. Fig. 11 shows the thermal image of the prototype when it is fully loaded. The maximum temperature is 70.5 °C without air cooling, which has sufficient thermal margin for the on-board power devices. By using the control signal scheme shown in Fig. 5, the ZVS of more than 70%

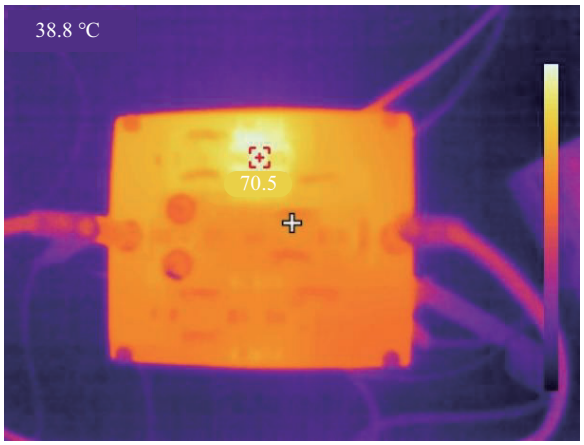


Fig. 11. Thermal imaging diagram of resonant converter at full load.

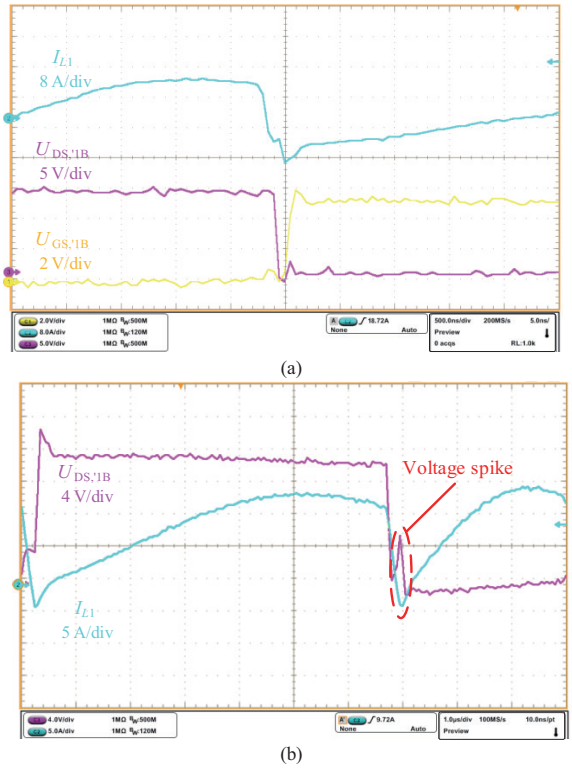


Fig. 12. (a) Drive, drain-source voltage waveforms of S'_{1B} under ZVS. (b) S'_{1B} turns on too late causing voltage spikes.

switches is finally achieved in the prototype. Fig. 12 shows the drive signal, drain-source voltage and inductor current signal of S'_{1B}. After the drain-source voltage drops to zero, the drive signal rises to a high level at this time. Due to the ZVS operating mode, the voltage waveform is clean and there is no significant switching noise. In the process of this experiment, a fixed dead time is used to realize ZVS. For the converter in different working states, the magnitude of the output current will change, and the corresponding drop speed of the inductor current will also change. Therefore, the dead time should also be adjusted accordingly. Finally, in the hardware experiments in the manuscript, the dead time and the phase shift time are

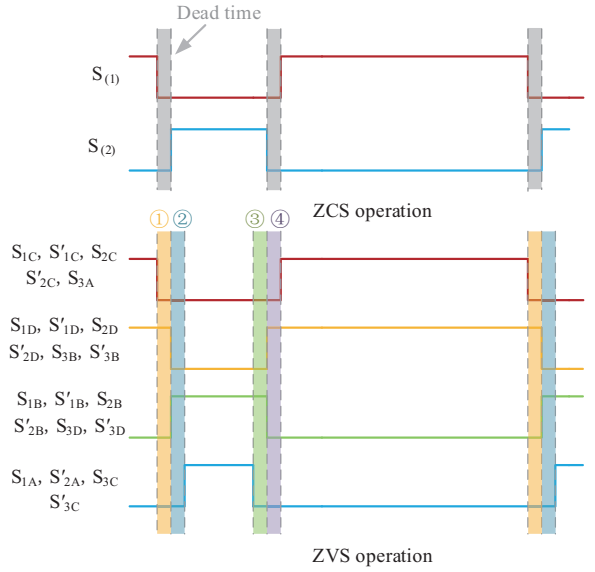


Fig. 13. Control signals for different modes of operation.

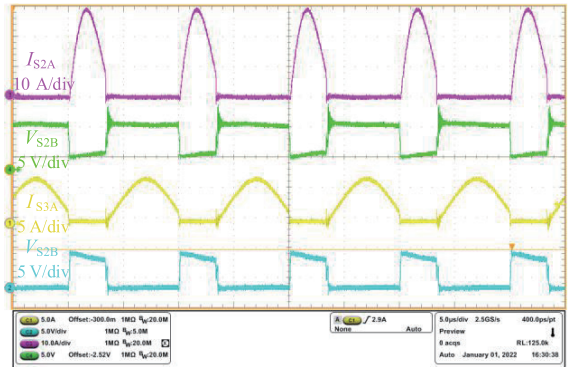
generally set between 15–30 ns.

As shown in Fig. 12, when the dead time is too large, the turn-on time of the switch is delayed, so the voltage spike phenomenon described above will occur. The converter has lost the ZVS condition at this time. With the increase of dead time, the voltage spike gradually increases, and the switching loss also increases.

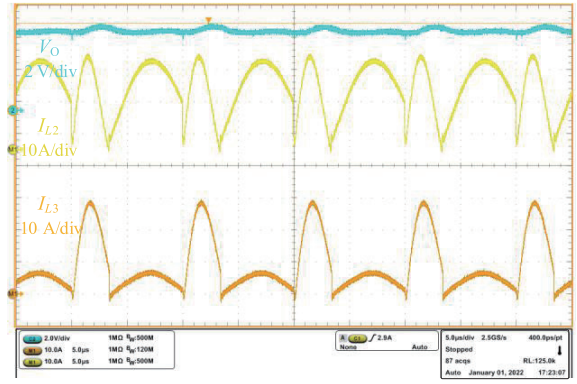
With the further increase of the load, the energy consumed by the parasitic capacitance at both ends of the drain and source of the switch occupies a smaller proportion of the switching loss. Therefore, in order to further improve the efficiency of the converter, the realization of ZVS should be abandoned at this time. It should pay more attention to the realization of ZCS (in the case of realizing ZVS, the inductor current will drop sharply in a short time. So, when state switching occurs, the current flowing through is not zero, which means the ZSC is not realized). As the Fig. 13 shows there are only two modes in the circuit topology, the switches are divided into two groups, which operate synchronously. The control signal also has a short dead time to prevent short-circuit.

Fig. 14 shows the waveforms of key nodes in the cascade connection of the first and second stages and the waveforms of output voltage and current under heavy load conditions. It can be seen from the Fig. 14 that the prototype abandons the ZVS scheme under full-load working conditions. The inductor current does not drop significantly and the whole cycle is greater than zero, achieving complete half-cycle quasi-resonance. The MOSFET switches at the current zero-crossing point. At the cascade connection, it can be seen from the current waveform that the currents flowing through L_2 and L_3 are phase-synchronized. The inductor current fluctuates around zero at the switching point. In other words, the switching between the first-level unit and the second-level unit is smooth, and there is no circulating current phenomenon.

To sum up, the multi-resonant cascaded switched capacitor converter proposed in this work can have a higher step-down



(a)



(b)

Fig. 14. (a) The key point waveform of each node in the cascade. (b) Output voltage and inductor current waveforms.

ratio than the traditional cascaded switched capacitor converter. And it also has the potential of extremely highly power density (The power density under the full load operation is 330 W/in^3). Since the length of the power loop was increased during the experiment to facilitate debugging, additional conduction losses were introduced. Therefore, the efficiency can still be greatly improved by optimizing the PCB layout and manufacturing process.

V. Conclusion

This paper proposes a 48 V−5 V multi-resonant switched capacitor converter suitable for data centers. The converter adopts a two-stage structure. The first stage is a single step-down conversion to reduce the voltage stress, and the second stage is a parallel conversion to reduce the current stress and reduce the size of the intermediate decoupling capacitor by staggered operation. In this paper, the working principle of the two-stage structure is analyzed. Then, the calculation formula of each resonant frequency in the converter and the quantitative relationship between the component parameters are given. In addition, through the analysis of the converter, the paper elaborates the principle of using half-coupling to reduce the decoupling capacitance. Then, using the inductor freewheeling, it is proposed to optimize the control signal, and realize the ZVS of most switches without changing the topology. Finally, according to the theoretical analysis, an experimental platform is built and an experimental prototype with a rated power of 120 W was produced and achieved a peak efficiency of 98.1% and a power density of 330 W/in^3.

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