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# Research Progress on Flexible Oxide-Based Thin Film Transistors

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**Abstract:** Oxide semiconductors have drawn much attention in recent years due to their outstanding electrical performance, such as relatively high carrier mobility, good uniformity, low process temperature, optical transparency, low cost and especially flexibility. Flexible oxide-based thin film transistors (TFTs) are one of the hottest research topics for next-generation displays, radiofrequency identification (RFID) tags, sensors, and integrated circuits in the wearable field. The carrier transport mechanism of oxide semiconductor materials and typical device configurations of TFTs are firstly described in this invited review. Then, we describe the research progress on flexible oxide-based TFTs, including representative TFTs fabricated on different kinds of flexible substrates, the mechanical stress effect on TFTs and optimized methods to reduce this effect. Finally, an outlook for the future development of oxide-based TFTs is given.

**Keywords:** oxide semiconductor; oxide-based thin film transistor (TFT); flexible device; mechanical stress; display

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## 1. Introduction

Since the beginning of the 21st century, the display industry has made great progress, flat panel displays (FPD) started coming into public view as liquid crystal displays (LCD) are pulling out [1–8]. Through several generations of product upgrades, LCDs have been absolutely dominant before active matrix organic light-emitting diodes (AMOLED) appeared [9–19]. OLEDs are considered as one of the most promising next generation display technologies due to their superior performance such as high efficiency, wide viewing angle, low power and small thickness [20–33]. Recently, the oxide-based TFTs driving OLED have become the most promising technology to realize really flexible displays [34–41]. The technological advance in TFTs is a significant factor for promoting the development of such displays [42–50]. Researchers around Nomura et al [42], the earliest engaged in this field, have successfully fabricated the first transparent and flexible oxide-based TFTs, which have rapidly attracted the interest of numerous researchers all over the world [51–61]. Compared with hydrogenated amorphous silicon (a-Si:H) TFTs and low-temperature polysilicon (LTPS) TFTs [62–73], oxide TFTs are reputed as the next-generation displays TFT technology due to their high performance, such as relatively high carrier mobility, good uniformity, low process temperature, optical transparency, low cost and flexibility [74–79]. Besides, integrated circuits containing oxide-based TFTs are gradually getting larger and replacing the silicon-based CMOS circuits. Examples are digital logic circuits, oscillation rings, and operational amplifiers [80–95].

In 2004, ZnO-channel TFT test structures were fabricated by Hoffman et al. using a bottom-gate structure on thermally oxidized Si, while ZnO has been deposited via radiofrequency (RF) sputtering from an oxide target with an unheated substrate [96]. In these devices, the ZnO-channel TFT mobility was as high as 25 $cm^2 V^{-1} s^{-1}$, which proved that oxide TFTs may become desirable alternatives for high-resolution display applications. Then, Fortunato et al. reported a bottom gate configuration ZnO-TFT with a mobility value of 20 $cm^2 V^{-1} s^{-1}$ and an optical transmittance above 80%, including a glass substrate, via RF magnetron sputtering at room temperature in 2005 [97]. It has been shown that ZnO-TFT can potentially be fabricated on thermal-sensitive substrates, such as plastics and metal foils. With the development of TFTs, the feature size of devices is becoming smaller. Hence the short channel effect on TFTs should be considered. Hsieh et al., in 2006, fabricated a series of miniaturized ZnO TFTs with various channel widths and lengths [98]. Well-behaved TFTs with channels of 5 μm were achieved with a saturated mobility of >8 $cm^2 V^{-1} s^{-1}$ and on/off ratios of up to $10^7$. At the same time, channel layers with amorphous indium gallium zinc oxide (a-IGZO) were employed in TFTs by Yabuta and his colleagues, with RF magnetron sputtering at room temperature [99]. These devices operated in n-type enhancement mode with a field-effect mobility of 12 $cm^2 V^{-1} s^{-1}$, an on-off ratio of ~$10^8$, and a subthreshold gate voltage swing of 0.2 V $decade^{-1}$ and opened the possibility for high-resolution and integrated circuit applications. A higher mobility of 100 $cm^2 V^{-1} s^{-1}$ was reported by Fortunato et al. [100]. However, it is still necessary to understand the origin of the hysteresis to achieve proper device stability under encapsulating conditions. An etch stop (ES) structure was employed in TFTs, where a 100-nm-thick $SiO_x$ layer was deposited by plasma enhanced chemical vapor deposition to prevent plasma damage to the active layer [101]. Such ES structure showed good stability under the condition of bias and illumination stress. After that, to improve the performance of oxide-based TFT, many workers reported to the use of different electrode materials. In 2018, Wang et al. focused on the high-frequency properties of a-IGZO TFT, and fabricated devices on high resistivity silicon substrates with a $Ta_2O_5$ gate dielectric. Such devices, high performance and fully oxide-based complementary logic gates for a range of electronics applications could become reality [59]. Additionally, dual gate structures of a-IGZO TFTs were presented [102–107]. With such structures, top gates were served as the device properties controlling terminals, the properties of TFTs could be improved by changing the top gate voltage. However, some challenges could still be considered while using top gate devices.

In the past ten years, with the progress of flexible electronic devices, the performance of oxide-based TFTs has been enhanced step-by-step and nowadays can satisfy the demand for real commercialization for flexible displays, wearable devices and curved televisions. Besides, with the improved understanding of TFT technology, related techniques, particularly for flexible TFTs, have been developed. Therefore, how to further enhance the performance of TFTs is also significant to other related fields. Several methods of low-temperature processes have been studied such as solution processing of oxide TFTs, which has attracted both industrial and academic interest [108–119]. Compared to the sputtering processing, employing solution processing in fabrication of TFTs could not only avoid using the expensive equipments, but also be compatible with ink-jet printing and roll-to-roll processes, which can significantly reduce the cost [120–131]. Hence, research work engaging in the oxide-based TFTs' technology is focusing on all aspects of TFTs to obtain better-performance devices, including materials, structures, processes, stabilities and mechanical properties.

In this review, the basic fundamental concept of the carrier transport mechanism of oxide semiconductor materials is introduced in Section 2.1. Secondly, five kinds of conventional configurations of oxide-based TFTs are briefly presented in Section 2.2, including ES, a back channel etch (BCE), top gate (TG), dual gate (DG), and co-planar (CP) structures. Next, the primary strategies to develop flexible oxide-based TFT on different kinds of flexible substrates with different process temperatures are presented in Section 3.1. After that, the mechanical stress effects of common bending behaviors on flexible TFTs were investigated and the effective methods to decrease these mechanical stress effects are given in Section 3.2. In the end, an outlook for the future development of flexible oxide-based TFT is presented.

## 2. Device Fundamental Concept and Conventional Configuration

### 2.1. Carrier Transport Mechanism of Oxide Semiconductor Materials

Compared to monatomic silicon, oxide semiconductors are more complex materials as these are built up from several chemical compounds and can contain more different kinds of defects and impurities. Hence, it is beneficial for fabrication to comprehend the carrier transport mechanism of oxide semiconductor materials. In ternary and multinary compound semiconductors (e.g., indium zinc oxide (IZO), indium gallium zinc oxide (IGZO)), zinc (Zn) is replaced by indium (In), which generates excess electrons, resulting in most oxide semiconductors exhibiting n-type characteristics. However, in binary semiconductors (e.g., ZnO, $In_2O_3$), the mechanism of conduction is unintelligible. Lany [132], Ambrosini [133], and Agoston [134] considered the mechanism to be oxygen vacancy doping; one of the most popular explanations. Calculation results show that at a high Fermi level oxygen vacancy has a low formation energy, which proves that the oxygen vacancy concentration indeed determines the conductivity and the charge carrier concentration. However, other theoretical calculations [72] show that oxygen vacancies form deep donors make it difficult to excite electrons to the conduction band. Another possibility for the explanation of n-type conductivity was reported by Van and Limpijumnong et al. [135,136]. These authors proposed that unintentional hydrogen incorporation could be the reason for the observed n-type characteristic of oxide semiconductors. Such an assumption, however, fails to explain the high conductivity of the high purity of $In_2O_3$. Besides, some other propositions still fail in persuasiveness [137–139].

In the case of the doped oxide semiconductors (e.g., a-IGZO), In has the electron structure of (n −1) d10ns0 (n > 5), where the electronic channel would be generated by overlapping the adjacent 5s electron orbit. The 5s electrons are spherically symmetric and insensitive to direction. Hence, the degree of ion alignment has little influence on electron transportation. As the conduction band minimum (CBM) is contributed by the In 5s orbital, rather than from Zn 4s or Ga 4s. The mobility and effective masses of monocrystalline and amorphous IGZO are relatively close due to the similar bandwidth of the conduct band level [140] and the close effective mass of 0.18 me and 0.2 me [141]. However, the mobility of IGZO depends on the electron concentration, which can be explained by the osmotic conduction model [142–144]. In this model, the center energy ($\phi_0$) of a-IGZO is getting closer to the Fermi level ($E_F$), with rising electron concentrations, thus, leading to a narrower distribution width ($\sigma_\phi$).

### 2.2. Typical Device Configurations

By depositing a gate, an oxide semiconductor and drain/source electrodes in different ways and in different orders, five different types of device configurations can be formed, namely ES, BCE, TG, DG, and CP structure, as shown in Figure 1.

In Figure 1a, the BCE configuration is shown, which is applied in most commercial applications (e.g., cellphone, TV) due to its simple photolithography process and low cost. As oxide semiconductors are very weak in most of the wet etchants, dry etching needs to be employed to etch the S/D electrodes. A downside of dry-etching, however, is that the TFT devices can become ion-damaged by plasma bombardment during the dry etching process [145]. To avoid these effects, the ES configuration shown in the Figure 1b and contains an added ES layer formed and patterned on the active layer to protect the channel during the etching of the S/D electrodes [146]. However, it makes the processes more complicated and increases the cost. Figure 1c shows the TG structure, where the passivation is replaced by the top gate insulator and electrode to protect the active layer [147]. Nonetheless, the stability of negative bias illumination stress of the top gate structure TFTs still needs to be improved. By combining the TFTs (Figure 1a–c), the DG structure with a top gate, a bottom gate is obtained, which presents a high performance for driving pixel circuits, gate driver circuits, and other integrated circuits, as shown in Figure 1d. However, it is observed that the overlap between the gate and source/drain electrodes in Figure 1a–d causes a high parasitic capacitance. This capacitance is proportional to the overlap area

and induces a resistance-capacitance (RC) delay in the TFT arrays and integrated circuits. To reduce this RC delay effect, coplanar structures of TFTs called CP TFTs are presented in Reference [148], as shown in Figure 1e. In CP TFTs, the overlap between the G and S/D electrodes is negligible so that the parasitic capacitance can be remarkably reduced.

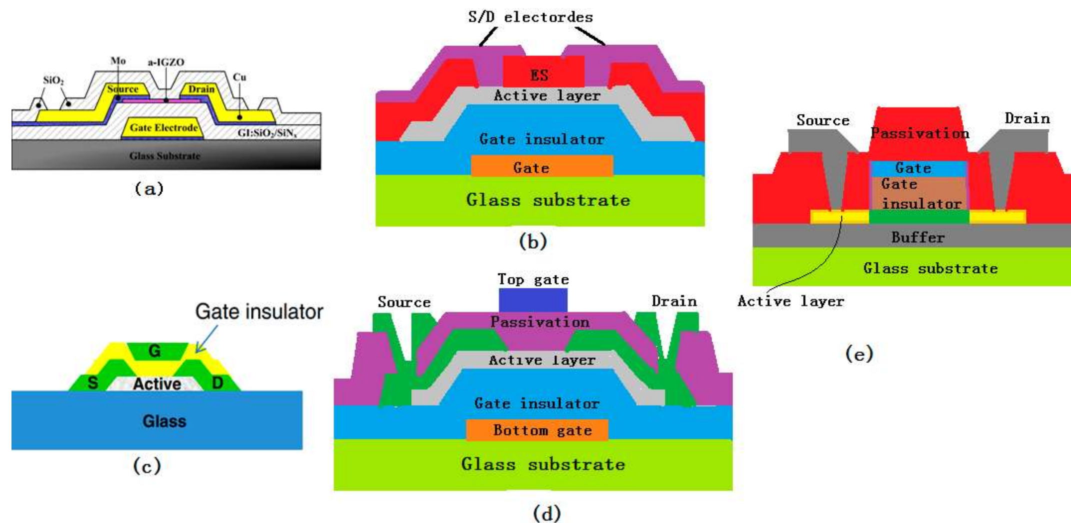


**Figure 1.** Typical device configurations of oxide semiconductors: (**a**) back channel etch (BCE) structure, (**b**) etch stop (ES) structure, (**c**) top gate (TG) structure, (**d**) dual gate (DG) structure, (**e**) co-planar (CP) structure.

## 3. Approaches to Flexible Oxide-Based TFTs

In the case of conventional substrates (e.g., glass, silicon), the process temperature and the effects of a high water vapor transmission rate and bending strain need not be considered. In contrast, all these effects will have to be considered on flexible substrates, especially the thermal expansion of the substrates during each process step. Temperature change will result in a mismatch between films and substrates, which can degrade the materials and the devices. This mismatch is contributed to by the large differences in the coefficients of thermal expansion (CTE), elastic modulus and toughness between polymer substrates and functional films. Three types of polymer substrates are shown in Figure 2 [149], which are categorized by their maximum process temperature: conventional polymers ($T_g < 100$ °C), common high-temperature polymers ($100 \leq T_g < 200$ °C) and high-temperature polymers ($T_g \geq 200$ °C). Polyimide (PI), polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polydimethylsiloxane (PDMS) and polycarbonate (PC) are the most commonly used flexible substrates. Hence, flexible oxide-based TFT fabrication on such substrates is discussed respectively in this section.

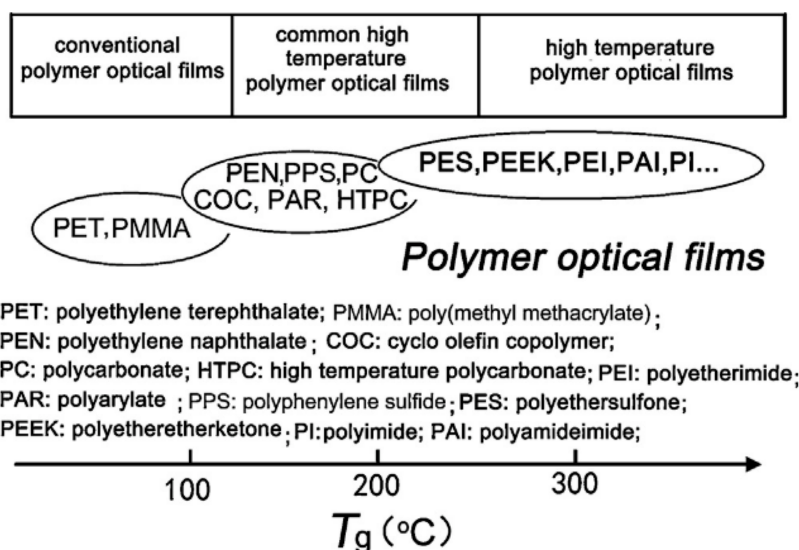


**Figure 2.** Classification of polymer optical films [149].

### *3.1. Flexible TFTs on Different Kinds of Substrates*

#### 3.1.1. PET Flexible Substrate

PET is currently widely used as a protection layer in the application, due to its good optical transparency and short cut-off wavelength. However, PET will lose its optical and mechanical properties at high processing temperatures, which may bring challenges to device fabrication, integration and operation. During the past ten years, research about oxide-based TFTs fabricated on PET substrates has been reported, which aims to suppress defect formation in PET through evolutionary process steps and optimized device structures.

In 2010, Liu et al. first achieved all-amorphous-oxide transparent, flexible TFTs with bilayer gate dielectrics on PET substrates at room temperature [71]. This TFT had combined gate dielectrics ($Ta_2O_5$/SiOx bilayer structure), the active layer consisted of amorphous zinc-indium-tin oxide (a-ZITO) and S/D electrodes of an oxide conductor (a-ZITO), and exhibited a saturated mobility of 20 $cm^2\ V^{-1}\ s^{-1}$ and on/off ratios $>10^5$. As shown in Figure 3a, the bilayer gate dielectric with a 70 nm a-$Ta_2O_5$ film and 5 nm $S_iO_x$ layers exhibited excellent insulating properties. With thin $S_iO_x$ layers, the dielectric-semiconductor interfacial compatibility could be enhanced and the hysteresis could be suppressed. However, there was no report on its stability. Another approach to reduce the process temperature is by using solution-based processes. Lee et al. utilized an organic-inorganic heterostructure to prepare high-performance ZnO-TFTs on a PET substrate using a low-temperature process (<150 °C), as shown in Figure 3b [69]. In this device, PMMA was adopted as a dielectric layer, and a ZnO film formed the active layer. However, the compatibility of the interface between PMMA and ZnO (organic-inorganic) needed to be enhanced through optimized processing or by using other materials.

High mobility oxide-based TFTs on flexible substrates are urgently needed, along with the development of high-resolution flexible displays and circuits integrated TFTs. Han et al. fabricated a flexible BCE structure TFT at room temperature by employing aluminum-doped ZnO (AZO) as an active channel layer [150]. In this way, a higher mobility of 21.3 $cm^2\ V^{-1}\ s^{-1}$, a drain current on/off ratio of $2.7 \times 10^7$, a low off current value on the order of $10^{-12}$ A, a subthreshold swing of 0.23 V $dec^{-1}$ and a threshold voltage of 1.3 V could be obtained, but no study on the stability of the device was provided.

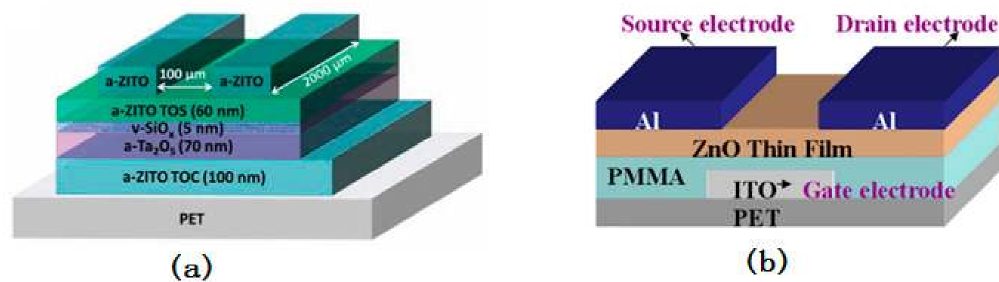


**Figure 3.** (**a**) All-amorphous-oxide transparent TFT [71]. (**b**) ZnO-TFT with an organic-inorganic heterostructure [69].

It is known that the substrates of TFTs should have a large mechanical deformation range, while employed in flexible displays, wearable electronics and in sensors. Thus, the bending stability in flexible applications is one of the most critical issues in the evaluation of device performance. Lee and his co-workers fabricated a bottom gate structure for flexible transparent IGZO TFTs, as shown in Figure 4 [151]. Figure 4a shows an un-passivated device, while Figure 4b presents a passivated one. The experimental results show that the 15-nm-thick $SiO_x$-passivated IGZO flexible TFTs reveal a much better performance including a saturation drain-source current of 10.6 µA, a mobility of 8.0 $cm^2\ V^{-1}\ s^{-1}$, a threshold voltage of 2.85 V, a transconductance of $4.64 \times 10^6$ S, and a subthreshold swing of 0.23 V $dec^{-1}$. Tests on the bending stability of the un-passivated and passivated IGZO flexible TFTs show that the variation of mobility and the threshold voltage is within 10% and 8% when bending for 1500 times with a bending radius of 1.17 cm. These variations in the mobility and threshold voltage between the TFTs mainly come from two factors: The first one is that the channel of the un-passivated TFT was exposed to the ambient, which resulted in the degradation of the device. The second is the strain effect. When bending the TFTs, stress coming from the mechanical deformation directly concentrates on the active layer in device (a), whereas in the device (b) it concentrates in the passivation layer.

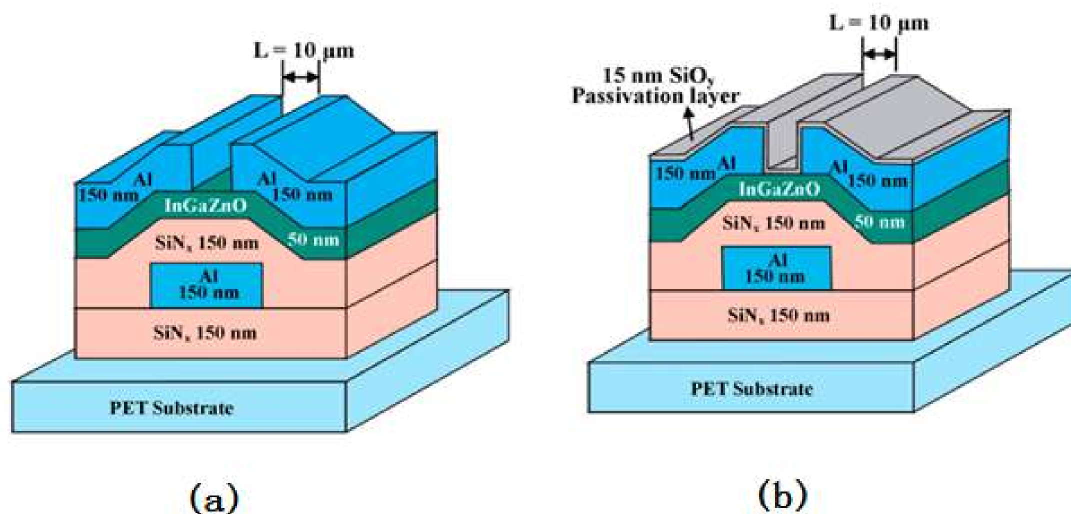


**Figure 4.** Schematics of bottom-gate-type indium gallium zinc oxide (IGZO) TFT [151], (**a**) un-passivated structure, (**b**) passivated structure.

As mentioned above, higher quality gate dielectric layers can hardly be deposited on PET substrates due to its low process temperature limit (<100 °C), which remains the biggest barrier for PET to become promoted. For the further development of TFT technology and for higher device performance, new substrate materials with a higher process temperature limit should be launched.

3.1.2. PEN Flexible Substrates

On PEN substrates, the films appear in a slightly white color. Compared with PET, the maximum process temperature of PEN is higher (Tg ≈ 180 °C). In the past, PEN has been utilized in the production of electronic items such as audio-visual accessories and videotape. Besides, PEN provides better barriers for oxygen and carbon dioxide, which makes it interesting for applications in flexible displays.

Gadre et al. used RF sputtering to achieve a-IGZO thin films on PEN at room temperature, which featured high transmittance and good performance after 6 h of oxygen-annealing followed by 6 h of vacuum-annealing [152]. Furthermore, a 130 nm thick $Al_2O_3$ was deposited as a gate insulator by Kim et al. employing an atomic layer deposition (ALD) method at a growth temperature (Ts) of 150 °C [81]. Bending tests were performed to investigate the change in device properties. Oxide TFTs based on the dual active layer architecture were developed by Marrs et al. [153], as shown in Figure 5a. Devices with this dual-active-layer exhibited an improved performance and stability under gate bias stress when compared to their single-layer counterparts.

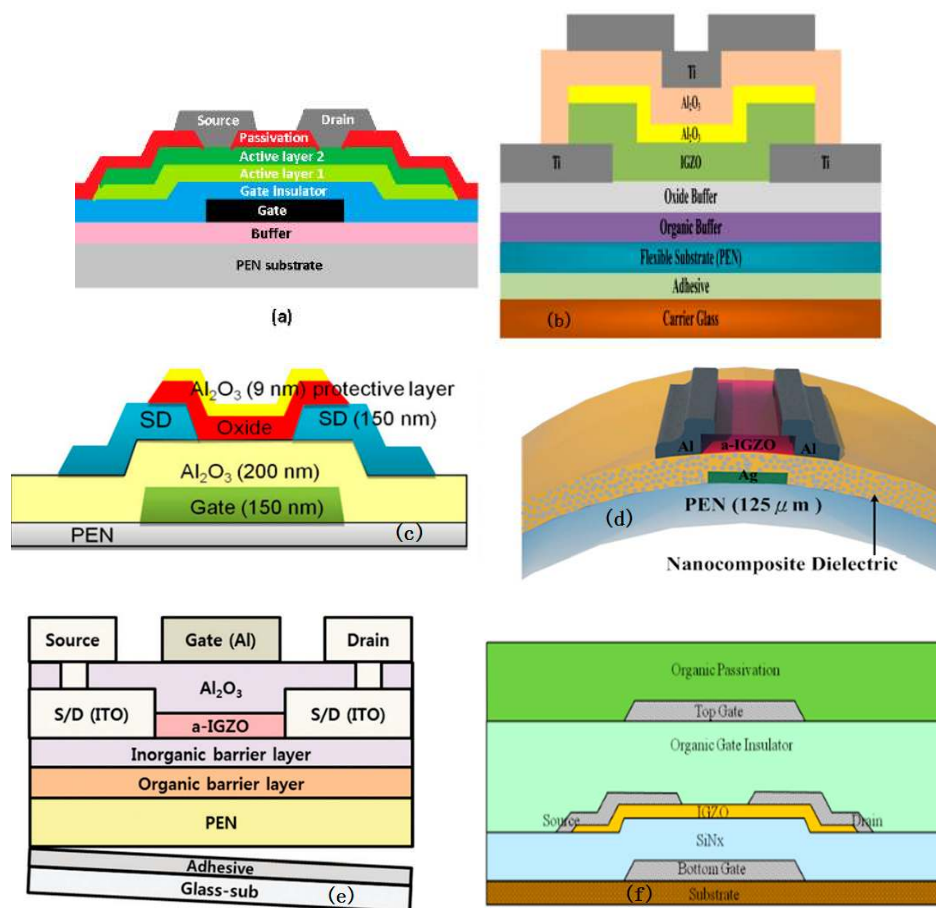


**Figure 5.** Schematic of the TFTs fabricated on PEN. (**a**) Dual active layer structure. (**b**) Top-gate structure [86]. (**c**) IZO:F-TFTs with fluorine-doped [124].(**d**) a-IGZO TFTs with nanocomposite dielectric [49]. (**e**) A-IGZO-TFT with double-layered barrier layer structure [154]. (**f**) A-IGZO-TFT formed using a flash lamp annealing process [155].

A top-gate structure IGZO TFT fabricated on PEN is shown in Figure 5b [86]. A cool-off type adhesive was used to laminate PEN from glass, which is convenient for the debonding process. There were two buffer layers deposited on the PEN before sputtering the S/D electrodes to achieve a smooth surface, low moisture permeability, and strong protection from mechanical damage. This device with a 2:1:2 (In:Ga:Zn) IGZO channel composition exhibited a high performance such as a mobility of 7.83 $cm^2 V^{-1} s^{-1}$, a threshold voltage of 1.93 V, and a subthreshold swing of 0.24 V $dec^{-1}$. As discussed

in Section 2.1, the solution-process technology is widely used in the production of flexible devices, due to the low process temperature and the inexpensive fabrication of large-areas without using vacuum deposition techniques. In 2013, Seo et al. fabricated flexible fluorine-doped indium zinc oxide (IZO:F) TFTs by spin-coating an aqueous solution containing metal fluoride precursors, as shown in Figure 5c [124]. After 2 h of annealing at 200 °C, these TFTs showed a mobility of 4.1 cm$^2$ V$^{-1}$ s$^{-1}$. Lai and co-workers adopted the $Al_2O_3$ nanoparticles to incorporate into a polymer as a nanocomposite dielectric on a-IGZO TFTs by means of a solution process. Compared to inorganic dielectrics, TFTs with nanocomposite dielectrics had a higher flexibility and exhibited a relatively high mobility of 5.13 cm$^2$ V$^{-1}$ s$^{-1}$, as shown in Figure 5d [49]. An IGZO-TFT with inorganic/organic barrier layers as a buffer layer is illustrated in Figure 5e. A 3 mm-thick spin-coated organic layer and a 50 nm-thick ALD $Al_2O_3$ inorganic layer were fabricated before depositing onto the active layer. TFTs with the proposed structure exhibited a saturated mobility of 15.5 cm$^2$ V$^{-1}$ s$^{-1}$, an on/off ratio of $2.2 \times 10^8$, and a subthreshold swing of 0.2 V dec$^{-1}$ [154]. The dual gate structure of the a-IGZO, shown in Figure 5f, formed a TFT using a flash lamp annealing process under mechanical stress, as presented by Liang et al. [155]. This device showed a threshold voltage of 0.26 V, a subthreshold swing of 0.37 Vdec$^{-1}$, an on/off ratio of $10^8$, and the drain current was ~$6 \times 10^{-5}$ A.

In 2014, Xu et al. demonstrated flexible oxide TFTs using anodized aluminum oxide as a dielectric layer, as shown in Figure 6a. With this high-performance dielectric layer, the TFTs exhibited a mobility of 12.87 cm$^2$ V$^{-1}$ s$^{-1}$, a subthreshold swing of 0.2 V dec$^{-1}$, and an on/off ratio of $10^9$. Moreover, a 5 inch flexible AMOLED demo display was fabricated by integrating the bottom emission OLEDs and the thin film encapsulation on the flexible TFT backplane, shown in Figure 6b [156].

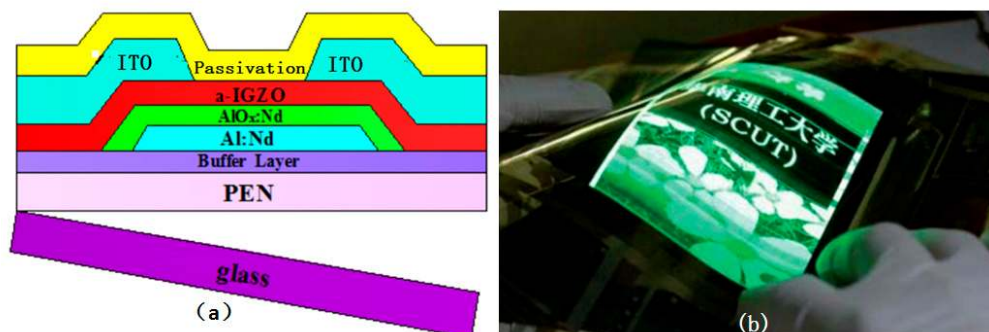


**Figure 6.** (**a**) Schematic of TFT with the dielectric of anodized aluminum oxide. (**b**) AMOLED on a PEN substrate [156].

As mentioned above, PEN substrates with higher maximum process temperatures than PET have been employed for flexible TFT circuits and displays by many researchers. When used under flexible occasion, substrates should have good mechanical strength as the mechanical strain is likely to be generated continuously. Reports on repeated bending tests can hardly be found on PEN substrates due to its poor mechanical strength of such substrates and its negative effect on the lifetime of the electronic devices.

### 3.1.3. Polyimide (PI) Flexible Substrate

According to Figure 2, PI substrates are high-temperature polymers, exhibiting a superior performance with a CTE of $12 \times 10^{-6}$ K, a small humidity expansion coefficient (HEC) ($9 \times 10^{-6}$% RH), a high $T_g$ of 360 °C, and a surface roughness in the nanometer range. Although the standard PI exhibits a yellowish to brownish color, PI is the most frequently used kind of substrates. Recently, colorless and transparent polyimide (CPI) films and their analogues occupy the leading edge positions in advanced polymer optical films in terms of their comprehensive properties and potential market volume, including polyamideimide (PAI) and polyetherimide (PEI) [149].

As shown in Figure 7a, a high-κ HfLaO gate dielectric was fabricated in an a-IGZO TFT on a PI substrate [76]. Due to the high-k gate dielectric, this device exhibits a low threshold voltage of 0.1 V, a small subthreshold swing of 0.18 $Vdec^{-1}$, a high mobility of 22.1 $cm^2\ V^{-1}\ s^{-1}$ and an acceptable on/off ratio of $2 \times 10^5$, making it possible for portable applications. Jung et al. reported a type of oxide semiconductor TFT formed by a solution process [157]. In this device, the active layer film was enhanced by co-doping Li and Zr. Depending on the annealing temperature, these devices exhibited variable performance.

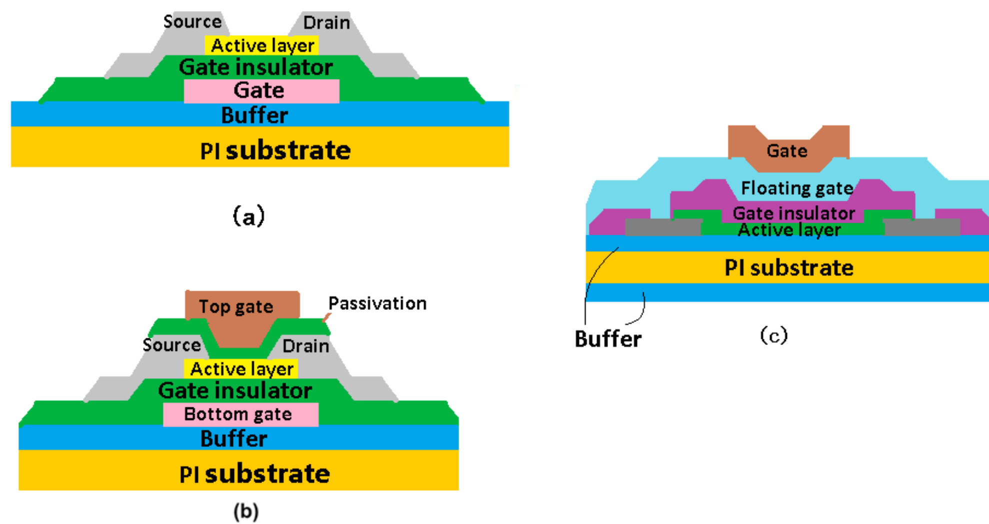


**Figure 7.** Schematic of TFTs on PI: (**a**) with a high-κ HfLaO as a gate dielectric, (**b**) dual gate structure with the conventional process at room temperature, (**c**) with a ferroelectric poly as a buried gate.

Dual gate a-IGZO TFTs on PI substrates were presented by Münzenrieder [158,159]. The structure of TFTs on PI substrate is shown in Figure 7b, 35 nm Ti was evaporated as a bottom gate, while 50 nm Cr was used as a top gate. With the dual gate structure, the gate capacitance was increased by 78% and the threshold voltage was higher (700 mV), while the transconductance was nearly double. Hence, the performance of the device was improved as well, such as the subthreshold swing of 69 mV $dec^{-1}$ and the on/off ratio of $2 \times 10^9$. While the self-alignment could also be used in fabricating the device. The S/D to gate overlaps as small as 1 μm led to parasitic overlap capacitances of 5.5 $Ff\mu m^{-1}$. As a consequence, the frequency of the TFT reached 5.6 MHz. Petti and his co-workers presented a type of a-IGZO memory TFTs as shown in Figure 7c. In this device, 100 nm-thick P(VDF-TrFE) was used as a floating gate and formed using spin-coating a solution of 1 wt% VDF (70 mol%) and TrFE (30 mol%) in methyl-ethyl-ketone. The deposited film was crystallized at 140 °C for 15 min in ambient air. The thickness and the recipe of the P(VDF-TrFE) layer were optimized to obtain Fe-TFTs capable of low-voltage operation (<10V). The results shown that the mobility was 8 $cm^2\ V^{-1}\ s^{-1}$, the on/off ratio was $1.7 \times 10^7$, the subthreshold swing was 152 $mVdec^{-1}$ and the gate leakage current $I_G$ was confirmed to be smaller than $10^{-10}$ A [50]. Nevertheless, the stability on mechanical stress should be further improved.

Figure 8 illustrates a type of IGZO-TFT with high reliability under bending tests. This device employed a thermally stable SA7 organic material as the multi-functional barrier and dielectric layers [160]. The fabricated TFTs exhibited a good performance with a mobility of 15.67 $cm^2\ V^{-1}\ s^{-1}$, a threshold voltage of 6.4 V and an on/off ratio of $4.5 \times 10^5$. Furthermore, bending tests were carried out. After 1000 bending cycles under a bending strain of 3.33% and a bending radius of 1.5 mm, no significant device degradation could be observed.

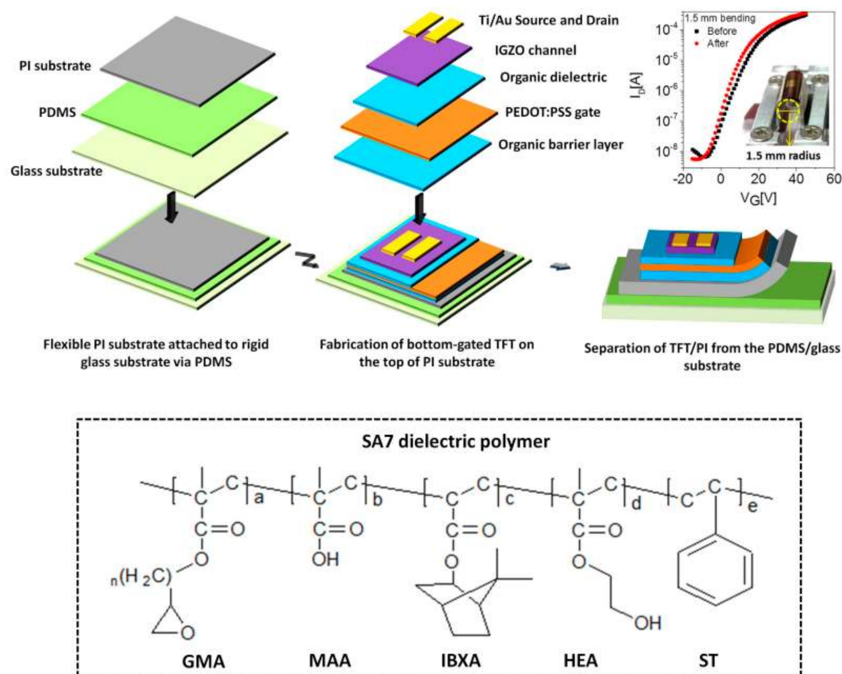


**Figure 8.** The fabrication process for IGZO TFTs (top left). Transfer curve of IGZO TFT under bending stress (top right corner). Chemical structure of SA7 [160] (dotted box).

Recently, Zhang and Wu et al. have presented two types of IZO TFTs structures and their applications on PI substrates [161,162]. Figure 9a, b shows the structures of the device, one is a BCE structure and the second an ES one. In the BCE structure, a 100-nm silicon nitride ($SiN_x$) film is deposited by plasma-enhanced chemical vapor deposition (PECVD) on the glass as a surface isolation layer (SIL) prior to the coating of the PI film to prevent the formation of a chemical bond between the PI and the glass. The PI layer with the thickness of 20 µm is formed by spin coating the poly (amide acid) (PAA) solution on the SIL. Then, it is soft-baked as follows: 80 °C for 30 min, 200 °C for 1 h, and 350 °C for 1 h. The thermal imidization should proceed in the oven with a nitrogen atmosphere for transforming the PAA into PI. The corresponding root-mean-square roughness of the PI film was 2 nm, which may be small enough to avoid affecting the roughness of the IZO film. Then, a stacked structure of $SiN_x$ (250 nm)/photoresist (2000 nm)/$SiN_x$ (250 nm) was deposited on the PI surface at 150 °C as gas and water barrier by PECVD and spin coating alternatively. It should be noted that the devices were post-annealed at 300 °C for 1 h in an air atmosphere, which is the maximum temperature for the TFT process. At last, the PI substrate in company with the TFT devices was separated from the carrier glass when the device formation was completed. The measurement curves of the transfer characteristic with different bending radius are shown in Figure 9c. In ES structure, a surface isolation layer (SIL) is deposited on the carrier prior to the coating of PI film to prevent the formation of a chemical bond between PI and the carrier glass. The poly (amide acid) solution with about a 15-µm thickness was coated on the SIL. In addition, it was transformed into the PI by the thermal imidization process in an oven with a nitrogen atmosphere. A stacked $SiN_x/SiO_2$ was deposited on the PI as a buffer layer with a total thickness of 300 nm by plasma-enhanced chemical vapor deposition (PECVD). A 200-nm molybdenum (Mo) gate metal film was deposited onto the buffer layer. Then, a 200-nm-thick $SiO_2$ gate insulator film was deposited by PECVD at 310 °C. A 30-nm indium zinc oxide active layer with the In:Zn ratio of 1:1 was deposited on the insulator $SiO_2$ by radio frequency magnetron sputtering, which was pre-annealed in an $O_2$ atmosphere for 30 min at 350 °C. Then, an ES layer used for protecting the active layer was fabricated and patterned by dry etching. For the source/drain electrodes, a stacked structure of molybdenum/aluminum/molybdenum (Mo/Al/Mo) was sequentially formed by sputtering and patterned by wet etching. The device was post-annealed

at 350 °C for 30 min in an $O_2$ atmosphere. Finally, the PI with TFTs was de-bonded mechanically from the glass. Figure 9d shows the measured transfer characteristic (W/L = 10 µm/10 µm with Vds = 5.1 V) at the initial state and the bent state with a different curvature radius (R) from 50 mm to 10 mm. Both devices exhibited a high performance and reliability on bending tests and have been employed into the applications shown in Figure 9e,f. We used the BCE TFTs to construct a new gate driver circuit with low power and high stability. ES TFTs were adopted to fabricate flexible AMOLEDs. The experimental results show that the display still works after 10,000 times of testing.

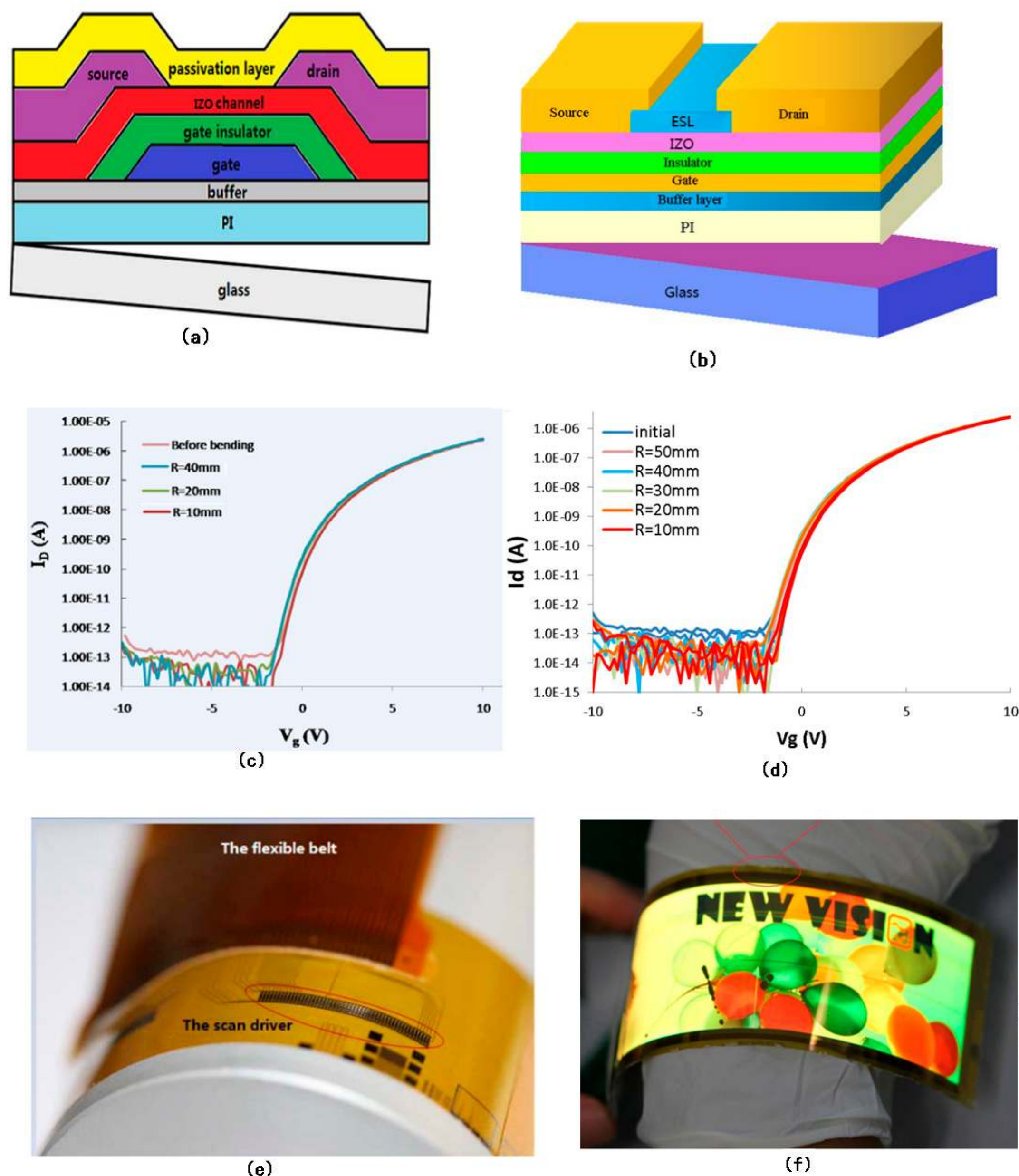


**Figure 9.** (**a**) and (**b**), schematic of BCE TFT and ESL TFT, (**c**) and (**d**), transfer characteristic of BCE TFT and ESL TFT, (**e**) and (**f**) application of BCE TFT and ESL TFT [161,162].

As the technology is developing, the application of oxide-based TFTs is not restricted to displays. For example, TFTs have been employed in integrated circuits, like ring oscillators, amplifiers, logic gates, radiofrequency identification (RFID) systems and so on [39,53,55,90,94,95,163–169]. It is necessary for TFTs to enhance their maximum power gain frequency and to reduce the parasitic capacitance between electrodes. Munzenrieder et al. used a self-alignment process to realize a BCE

structure with a channel with a length of 0.5 μm [163]. There, the maximum oscillation frequency (maximum power gain frequency) $f_{max}$ was extracted to be >300 MHz, giving hope that the device can be applied to high-frequency applications. Bending tests, also conducted in the study, showed that $f_{max}$ was reduced by 3.6% when a TFT was bent to a tensile radius of 3.5 mm.

A flexible-skin-like sensor, biosensor and other kinds of sensors based on oxide-based TFTs are receiving wide interest [170–172]. Knobelspies and his co-workers presented a room temperature gas sensitive TFT, as shown in Figure 10 [172]. Figure 10a shows the schematic fabrication flow of the a-IGZO TFT whose channel produces a chemical reaction when it is exposed to the oxygen, $NO_2$ or $H_2O$. The experimental results show that there was almost no hysteresis in the response to $NO_2$ in the investigated range of 2–5 ppm with 20% background oxygen at room temperature. When combined with analog or logical circuits, this sensor could be realized for actual applications.

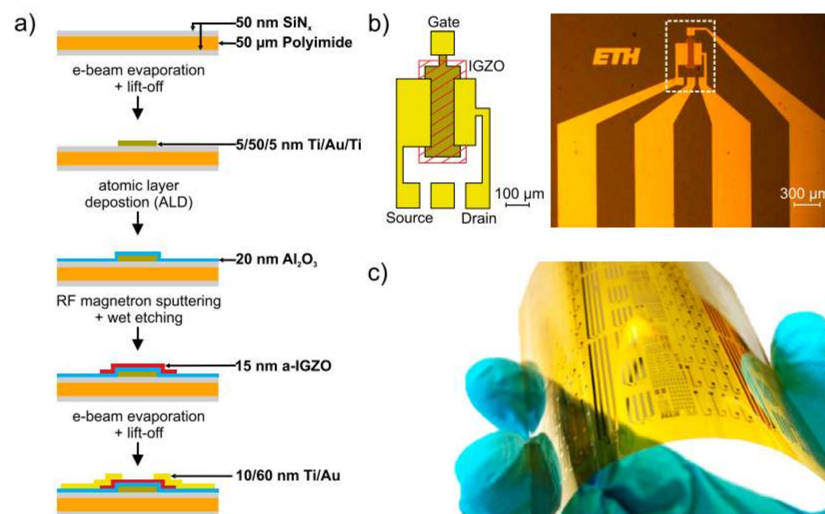


**Figure 10.** (**a**) schematic fabrication flow of the gas sensitive TFT, (**b**) layout of the TFT, (**c**) photograph of the fabricated sensors on the flexible polyimide substrate [172].

So far, PI is one of the most appropriate substrates for flexible electronic devices. Actually, some electronic devices with PI-substrate displays have already been marketed. PI with its high process temperature, good compactness and mechanical strength has been widely studied for experimentation and commerce.

### 3.2. Flexible TFTs under Mechanical Stress

When bending flexible devices, mechanical stress will be generated as the substrate and films of the TFTs come under tensile or compressive strain. TFT properties will then also be degraded. Furthermore, when the radius of curvature and the mechanical stress increase beyond tolerance, cracks in the substrate emerge and TFTs will fail. Hence, it is necessary for researchers to comprehend the impact of mechanical stress on flexible device performance [173–183]. In fact, with the widely extending use of flexible applications, bending behaviors of the TFTs will become more and more complex. Three types of practical applications can be distinguished: the first involves a fixed bending radius, like Samsung Galaxy S mobile phones and curved TVs. In the second kind, the bending is mostly in one direction, like in wristband-like displays, wristwatches and flexible TVs. In the last one, bending occurs in any direction randomly, like in wearable electronics and skin sensors. In this section, bending test platforms and methods are introduced in Section 3.2.1. Then, the degradation of devices under the tensile and compressive strain is discussed in Section 3.2.2. Finally, two methods for the optimization of TFT design are introduced.

### 3.2.1. Bending Test Platforms and Methods

Some bending test platforms and methods are reported in References [36,175], which simulate the operation of flexible devices in real-world scenarios. Despite all of the differences in bending behaviors, TFTs suffer no more than the tensile or compressive strain from along with the channel length or the channel width as the mechanical process is applied. Figure 11 shows the four common types of bending test platforms: (A) the substrate between two moving metal splints can be bent to various radius [173], (B) the substrate is wrapped around a rigid cylindrical rods, which makes it easy to contact the electrodes with probes [158], (C) custom-built bending testers for flexible TFTs and displays [162], which includes a programmed counter, a dc motor and a jig. With this kind of testers, the number of bends on devices or displays can be counted conveniently. (D) An extreme bending test device is shown in panel D, where the critical radius of curvature of TFTs can be measured [155].

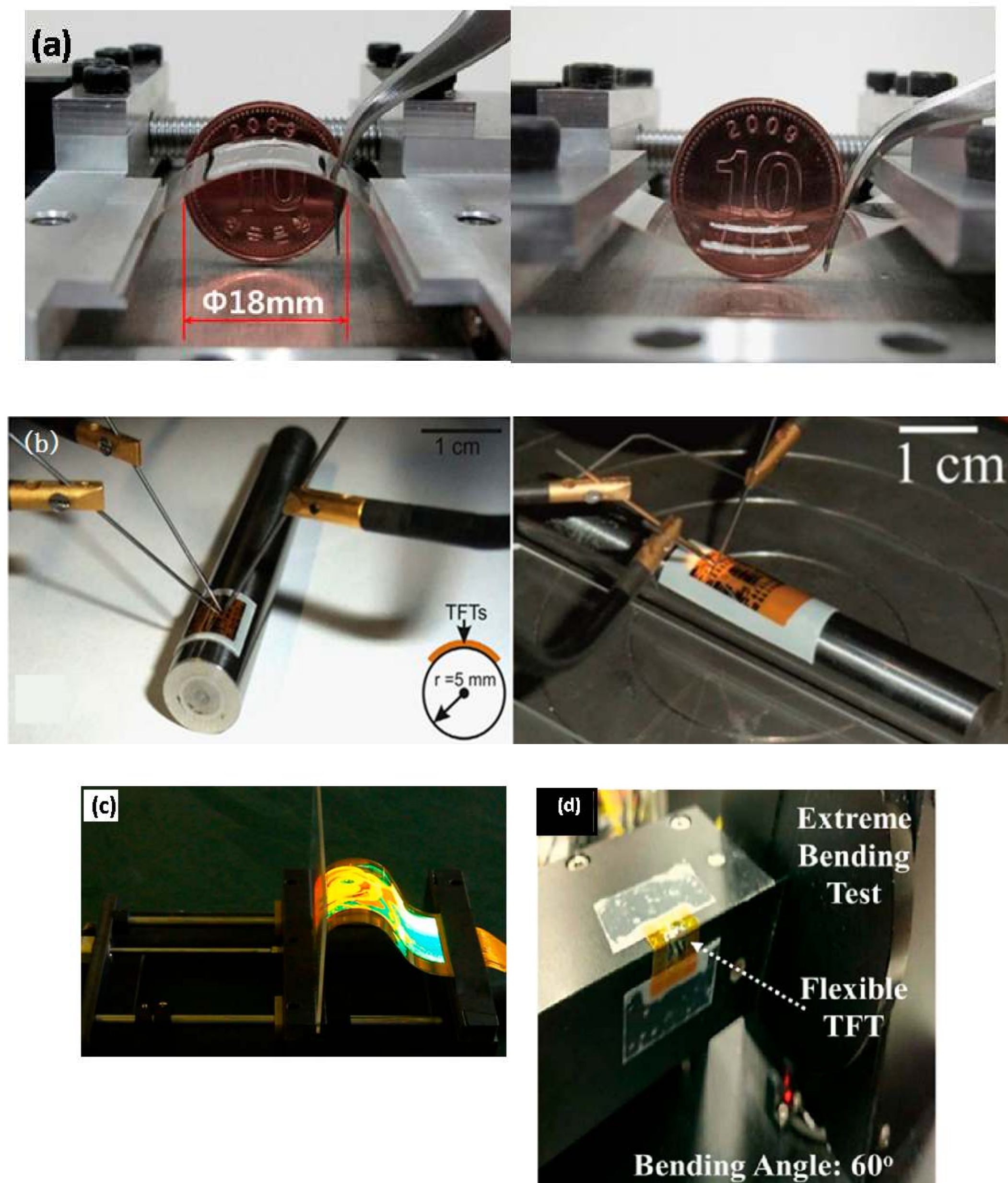


**Figure 11.** Bending test platforms (**a**) Substrate between two moving metal splints [173]. (**b**) Substrate wrapped around the rigid cylindrical rods [158]. (**c**) Custom-built bending testers [162]. (**d**) Extreme bending test [155].

### 3.2.2. Degradation of TFTs under Mechanical Stress

As shown in Figure 11c, displays bent in one direction are the most common in the market. When the substrates are bent inwards or outwards randomly, TFTs suffer tensile or compressive strain. Depending on the direction of the strain, either along the channel width or along the channel length, different device performances can be observed. In this section, the bending behaviors of strained TFTs are discussed.

Figure 12 shows two kinds of bending behaviors of IGZO TFTs [160]. In Figure 12a, the TFT was bent along with the channel width, while the TFT in Figure 12b was bent along with the channel length. For both cases, the values of the mobility and the threshold voltage were evaluated from the transfer curves measured at the various bending radii. As one can observe from Figure 12c, there was almost no degradation in the transistor performance until the bending radius was decreased to about 3 mm. When the bending radius dropped below 3 mm, TFTs bent along the channel width were more stable than those bent along the channel length. Meanwhile, the threshold voltage increased because of the stretching and thinning of the polymer dielectric layer.

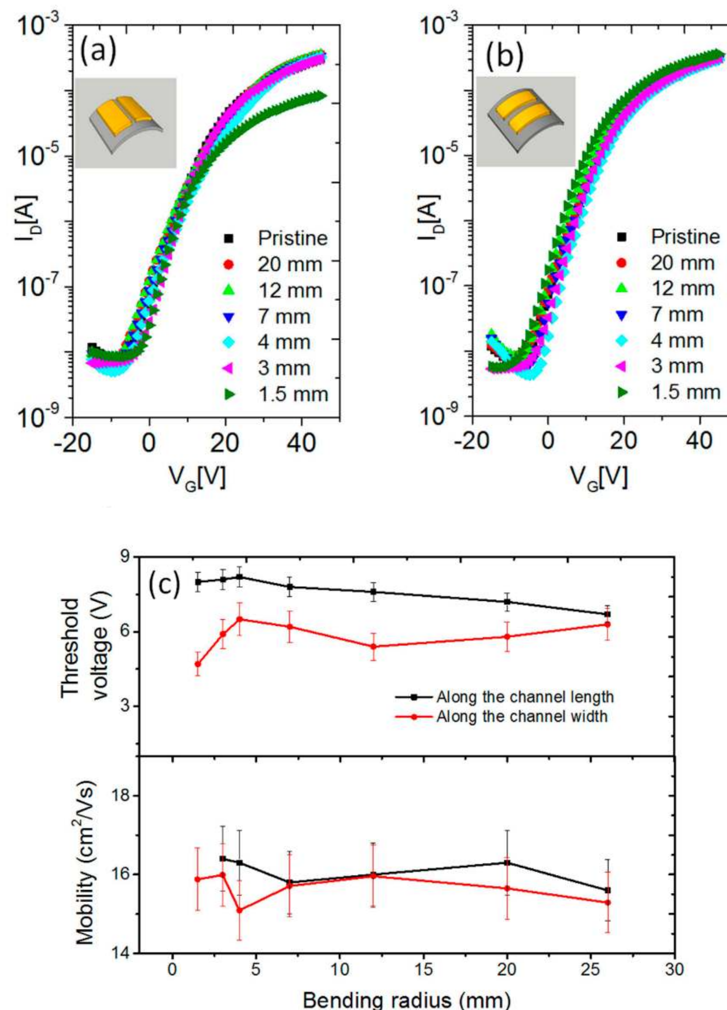


**Figure 12.** Two kinds of bending behaviors of IGZO TFTs and their transfer curves; (**a**) bending along channel width and (**b**) along the channel length at various bending radius. (**c**) The extracted, mobility and threshold voltage at various bending radius [160].

The results of the repeatability tests with four forms are shown in Figure 13a–d [160]. In Figure 13a,b the TFTs were bent along the channel width at a bending radius of 3 mm and 1.5 mm, respectively. In Figure 13c,d, the TFTs were bent along the channel length, also at a bending radius of

3 mm and 1.5 mm. The variations in mobility and threshold voltage values derived from the transfer curves in Figure 13a–d are shown in Figure 13e. In general, the TFTs bent along the channel width show better performance than those bent along the channel length.

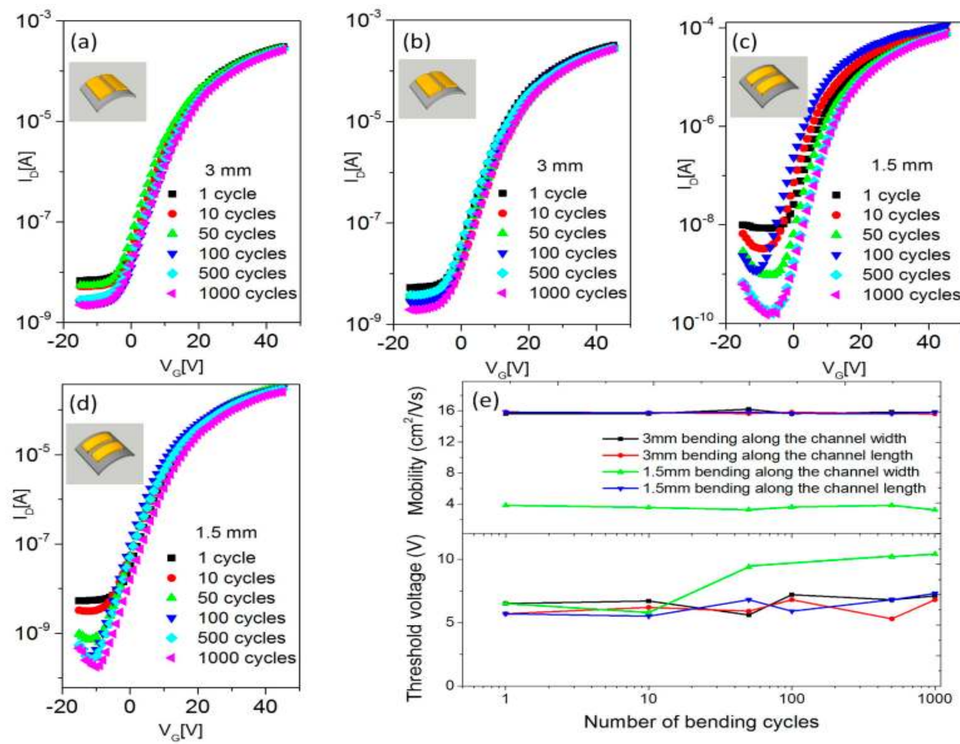


**Figure 13.** Transfer characteristics of TFTs repeatedly bent along the channel width and along the channel length with different radius: (**a**) 3 mm and (**b**) 1.5 mm as along the channel width, (**c**) 3 mm and (**d**) 1.5 mm along the channel length. (**e**) the mobility and threshold voltages as a function of the number of bending cycles [160].

Figure 14a shows pictures of TFTs in a flexible display under compressive ($\varepsilon < 0$) and tensile ($\varepsilon > 0$) strain as the display is being subjected to repeated uni-directional bending [162]. Kim and Münzenrieder et al. reported that the threshold voltage in Figure 14b and the TFT mobility in Figure 14c shifted to opposite directions under compressive and tensile strain [81].

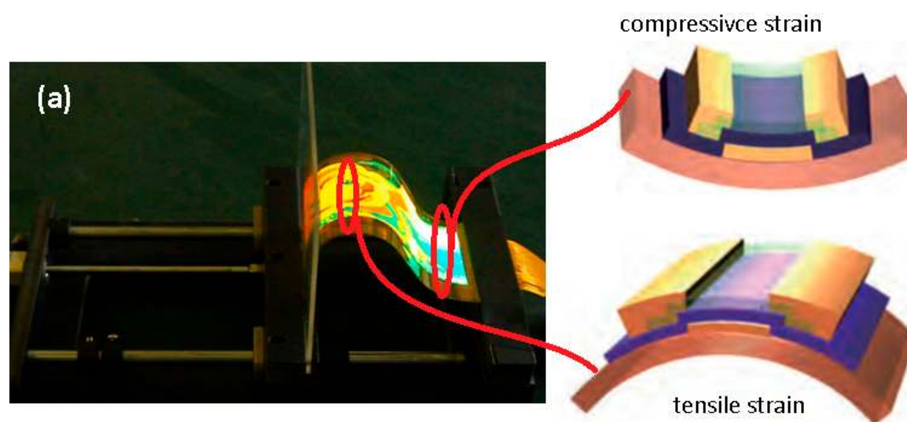


**Figure 14.** *Cont.*

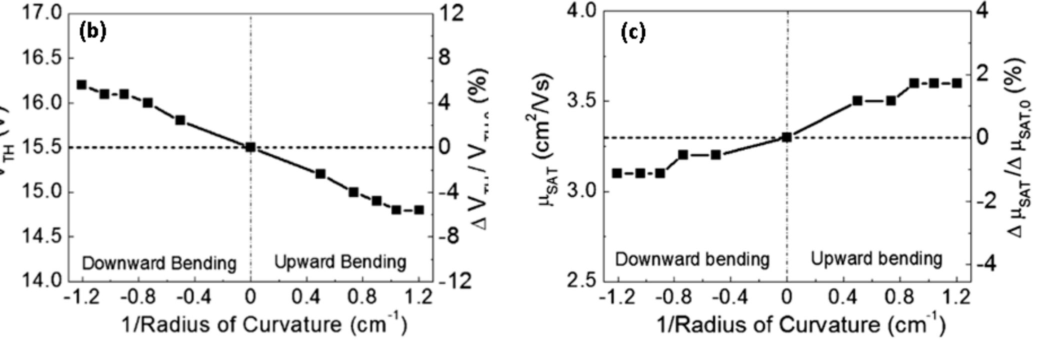


**Figure 14.** (**a**) variation of compressive and tensile strain with inverse bending radius [162], variations in $V_{TH}$ (**b**) and $\mu_{sat}$ (**c**) and their percentage variations [81].

With the help of such bending tests, it was found that the degradation of TFTs is dependent on the direction of the strain. This behavior can be accounted for by considering the impact of the piezoelectric effect on the transport behavior in the ZnO channel/gate insulator/gate region [81]. Figure 15a shows the effect of compressive strain on the TFTs, considering that a negative piezoelectric field affects the interface in a way that shifts $V_{TH}$ towards the negative and the mobility toward the positive values. In Figure 15b, the tensile stain generates a positive piezoelectric field between the ZnO channel and the gate insulator interface. The $V_{TH}$ and the mobility are then shifted into the opposite direction compared to the compressive-strain case. With this mechanism in mind, the changes in electrical transport behavior reported in Figure 14b, c can be reasonably explained.

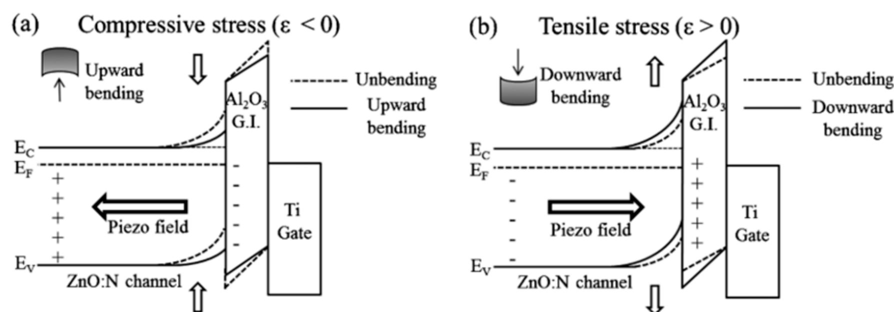


**Figure 15.** Electrical transport behaviors under two kinds of strains; (**a**) compressive stain and (**b**) tensile stain in flexible TFTs [81].

### *3.3. Optimized Ways for the Reduction of Mechanical Stress*

Since the performance of TFTs is compromised under mechanical bending stress, its impact needs to be minimized. To achieve this, two options are at hand: the first involves structure optimization of the TFTs and the second optimization of the device layout.

Turning to the first option, an additional layer can be applied to the top of the TFT device as reported in Section 3.1. Such devices exhibit good stability after 10,000 bending cycles. The experimental results show that the stress coming from the bottom films (closer to the substrate) can be effectively absorbed by the layer on top and thus protect the TFT device.

Secondly, in addition to structure optimization, changes in the TFT layout are another effective way to reduce the effect of mechanical stress. Such changes involve using different patterns for the design of each electrode and the active layer. Figure 16 [181] shows three different types of patterning: a TFT design with conventional S/G/D patterns (Figure 16a), a design with a conventional S/G/D pattern but a strip semiconductor layer underneath (Figure 16b). Both structures permanently fail as cracks occur on the electrode films after 5000 bending cycles.

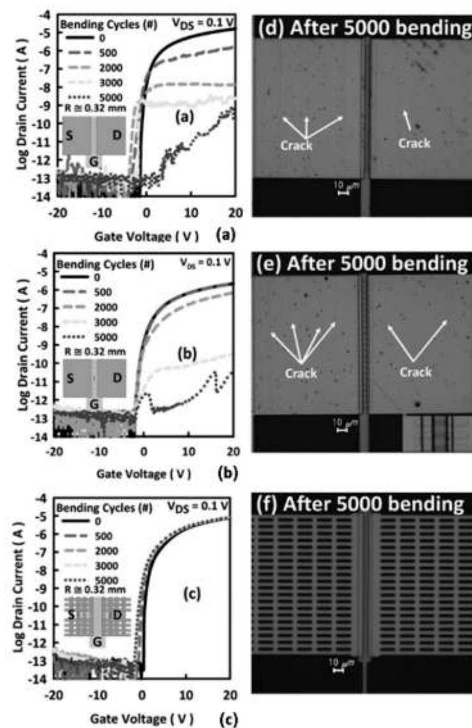


**Figure 16.** Three kinds of flexible TFTs for bending tests. Transfer curves and optical images of a-IGZO TFTs with (**a**,**d**) conventional structure with block electrode shape, (**b**,**e**) conventional block electrode shape and strip semiconductor layer shape, and (**c**,**f**) metal mesh electrode shape [181].

In comparison, a TFT with metal mesh electrodes and a strip semiconductor film underneath shows high mechanical stability without any cracks after bending.

As discussed in Section 3.2.2, TFTs bent along the channel width exhibit higher stability and performance than those bent along the channel length during the bending test. Hence, the layout of TFTs should be rationally designed along the channel width, especially in applications with fixed a bending radius and bending in one direction. While in the case of bending in any direction, a tradeoff in the TFT channel design should be considered. It is suggested that TFTs might achieve a relatively high performance when the channel of the TFT and the bending direction form an angle of 45 degrees. More effort is needed to demonstrate this possibility.

## 4. Summary and Outlook

Oxide-based TFTs can be fabricated on (1) rigid substrates like glass, foils; (2) flexible substrates like PI, PEN and PET. These excellent characteristics have caused oxide-based TFTs to become actively investigated for one of the most popular TFT technologies in flexible applications. In this review, we have mainly focused on recent advances for the oxide-based TFTs employing room temperature and low-temperature processes. Particularly, we have emphasized representative TFTs fabricated on PI, PEN, PET and other substrates. The detailed performance for oxide-based TFTs is described in Table 1.

The degradation of mobility and stability of TFTs originates from mechanical stress. Besides, the strain in films could also affect critical parameters such as the energy bandgap, dielectric behavior, and thermal conductivity. To reduce this degradation effect, two optimized methods have been introduced. One is the structure optimization of TFT and the other layout design optimization. With these methods, degradation could be reduced effectively.

Over the past ten years, the performance of flexible oxide-based TFTs has been enhanced step-by-step. To date, there are still many challenges hindering the development of commercial productions, including repeatability, reliability, uniformity in large areas. Particularly, repeatability

means after how many bending cycles on the flexible device we can still promise the full performance of the device. Reliability means to what extent flexible devices can sustain adverse environmental conditions, such as strong mechanical stress, humidity, as well as high and low-temperature. Finally, uniformity means what the size of the flexible display we could fabricate without any mismatch on TFTs or distortion on the display. After solving the mentioned issues, the prospect for mass production will be bright.

**Table 1.** Summarized performances for representative flexible oxide-based TFTs.

| TFTs | Threshold Voltage (V) | Mobility (cm$^2$ V$^{-1}$ S$^{-1}$) | On/Off Current | Subthreshold Swing (V dec$^{-1}$) | Channel Material | Substrate | Temperature (°C) |
|---|---|---|---|---|---|---|---|
| Reference [71] | 4 | 20 | $10^5$ | 0.26 | a-ZITO | PET | <150 |
| Reference [69] | 5.4 | 7.53 | $10^4$ | >2 | ZnO | PET | <150 |
| Reference [150] | 1.3 | 21.3 | $2.7 \times 10^7$ | 0.23 | AZO | PET | room temperature |
| Reference [151] | 2.85 | 8.0 | $2.51 \times 10^7$ | 0.23 | InGaZnO | PET | - |
| Reference [57] | 1.2 | 66.7 | $2 \times 10^7$ | 0.33 | TZO | PET | 80 |
| Reference [86] | 1.93 | 7.83 | ~$10^8$ | 0.24 | IGZO | PEN | 150 |
| Reference [124] | 5.5 | 4.1 | ~$10^8$ | 0.2 | IZO:F | PEN | 200 |
| Reference [154] | 4.1 | 15.5 | $2.2 \times 10^8$ | 0.2 | IGZO | PEN | 180 |
| Reference [156] | 2.48 | 12.87 | $10^9$ | 0.2 | IGZO | PEN | 150 |
| Reference [157] | 0.1 | 5.39 | $2 \times 10^5$ | 0.81 | LZZO | PI | 320 |
| Reference [158] | 0.95 | 10 | $2 \times 10^9$ | 0.069 | IGZO | PI | 150 |
| Reference [159] | −0.6 | 9.5 | $4.5 \times 10^8$ | 0.109 | IGZO | PI | 150 |

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