Resistance characterization for weak open defects

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Strong open defects can cause a circuit to malfunction, but even weak open defects can cause it to function poorly. Detecting weak opens is thus an important, but challenging, task. Characterizing weak opens can help researchers assess the need for delay fault tests.

THE NEED TO ELIMINATE malfunctioning or soon-to-be malfunctioning circuits makes defect detection a great concern in the semiconductor industry. As previous work based on inductive fault analysis (IFA) has shown, most defects in current technologies stem from undesired extra material or the lack of material deposition.[1,2] Circuit defects include bridging[3] and open defects. Here we focus on open defects.

Traditionally, open defects have been defined as unconnected nodes in a manufactured circuit that were connected in the original design. In general, killer defects cause such strong opens that they immediately affect the circuit's yield. You can find these opens by applying regular stuck-at patterns. However, open defects can also still connect the network's two end points, but only weakly, by introducing a higher-than-expected but finite resistance between the linked points.[4,5] Such weak opens still let the circuit function, but with degraded performance in the form of signal delay.[6] Thus, open defects can manifest themselves as resistive broken lines or as resistive vias and contacts. From a reliability and quality-engineering standpoint, weak opens are potential hazards because they can escape the Boolean testing stage.[7-10] To detect weak opens, engineers must apply more sophisticated test methods, such as delay fault testing. To substantiate the need for such tests, later in the article we show a positive correlation between the distribution of weak opens found in back-end defect monitors and the number of delay faults found in a small test chip.

Figure 1 shows an example of an open line and a via.

Detecting weak open-line defects

Our defect monitor is a yield evaluation monitor (YEM) manufactured in a six-metal-layer, aluminum-based 180-nm CMOS process. The monitor module is the well-known meander-comb structure.

We monitored 40 dies across the wafer for each of the six metal layers. In each die, we placed four instances of the meander-comb structure using four different spacings between the meander and the combs. We use the different spacings to compute the defect density distribution for bridging defects. The YEMs are labeled as MA*x*, MB*x*, MC*x*, and MD*x*, where *x* indicates the metal layer. R_{MA1} denotes the resistance of the metal 1 meander in structure MA1. Characterizing open defects depends on the

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metal meander width, which is the same for all four spacings. Fortunately, this is not a real restriction, because the meanders have minimum metal width, as does almost all the routing in our test chip.

The meander resistances differ because the four YEMs vary in length. Furthermore, because of process variations that affect the meander's height and width, the resistance values of a single YEM vary by 10% to 20%. These variations have a radial shape, with the highest resistance at the wafer's center and the lowest resistance at the edge.

To accurately detect weak open-line defects, we must eliminate the uncertainty introduced by process variations. To do this, our method correlates the resistance of a given monitor with the resistance of other structures from the same die. This method has two advantages:

- It provides a high resistance correlation (greater than 98%) between meander-comb structures of the same die despite the radial process variation that affects all structures. Figure 2 gives an example of R_{MA1} versus R_{MB1} and R_{MC1} (the resistances for metal 1 meander MA1 versus MB1 and MC1) with a correlation greater than 99%.
- It can detect small increases in resistance that cannot be found with fixed limits.

Distinguishing metal opens from shorts

We consider structures with points outside the correlation cloud (for example, structures with open defects) as potentially defective. However, a bridging defect can also cause an outlying

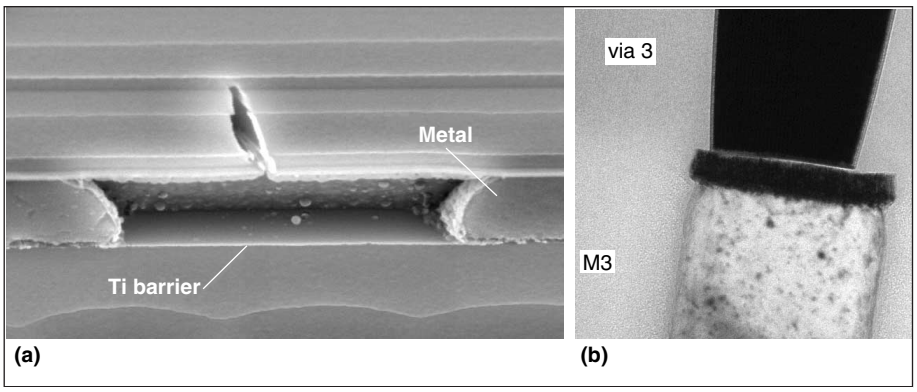

Figure 1. Examples of weak open defects: detailed cross section of a metal open line, showing the metal cavity and formation of a weak open defect due to the Ti barrier (a); and a resistive via (b).

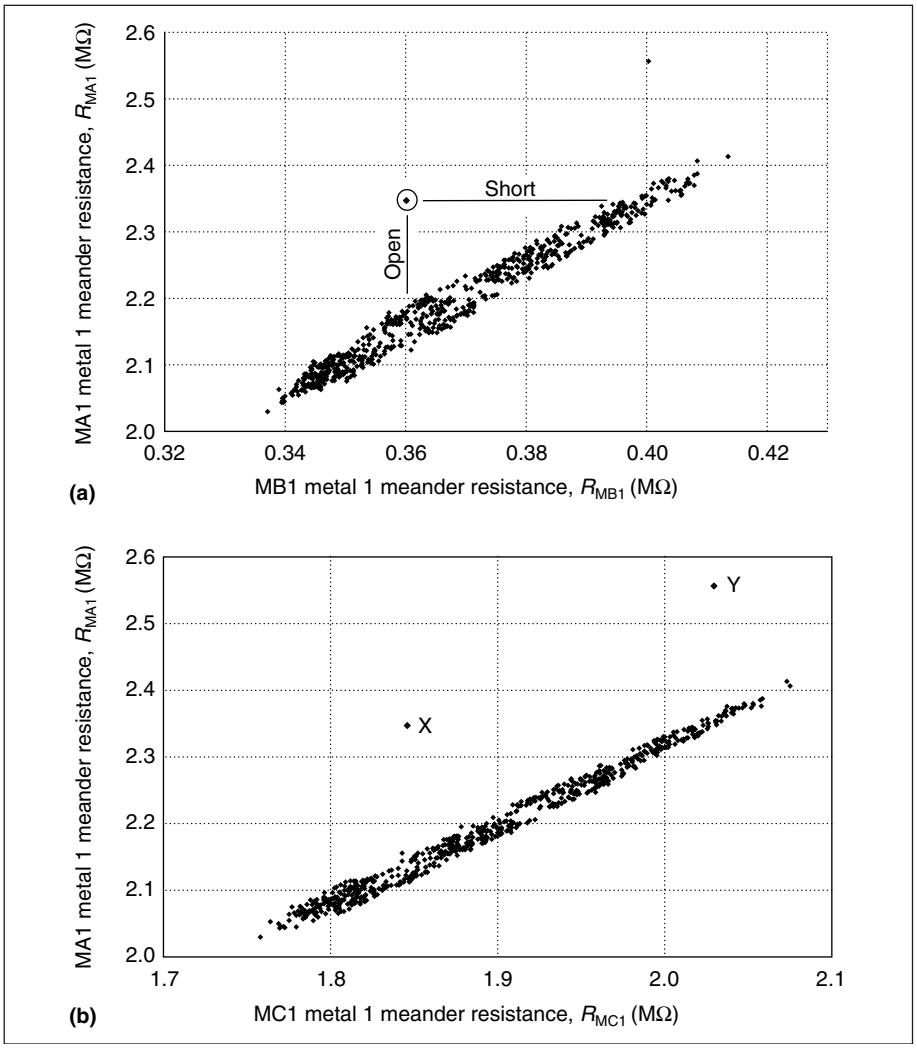

Figure 2. Correlation of meander resistances. An outlier can be an open in one meander (MA1) or a short in another (MB1) (a); correlating meander MA1 with meander MC1 shows that both outliers were actual weak open defects in module MA1 (b).

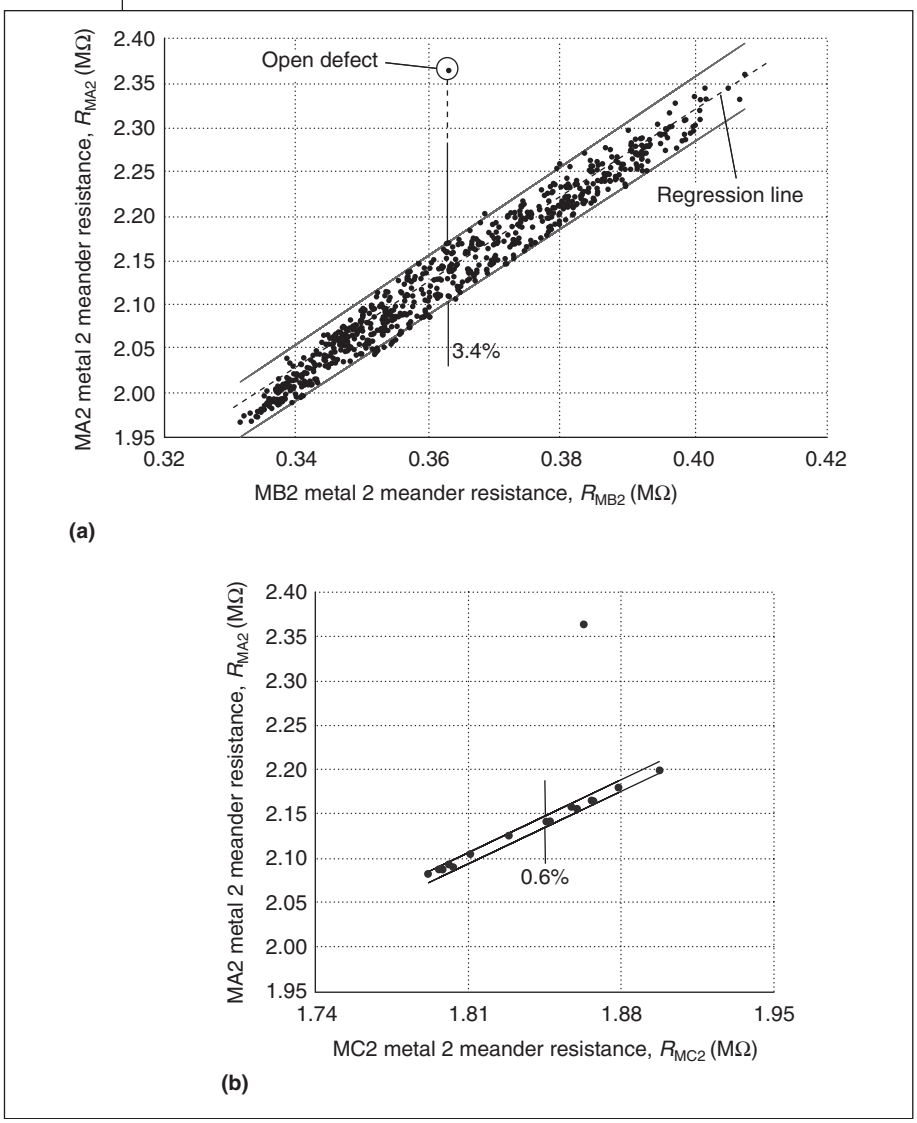

Figure 3. Extraction of a defect's resistance for an open line made in metal 2 (a), where the high correlation (98.4%) between structure MA2 and MB2 introduces an uncertainty of only 3.4%; the uncertainty improves to just 0.6% if we consider only dies located at the same (x, y) location (b).

point. As Figure 2a indicates, not only an open defect in meander MA1 but also a short between meander MB1 and its combs can cause an outlying point. A short can occur if the meander has two bridges to one of the combs, such that a part of the meander is bypassed through the comb. To distinguish these two cases, we compare the correlation of the suspected meander to another meander of the same die. Although we cannot detect a single short between the meander and a floating comb in this way, such shorts do not influence the distribution of opens.

Figure 2b illustrates two real open defects (points X and Y). Because the behavior of MA1 (the defective module) against both MB1 and MC1 is similar, we classify structure MA1 as having two open defects. Notice that this correlation method points not only to Y as an open defect (because it is beyond the fixed limits) but also to X. Fixed limits would not have found the latter defective module, because its resistance lies within the expected (and accepted) range of resistance values when accounting for process variations.

Accurate resistance estimation for weak opens

A closer look at correlation properties among defective structures can help us accurately extract the open-defect resistance. For most cases, the resistance of a defect-free meander varies by only 2% to 4% from its expected value. Figure 3a shows this range of uncertainty as the width of the band necessary to cover all data points—in this case, approximately 3% of the average value. The open defect's resistance is the difference between the outlying point's resistance and its corresponding vertical projection onto a regression line. The lines on either side of the band bound the accuracy of the estimated value.

For instance, consider the outlying point in Figure 3a. It corresponds to a resistance of 2.36 MΩ with a reference resistance of 2.14 MΩ ± 1.7% on the regression line. Thus, its estimated defect resistance is 220 kΩ ± 37 kΩ. Using only the measurements from the wafer containing the suspected defect will not reduce the width of the band. However, we can improve the uncertainty value by including only data within a given spatial region—for example, the wafer's circular zones—and stacking this information

for all wafers of the lot. Gathering data from only dies at the same (x, y) location reduces the uncertainty even further. Moreover, longer meanders decrease the width of the band more than shorter ones. Figure 3b illustrates these last two effects for the data set in Figure 3a. The band covering all points shrinks to 0.6% wide, yielding a more accurate estimate of the defect resistance value.

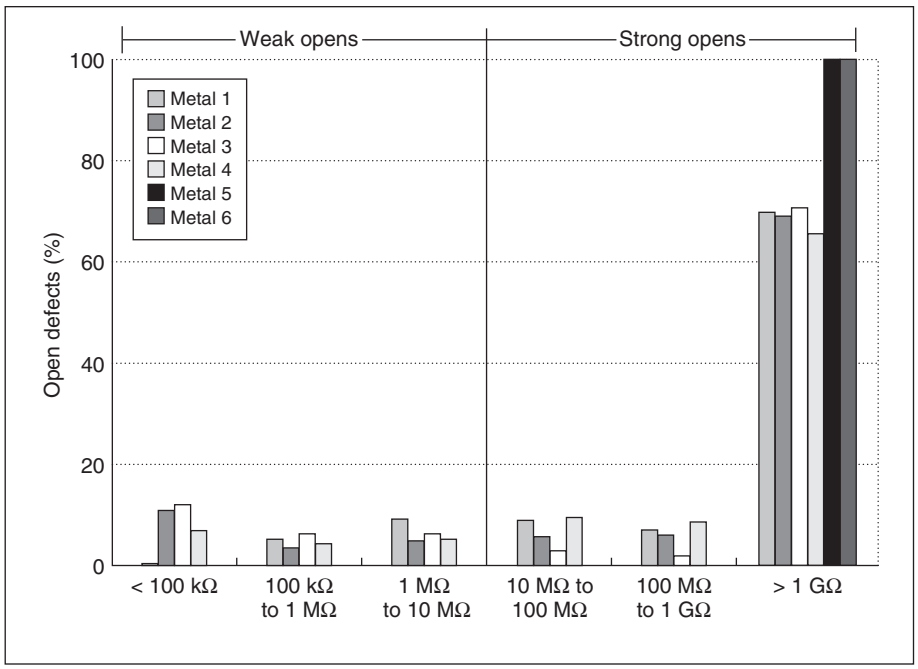

Figure 4. Distribution of metal open resistances.

Statistical distribution of weak open-defect resistances

We found the percentage of low-resistivity open defects for 7,440 dies (× 4 YEMs/die) and for each of the six metal layers, as shown in Figure 4. This corresponds to 186 wafers from 12 lots. In general, the average percentage of defective YEMs is less than 0.5%. We eliminated, from the analysis, dies that were consistently defective for all wafers, because such defects are most likely not due to random mechanisms.

Our research has found an important difference between metal layers: Because line width and thickness differ, the percentage of defective structures made of metals M5 and M6 is noticeably lower than for metals M1, M2, M3, and M4. The percentage of strong opens with resistances greater than 1 GΩ is more than 65% for all metal layers. All open defects in metals M5 and M6 belong to this range and behave as completely open lines. An important percentage of open-line resistances have values lower than 10 MΩ. Indeed, between 15% and 25% of metal layers M1 to M4 have resistances in this range.

Detecting contact and via opens

Our 180-nm CMOS process has three types of contacts: those to active, those to poly, and those to a local interconnect layer (LIL). Contact monitors consist of long contact chains connected by metal M1. The bottom layer could be n-active, p-active, p+ polysilicon, or LIL. Each chain has two million contacts and eight taps. We measured the contact chain's resistance for seven different lengths. Wiring connects the chains to pads, also contributing to the measured resistance. Our process control monitor (PCM) testers report the average resistance per contact for each measured chain length.

The via defect monitor is a chain of up to 4 million vias. As with the contact chains, multiple taps let us measure chain length resistance. The chains for vias 4 and 5 are shorter (1 million vias) due to the wider spacing of metals M5 and M6. Process variations affect not only the metal connecting the contacts and vias but also the contacts and vias themselves. Therefore, our detection method must compensate for the resulting huge spread in resistances of good contact and via chains, as well as for the added resistance of the pads and the interconnect.

Long contact and via chains can catch weak open contacts or vias that have a very low probability of occurrence, but can only determine the resistance with low accuracy. Short chains, on the other hand, can determine the resistance more accurately, but can only catch opens that have a high probability of occurrence. For example, the monitor cannot detect a weak contact of a few hundred ohms with an occurrence probability of a few parts per million (ppm). This is a limitation in the design of

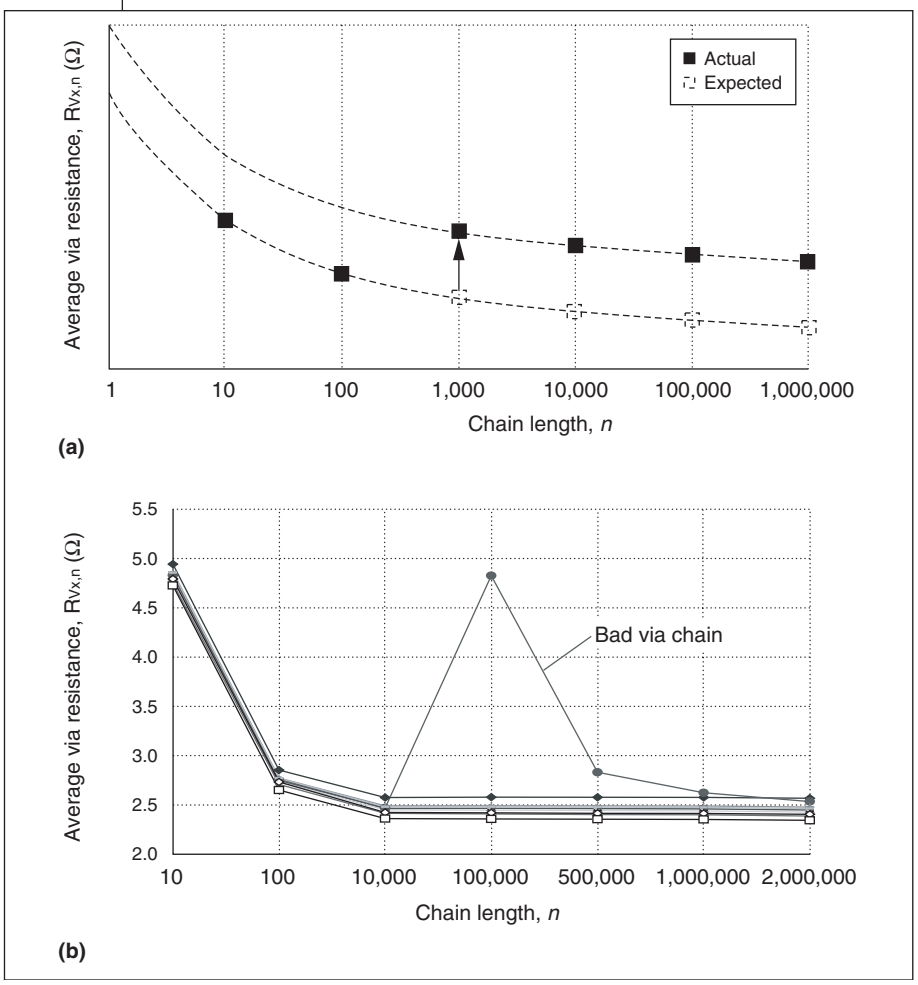

Figure 5. Via resistance characterization: abnormal behavior (solid boxes) versus expected behavior (open boxes) (a), and actual measured resistances for several sites, including one bad site (b).

the defect monitor. Our analysis distinguishes between three ranges of contact (or via) opens:

- Short chains let us accurately determine slightly elevated contact or via resistances.
- Medium chains let us detect vias and contacts with resistances between a few kilo-ohms and several mega-ohms. This group is the most harmful, because contacts and vias in this range can easily slip through a static stuck-at test, and fail during the actual product's normal operation—or worse, they could shorten a product's lifetime.
- Long chains let us detect completely open contacts or vias that determine the contact or via yield. (Such contacts and vias are outside this article's scope.)

Some of these weak opens are not caused by a via or contact, but rather by the metal connecting the via (or contact) chains. Only physical failure analysis can distinguish whether a metal open, a via, or a contact open is the cause of the open in the chain. We can compensate for this uncertainty by computing the probability of a metal open in a via chain using the percentage of metal opens in the comb-meander structures. Such computations show that in our case, metal opens explain less than a tenth of the via chain opens. Therefore, we decided not to compensate the number of via opens for the estimated number of metal opens in those chains.

Weak opens with low resistance

Our technique operates on individual chains for low-resistivity opens. It does not have to compensate explicitly for global process variations (we only observe single sites), but must compensate for the added resistance of the two pads and chain interconnect. For each via layer x and chain length n, the measured average resistance ($R_{Vx,n}$) is a function of each contact's or via's average resistance (R_{Vx}), and the resistance of the pads and interconnect (R_{pads}). Plotting the average resistance against the number of elements results in a hyperbola (see Figure 5a). By placing all chain measurements in such a plot, we can accurately determine R_{Vx} and R_{pads}. If a single weak contact or via occurs, the measured average resistance jumps. Figure 5b shows an example from actual data.

In theory, data from only three chain lengths are sufficient to determine the resistance of the weak via (two chain lengths to fit the curve, and one containing the weak open to compute its resistance). In practice, however, you should consider using at least four chain lengths because the pads, the interconnect, or bad con-

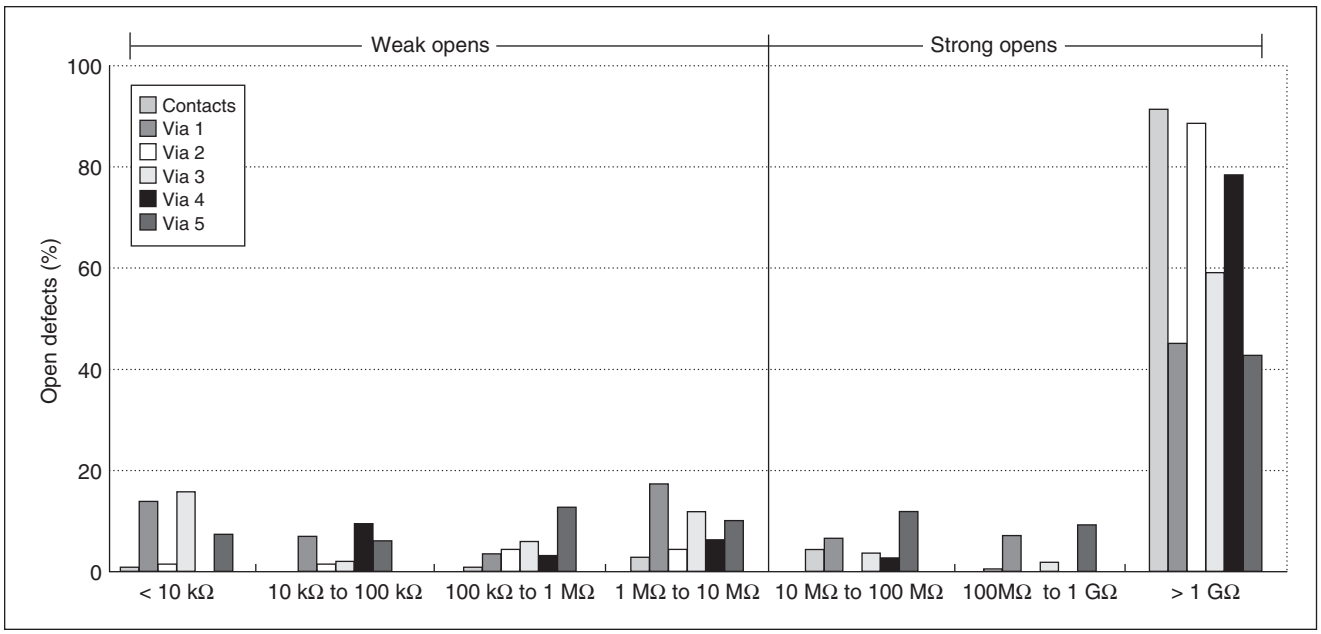

Figure 6. Resistance distribution for contact and via opens.

tacting can also cause a higher average resistance. If, after the jump in average resistance, at least two measured resistances fit on the new hyperbola, then it's likely that neither probing nor pads caused the jump.

This technique is applied only to short chains because systematic process variations in dense arrays of vias or contacts cause the measured resistance curve over the different chain lengths to deviate from the expected hyperbola.

Weak opens with medium resistance

For medium-resistance opens, we use a method similar to that used to detect metal opens. We correlate the resistance of one chain length (say 10,000 elements) against the resistance of a different chain length (say 100,000 elements) measured on the same chain. Plotting such points for all YEMs in a lot compensates for process variations.

Cloud width is typically 3% to 4%. Unlike with metal opens, we can now reduce the variation to 2% or 3% by observing only single-wafer measurements (eliminating wafer-to-wafer variation). Using measurements from the same site over all 25 wafers only marginally reduces the width of the band further. This reduction is less pronounced than for metal opens because a via chain's resistance depends on variations introduced while processing three layers (two metal and one via), whereas the meander resistance depends on processing only one layer.

Statistical distribution of open contact and via resistances

We analyzed four lots of 25 wafers each for open contacts, and three lots (also of 25 wafers each) for open vias. Figure 6 shows the distribution of open contacts and vias. Empty fields are due to the small sample size. Because there were so few weak open contacts per layer, we summarized all data in the "contacts" bar. For open contacts, the percentage of strong opens tends to be higher (more than 91%) than for metal open lines. Via results vary widely and depend on via type—from 52% for via 5 to 88% for via 2.

The incidence of weak open contacts is very small—below 5%. This corresponds approximately to a probability of weak contact failure of 10^{-9}, considering that there are on average 2 million contacts per structure. The resistance distributions of opens vary considerably for the different via layers. For vias 1, 3, and 5, the percentage of weak opens ranges from 35% to 41%, whereas for vias 2 and 4 the percentage decreases to 19% and 12%.

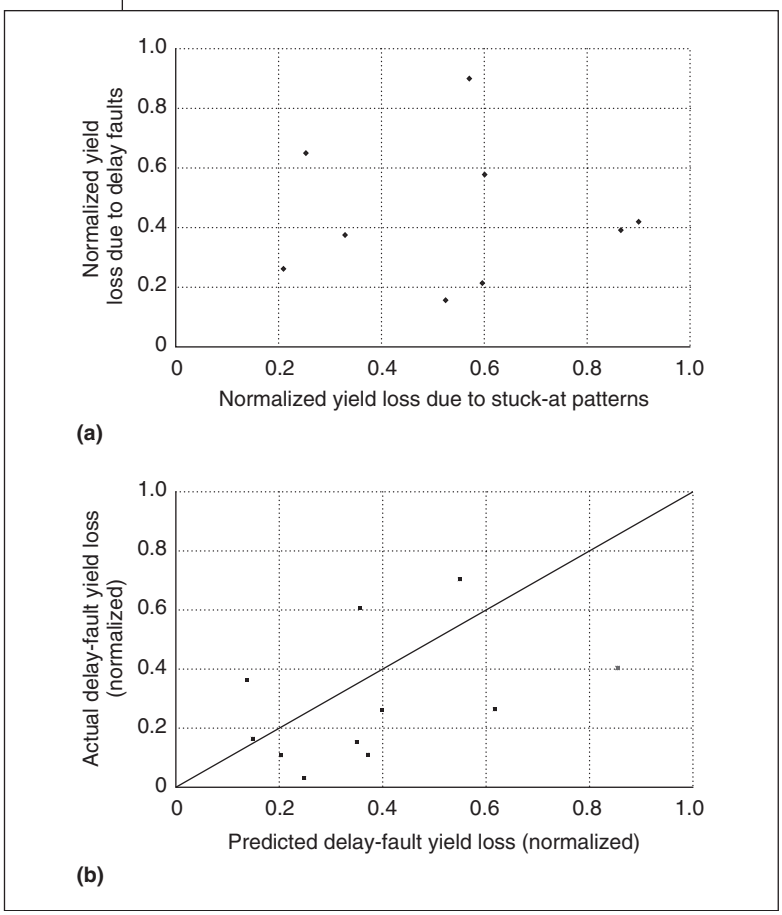

Figure 7. Correlation of normalized yield loss due to stuck-at patterns and delay faults (a), and predicted versus actual normalized yield loss due to delay faults (b).

Correlating delay faults with weak opens

To correlate delay faults (delays falling outside the correlation cloud) with weak opens, we used lots produced in a six-metal-layer, 180-nm CMOS process that have both the YEMs and a small test chip on a reticle. We computed the number of delay faults of six DSP cores in the test chip. All DSP cores that pass the stuck-at test undergo a delay fault test, which uses special patterns with two normal mode cycles between scan-in and scan-out. The active clock edge in the second normal mode cycle is varied relative to a fixed active clock edge in the first, so we can measure the minimum delay between them. We collected this data over the entire lot.

Offline, we plotted the measured delays for each device against the cycle time of a ring oscillator routed through one of the DSP cores. The number of delay faults was typically in the range of a few hundred ppms. Figure 7a shows the normalized additional yield loss due to delay faults obtained from nine lots. As the figure illustrates, the percentage of delay faults (*y*-axis) does not correlate with the chip's yield (*x*-axis). Thus, for this process, the predominant yield-killing mechanisms (metal shorts, for example) differ from the mechanism causing delay faults (weak opens).

Empirical estimates

We applied the techniques described in this article to determine the probability of a weak metal or via open in a DSP core. For each lot and metal layer, we first computed the probability that a piece of interconnect would be hit by a weak open (having a resistance below 10 MΩ). This is possible because our techniques give the number of weak opens per lot. We know both the length of the meanders in the YEM structures and the lengths of the interconnect in the DSP cores per metal layer, so we can compute the probability of a weak metal open for each metal layer of the DSP core.

We follow a similar procedure for the via levels. We used the methods described here to compute the probability of a weak open via (having a resistance between 10 kΩ and 10 MΩ) for each lot and each via level. Normalizing for the via chain lengths and then multiplying the resulting probability of failure (obtained from the normalization) by the number of vias in a DSP core gives the probability of a weak via for each via level. Combining the probabilities of a weak via and a weak metal open gives the probability of a weak open in the DSP core's back end.

Predicted versus actual data

We counted the actual number of delay faults in the DSP cores for 11 different lots. Next, we applied our procedure to obtain the estimated number of weak opens for every lot. Assuming that each weak open in the back end results in a delay fault, these two results should be correlated. Each point in Figure 7b is a lot prediction (*x*-axis) against the actual measured percentage of delay faults (*y*-axis). Both axes are normalized by the same factor; thus, the

order of magnitude of the data before normalization is the same. If the model describes the data perfectly, we should obtain the straight line shown.

Clearly, the correlation in Figure 7b is rather weak. The confidence interval is between –0.247 and 0.812. This probably stems from our limited delay-fault model and small data set. On the one hand, our prediction can be too low. We did not consider contact opens, resistive bridges, or the many front-end problems that can cause delay faults. On the other hand, our prediction can be too high. Metal opens can cause weak opens in via chains, creating a higher probability of failure. Furthermore, some weak opens cause a delay in a noncritical path, and the coverage of the delay-fault test might not be close to 100%.

Despite these shortcomings, it is clear that our prediction is in the correct order, and we can observe a trend: More weak opens result in more delay faults.

THIS EXPERIMENT verified the correlation between weak opens and delay faults. From this analysis, we can conclude that in modern deep-submicron technologies, the incidence of weak opens is high enough to require delay-fault testing. The resistance distribution of these weak opens is roughly flat if the resistance values are separated by an order of magnitude.

Our methods and results are obtained for a process with an aluminum interconnect. Although for copper-based processes the resulting resistance distributions could differ, the methods remain valid. ■

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