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Research Article

Resistance Switching Characteristics in ZnO-Based Nonvolatile Memory Devices

Fu-Chien Chiu

Department of Electronic Engineering, Ming Chuan University, Taoyuan 333, Taiwan

Correspondence should be addressed to Fu-Chien Chiu; fcchiu@mail.mcu.edu.tw

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Bipolar resistance switching characteristics are demonstrated in Pt/ZnO/Pt nonvolatile memory devices. A negative differential resistance or snapback characteristic can be observed when the memory device switches from a high resistance state to a low resistance state due to the formation of filamentary conducting path. The dependence of pulse width and temperature on set/reset voltages was examined in this work. The exponentially decreasing trend of set/reset voltage with increasing pulse width is observed except when pulse width is larger than 1 s. Hence, to switch the ZnO memory devices, a minimum set/reset voltage is required. The set voltage decreases linearly with the temperature whereas the reset voltage is nearly temperature-independent. In addition, the ac cycling endurance can be over 10^6 switching cycles, whereas, the dependence of HRS/LRS resistance distribution indicates that a significant memory window closure may take place after about 10^2 dc switching cycles.

1. Introduction

Developments of next generation nonvolatile memory (NVM) devices are required because the physical limitations of traditional Flash memory devices are approaching. In recent years, the resistance random access memory (RRAM) device has attracted a great deal of attention for the next generation NVM applications [1]. Since the RRAM technology is well compatible with the complimentary metal oxide semiconductor (CMOS) process [2], the scaling of RRAM devices may keep on in terms of the low power operation. This benefit will bring a strong cost-competitiveness to RRAM. In addition, the advantages of RRAM include small cell size, simple cell structure, high switching speed, high operation durability, multi state switching, and three-dimensional architecture [1–5]. The resistance switching behavior has been reported for a variety of materials such as perovskite-type oxides [1, 3], binary metal oxides [2–4], solid-state electrolytes [4], organic compounds [6], and amorphous Si [7]. In these RRAM materials being studied, binary metal oxides are most potential due to their simple constituents, good compatibility with CMOS processes, and resistive nature to thermal/chemical damages [2, 4, 8].

In this work, Pt/ZnO/Pt capacitors were fabricated and investigated for the NVM applications. The dependence of pulse width and temperature on set/reset voltages was examined. Experimental results show that a minimum set/reset voltage is required to switch the ZnO memory devices. The exponential decreasing trend of set/reset voltage with increasing pulse width is observed except when pulse width is larger than 1 s. The set voltage decreases linearly with the temperature, whereas the reset voltage is almost temperature independent. In addition, the resistance values both at high resistance state (HRS) and low resistance state (LRS) in different Pt/ZnO/Pt memory devices were characterized. The dependence of HRS/LRS resistance distribution on set/reset switching cycles indicates that the memory window begins to close after about 100 voltage sweeping cycles. Although the dc cycling endurance is detrimental, the ac cycling endurance over 10^6 switching cycles can be achieved.

2. Experiment

In this work, the sample structure of the resistive switching memory devices is metal insulator metal (MIM) capacitor, as indicated in Figure 1. The ZnO film was deposited on

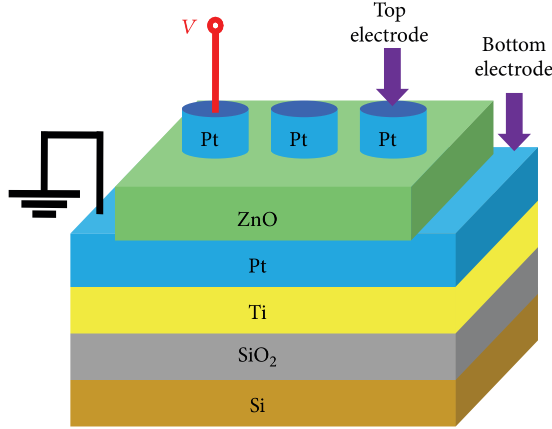

Figure 1: Schematic structure of Pt/ZnO/Pt and configuration of electrical measurement.

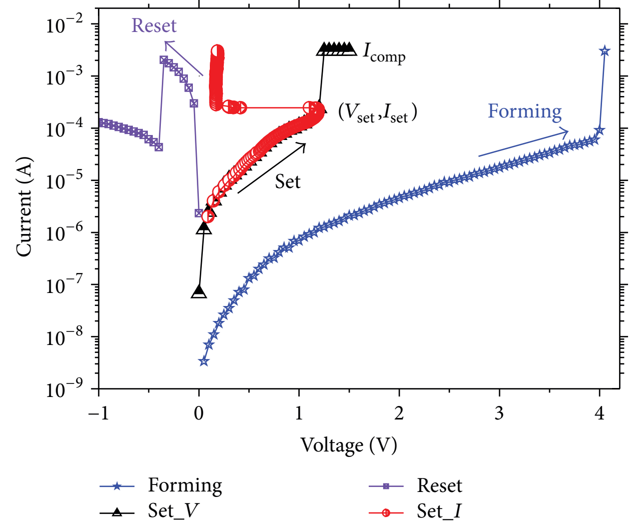

Figure 2: Typical current-voltage switching characteristics in Pt/ZnO/Pt memory cells. The set process can be performed by voltage sweep (Set_V) or current sweep (Set_I).

Pt/Ti/SiO_2/Si substrates by *rf* magnetron sputtering at room temperature. The ZnO film thickness is 25 nm. The sputtering power is 40 W. The working pressure is 5×10^{-3} Torr in Ar ambient with a flow rate of 25 sccm. Pt top electrode was then defined by *rf* magnetron sputtering through a metal shadow mask. The electrical properties of the fabricated Pt/ZnO/Pt memory devices were characterized under dark condition by using Agilent 4156C semiconductor parameter analyzer and Agilent 8110A pulse pattern generator, as well as Barth 4002 transmission line pulse generator. During the electrical characterizations, the bias voltage (or current) was applied on the top electrode with the bottom electrode grounded.

3. Results and Discussion

In this work, an initial forming process is required to achieve the bipolar resistance switching behavior on the virgin memory cells. Typical I-V switching characteristics in the Pt/ZnO/Pt memory devices are shown in Figure 2. The forming voltage is about 4 V. After the forming process, the memory device is in low resistance state (LRS). By sweeping the voltage in negative side without a current compliance (I_{comp}), the device current decreases suddenly at a reset voltage (V_{reset}) or a reset current (I_{reset}), and the device is switched from an LRS to an HRS. This event is defined as the reset process. Then applying the voltage in positive side, an abrupt increase of the device current takes place at a set voltage (V_{set}) or a set current (I_{set}). The V_{set} triggers the memory cell from an HRS to an LRS, which is defined as the SET process. Obviously, the $V_{set} \sim 1$ V should be larger than $V_{reset} \sim -0.5$ V, and the $I_{set} \sim 2 \times 10^{-4}$ A should be smaller than the $I_{reset} \sim 2 \times 10^{-3}$ A. Since the resistance switching depends on the polarity of applied voltage, the resistance switching in Pt/ZnO/Pt structure is bipolar. The bipolar resistance switching is also found in doped ZnO films with sulfur, cobalt, or manganese [9, 10] and in the structure of TiN/ZnO/Pt [11]. In addition, the unipolar resistance switching can be observed in the structures of Al/ZnO/Al [12] and Cu/ZnO/n^+-Si [13]. Even both unipolar and bipolar resistance switchings may coexist in the structure of Ag/ZnO/Pt [14]. The voltage-biased set process results in a sudden current jump at V_{set}, which causes the memory cell to switch from an HRS to an LRS. If, however, the set process is performed by the current sweeping, a negative differential resistance or snapback characteristic may be observed [15]. When the memory cell is switched from an HRS to an LRS at V_{set} (or I_{set}), the current transports through quite low resistance immediately due to the conductive filaments formed between two electrodes and then the voltage across the memory cell begins to decrease significantly resulting in the I-V snapback characteristic (indicated by Set_I) as shown in Figure 3. Accordingly, the current-biased set I-V curve is much different from the voltage-biased one after the onset of resistance switching from an HRS to an LRS, because the voltage will continue to increase during the voltage sweep mode (indicated by Set_V). Note that the I-V snapback phenomena can be often observed in the electrostatic discharge (ESD) protection devices [16] and even in ultrathin SiO_2 films [17]. Since the electric-pulse-induced resistance switching could be significantly affected by the ac voltage pulse width (W_{ac}), the relationship between set/reset switching voltage and W_{ac} was examined. In this work, both V_{set} and V_{reset} decrease with increasing W_{ac}. An exponential relationship between V_{set}/V_{reset} and W_{ac} can be observed for the condition of low W_{ac} (10^{-7} to 10^{0} s), as shown in Figure 3. Meanwhile, a critical threshold voltage is approached for large W_{ac} (>1 s) [4]. This implies that a minimum set/reset voltage is required to switch the ZnO memory devices. The thresholds V_{set} and V_{reset} are about 0.55 V and −0.25 V, respectively.

Figure 4 shows the temperature dependence of I-V characteristics both in HRS and LRS. Experimental results show that the device current increases with increasing temperature both in HRS and LRS. According to the temperature dependence of I-V characteristics [18], the conduction

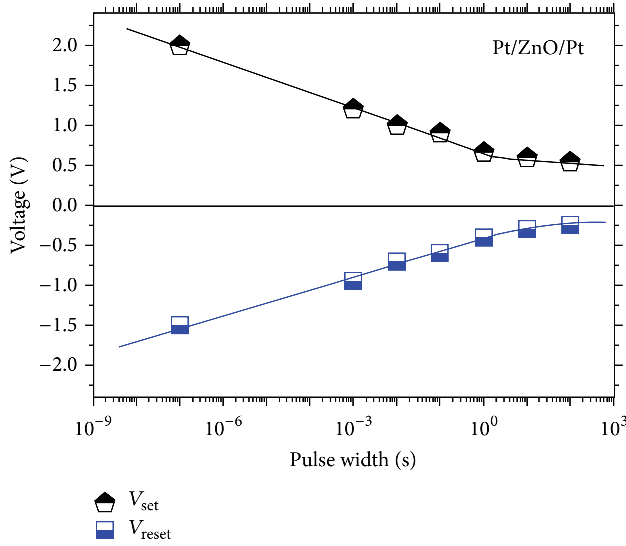

FIGURE 3: Dependence of ac voltage pulse width on set voltage (V_{set}) and reset voltage (V_{reset}).

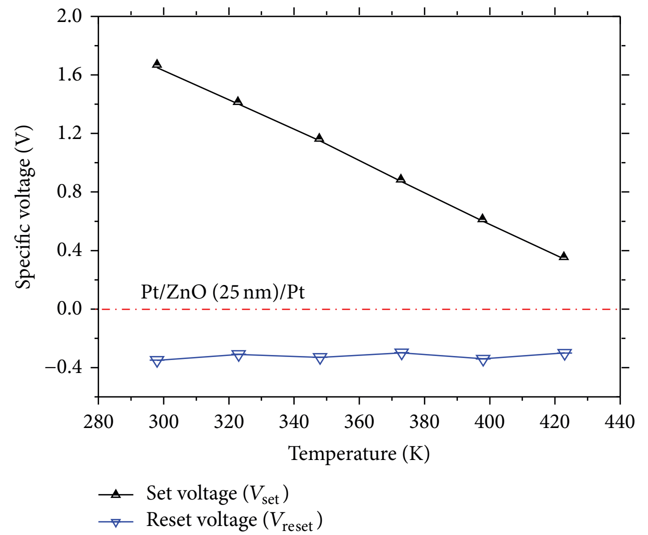

FIGURE 5: Temperature dependence of set voltage (V_{set}) and reset voltage (V_{reset}) on Pt/ZnO/Pt devices.

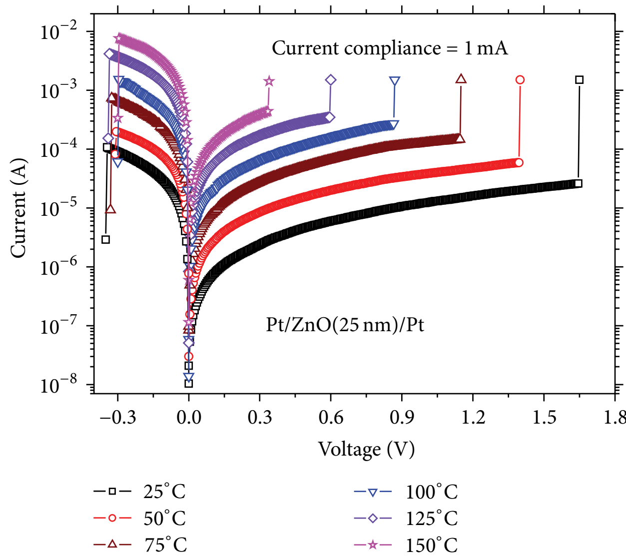

FIGURE 4: Temperature dependence of current-voltage characteristics on Pt/ZnO/Pt devices.

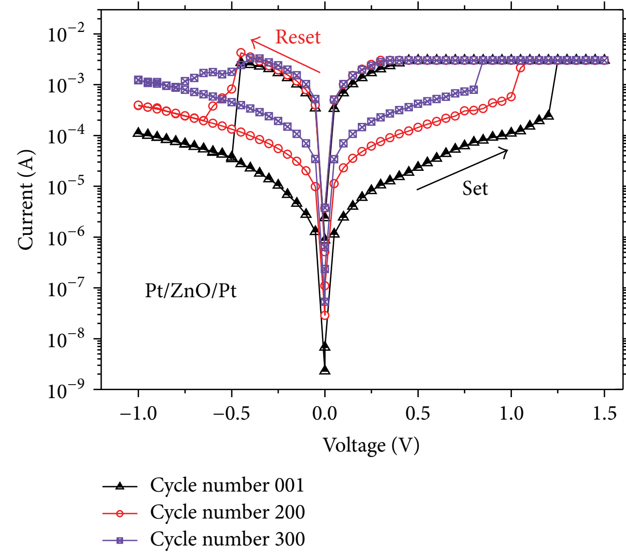

FIGURE 6: *I-V* characteristics before and after the test of dc cycling endurance performed by voltage sweepings at room temperature.

mechanism in Pt/ZnO/Pt structure is dominated by the hopping conduction in HRS. The hopping conduction is not the electrode-limited conduction mechanism but the bulk-limited conduction mechanism [19]. The electrode-limited conduction mechanism depends on the electrical properties at the electrode-dielectric contact. However, the bulk-limited conduction mechanism depends only on the properties of the dielectric itself. This may imply that the resistance switching mechanism in Pt/ZnO/Pt structure is not the interface type but the filament type. In addition, the device current is enhanced at the elevated temperature in HRS. Consequently, the switching voltage is lowered by the energy requirement of conductive filament formation. Due to the thermally assisted current conduction, the set voltage decreases with increasing temperature. Figure 5 shows that the set voltage decreases linearly with the temperature, whereas the reset voltage is almost temperature independent. The constant reset voltage is also observed during the dc cycling endurance tests performed by voltage-biased set/reset switching for the Pt/ZnO/Pt memory devices. Figure 6 shows the *I-V* curves before and after the test of dc cycling endurance performed by voltage sweepings at room temperature. The reset voltage during the test of dc cycling endurance keeps approximately constant. The uniform V_{reset} value suggests that the dominant reset process may result from the same rupture place in the conducting filamentary paths [3] leading to the dramatic current drop between both electrodes. Note that the I_{comp} of 3 mA was set to prevent the permanent breakdown of

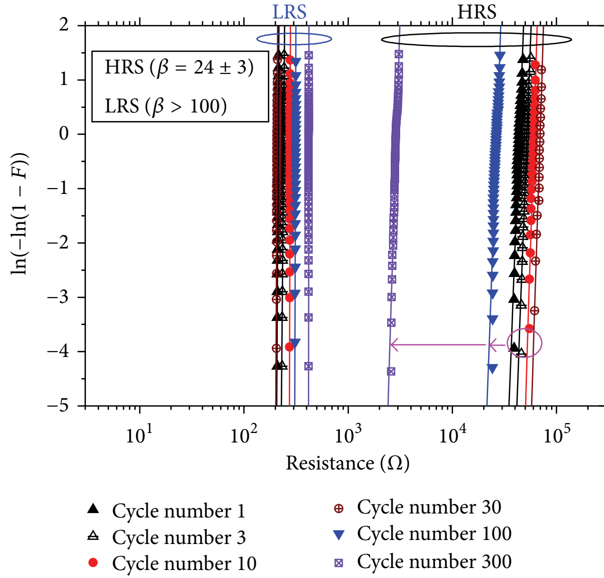

Figure 7: Weibull plots of HRS/LRS resistances during dc switching endurance for Pt/ZnO/Pt memory devices.

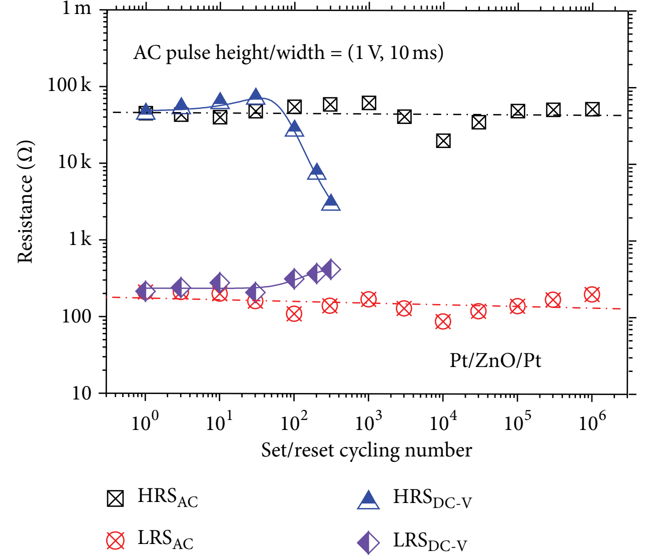

Figure 8: Memory window between HRS and LRS as a function of the number of dc/ac switching cycles for Pt/ZnO/Pt devices.

the memory devices during the set processes. On the contrary, no I_{comp} was set for the reset process. As shown in Figure 6, the HRS/LRS resistance ratio is on the order of 10^2–10^3 before the test of dc cycling endurance. Whereas the current in HRS increases after about 100 dc voltage sweeping cycles, which results in the change of HRS/LRS resistance ratio. Figure 7 shows the Weibull cumulative distributions of HRS/LRS resistance (R_{HRS} /R_{LRS}) values versus the cycle numbers of dc switching endurances for different Pt/ZnO/Pt memory devices. The Weibull distribution function is frequently used in semiconductor failure analysis and can be expressed as [20]

$$F(Q) = 1 - \exp\left[-\left(\frac{Q}{\alpha}\right)^{\beta}\right],$$
$$W(Q) \equiv \ln[-\ln(1-F)] = \beta\ln\left(\frac{Q}{\alpha}\right), \quad (1)$$

where $F(Q)$ is the cumulative distribution function of failure, Q is the resistance value either in HRS or LRS, α is the HRS/LRS resistance value at approximately 63rd percentile, and β is the Weibull shape factor, often called Weibull slope. Usually, $\ln[-\ln(1-F)]$ is plotted as a function of Q and this will yield a straight line. In this work, the Weibull slope (β) was estimated by the method of maximum likelihood estimation [21]. The β values for memory devices in LRS are very large, which means that the LRS resistance (R_{LRS}) values are extremely centered. As the dc switching cycles increase, the R_{LRS} nearly keeps constant even though R_{LRS} increases slightly with the switching cycle. Meanwhile, the β values for memory devices in HRS are much smaller than those in LRS. This means that the HRS resistances (R_{HRS}) have a relatively broad distribution. In addition, the R_{HRS} values begin to increase significantly after 100 dc switching cycles, as indicated in Figure 7. Therefore, the memory window begins to close after about 100 voltage-biased switching cycles. As indicated in Figure 8, the memory window between HRS and LRS is a function of the number of switching cycles. The dc cycling endurance is very detrimental, whereas the ac cycling endurance over 10^6 switching cycles can be achieved. In the case of dc cycling endurance, the dc forward sweeping voltage may set the memory device into the soft breakdown mode in which the dielectric is stressed by a large compliance current (3 mA). This high stress may result in the dielectric degradation and therefore memory window closing. As the test of ac cycling endurance, the switching between HRS and LRS is highly controlled, reversible, and reproducible. The memory window shows no degradation after 10^6 ac switching cycles, as shown in Figure 8. In this work, the alternate ac voltage pulses of +1 V and −1 V were applied per 10 ms in the test of ac cycling endurance. The relatively large pulse width (10 ms) was used for worse case. Experimental results showed that ac endurance could be at least higher than 10^6 switching cycles. This implies that the ZnO thin film is very potential in future nanoscale nonvolatile memory applications. Based on the cycling endurance tests, the serious reliability issue in the dc type is highlighted.

4. Conclusions

In summary, bipolar resistance switching characteristic was revealed in Pt/ZnO/Pt memory devices. The dependence of pulse width on set/reset voltages indicates that a minimum set/reset voltage is required to switch the memory cells. The set voltage decreases linearly with the temperature, whereas the reset voltage is nearly temperature independent. The dependence of HRS/LRS resistance distribution shows that the memory window closure may occur after about 100 dc switching cycles. The ac cycling endurance shows that no

degradation is observed after 10^6 cycles, which is potential in future nanoscale nonvolatile memory applications.

Conflict of Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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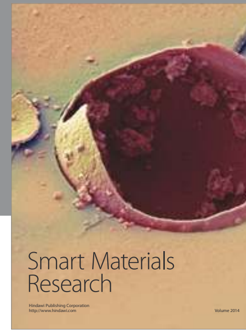
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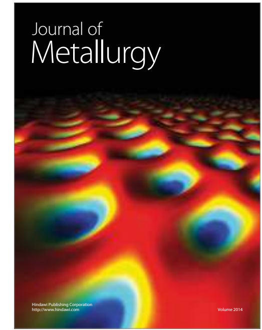
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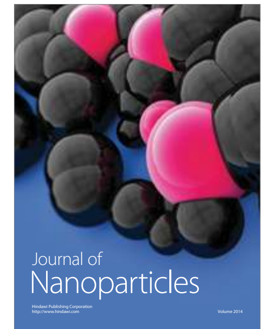
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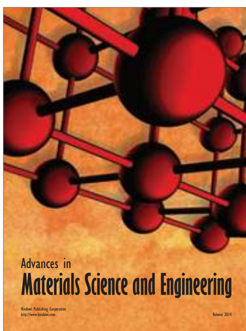
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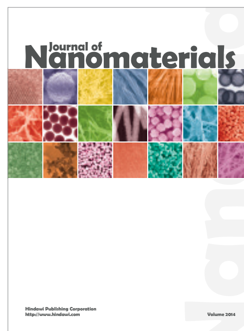
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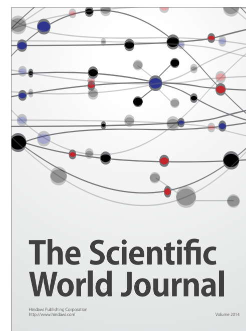
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