Resistive FET Mixer Conversion Loss and IMD Optimization by Selective Drain Bias

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***Abstract*—This paper describes a dedicated nonlinear MESFET model, which was used to accurately represent the device's drain–source current nonlinearity. An analytical expression is proposed, based on the Shockley approach, with good derivative reproduction. The evolution of the $Ids(Vgs, Vds)$ Taylor-series-expansion coefficients across $V_{\rm GS}$ and $V_{\rm DS}$ revealed not only the presence of important minimum conversion loss bias, but also of in-band intermodulation distortion sweet spots that have been used to optimize an FET resistive mixer performance. Some previously reported experimental results are also discussed through the use of the derivatives, and an alternative topology is considered for resistive mixers working on the border between the linear and saturated regions.**

***Index Terms*—Intermodulation distortion, MESFET's, mixers, modeling, Volterra series.**

I. Introduction

TODAY, there are many multitone digital telecommunications systems demanding very high dynamic range components, such as amplifiers, mixers, or switches. In the design process, this not only means good noise performance, but also high linearity or low in-band intermodulation distortion (IMD) levels. Recently, it has become clear that the empirical nonlinear models usually adopted to represent FET devices could not be used to produce accurate IMD calculations. The weakly nonlinear nature of these transistors has determined the limitations of models not conceived to fit the device's current/voltage (I/V) and charge/voltage (Q/V) derivatives [1].

The small-signal distortion is caused by nonlinearities in the neighborhood either of an invariant bias point for switches and amplifiers or of a time-varying LO "bias point" for mixers. These nonlinearities can be ideally and, respectively, represented by an invariant or time-varying Taylor-series expansion. Thus, a specific model for IMD prediction in amplifiers and switches would need to reproduce the nonlinear characteristics and their derivatives around the specific bias point, while an adequate model for the same purpose in a mixer must reproduce them over the entire LO range [2].

Specific techniques for IMD characterization of MESFET's and HEMT's have subsequently appeared, which are increasingly accepted by microwave circuit designers. The procedures for a direct experimental extraction of some [3] or all [4] of the $Ids(Vgs, Vds)$ Taylor-series coefficients in the following equation are perhaps the most significant examples since this nonlinearity is mainly responsible for the device's small signal (linear or weakly nonlinear) behavior:

$$\begin{aligned} &Ids(Vgs, Vds) \\ &\quad = Ids(V_{\rm GS}, V_{\rm DS}) + Gm1 \cdot Vgs + G_{\rm ds} \cdot Vds \\ &\qquad + Gm2 \cdot Vgs^2 + Gmd \cdot Vgs \cdot Vds + Gd2 \cdot Vds^2 \\ &\qquad + Gm3 \cdot Vgs^3 + Gm2d \cdot Vgs^2 \cdot Vds \\ &\qquad + Gmd2 \cdot Vgs \cdot Vds^2 + Gd3 \cdot Vds^3. \end{aligned} \tag{1}$$

Besides the obvious help these procedures have brought in computer-aided design (CAD) of nonlinear microwave circuits, they have also revealed unexpected MESFET IMD bias and load sweet spots in the saturation zone that have already been used in the design of very high dynamic-range amplifiers [4]–[6].

In the linear region, few important results have been reported [7]–[10]. Most of them have dealt with a simplified output conductance description of the drain–source current nonlinearity for IMD prediction in cold FET applications (switches and resistive mixers). Although interesting points have been presented, the cross terms' influence on IMD behavior is still unclear. Considering that these applications take full advantage of the gate–voltage-controlled channel resistance (an effect represented by $Gmd \equiv \partial G_{\rm ds}/\partial Vgs$), a complete $Ids(Vgs, Vds)$ expansion should give us a more accurate nonlinear description than the one currently available.

In the models' field, some continuous expressions have been reported in significant papers [3], [11]–[14] for an accurate IMD description. Most of them reproduce the transconductance derivatives in the saturated region, although they do not perform very well in the linear region or with varying load conditions. Others, e.g., [8], provide a specific output conductance description only in cold FET operation. A few of them, however, have acceptable performance in the whole working range.

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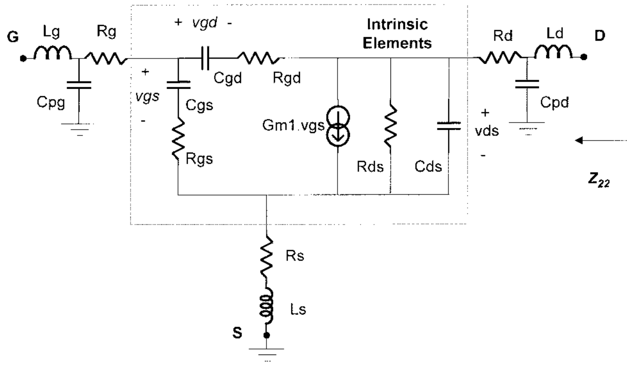

Fig. 1. Small-signal MESFET equivalent circuit.

In this paper, the experimentally extracted Ids derivatives will be shown for a typical MESFET device in its whole linear region. With a complete characterization of this nature, important conclusions may be drawn. For example, a very interesting set of bias points with null third-order derivatives will be associated with the transition between the linear and saturated regions. An analytical model, based on the classical Shockley approach, will then be proposed as a useful tool for accurate IMD control, either with bias or load condition, in different applications working in different regions.

A resistive mixer will be extensively analyzed. The presence of both optimum conversion-loss gate-bias and drain-bias induced sweet spots will be related to the derivatives' behavior and will be predicted with our model. Some interesting experimental results reported in [15] will also be explained through the knowledge of derivatives, and will allow us to discuss a nonclassical mixer topology.

In Section II, we will consider the derivative extraction, to continue in Section III with the model development. Sections IV and V will deal with the classical resistive mixer, to introduce in Section VI a brief analysis of the mentioned alternative topology.

II. Nonlinear Characterization Results

A. Extrinsic Resistances

Extracting the complete set of $Ids(Vgs, Vds)$ derivatives in the linear region is much more difficult than in the saturated region. The first reason for this complexity is due to a different degree of propagation of the errors that could appear in the extrinsic extraction procedure. Most of the existing techniques for extracting the small-signal circuit elements in Fig. 1 make a first extraction of the bias-independent extrinsic elements in order to directly derive at each bias point the intrinsic elements from the corresponding measured S-parameters.

The approximate expression in (2) for the real part of Z_{22} at low frequencies (capacitors as opens and inductors as shorts), gives us the possibility of considering the Rds sensitivity to errors in the extrinsic resistances Rs and Rd as follows:

$$\mathrm{Re}\{Z_{22}\} \approx Rs + Rd + Rds \tag{2}$$

$$\frac{\Delta Rds}{Rds} \approx \frac{-\Delta(Rs+Rd)}{Rds}. \tag{3}$$

It is quite evident that, when extracting Rds from Z_{22}, the sensitivity of this parameter to deviations in either Rs or Rd would be insignificant for relatively high Rds values (as in saturation) while it is critical for Rds values of the same order of magnitude (the linear region case for V_{GS} above pinchoff).

As the second- and third-order derivative extraction is based on the consecutive solution of the first-, second-, and third-order equivalent circuits, employing the nonlinear current technique of Volterra-series analysis [16], [17], the deviations in Rds will strongly propagate to the higher derivatives [18].

The technique in [19] with the $Rs + Rd$ equation of [20] obtained from S-parameters, gave us the best results. As each second- and third-order coefficient is related to the ones of the previous order by a differentiation operation (4), we have the possibility of detecting errors in Rs and Rd by a close examination of the experimentally extracted derivatives as follows:

$$\begin{aligned}
Gm2 &\approx \frac{1}{2}\cdot\frac{\partial Gm1}{\partial Vgs}\\
Gmd &\approx \frac{\partial Gm1}{\partial Vds} \approx \frac{\partial G_{\mathrm{ds}}}{\partial Vgs}\\
Gd2 &\approx \frac{1}{2}\cdot\frac{\partial G_{\mathrm{ds}}}{\partial Vds}\\
Gm3 &\approx \frac{1}{3}\cdot\frac{\partial Gm2}{\partial Vgs}\\
Gm2d &\approx \frac{\partial Gm2}{\partial Vds} \approx \frac{1}{2}\cdot\frac{\partial Gmd}{\partial Vgs}\\
Gmd2 &\approx \frac{\partial Gd2}{\partial Vgs} \approx \frac{1}{2}\cdot\frac{\partial Gmd}{\partial Vds}\\
Gd3 &\approx \frac{1}{3}\cdot\frac{\partial Gd2}{\partial Vds}.
\end{aligned} \tag{4}$$

B. Derivative Behavior

By using the two-sided harmonic measurement setup (already presented and discussed in [4] and [21]), and with the remarks of the above subsection, the authors have completely characterized the predominant drain–source current nonlinearity of a general-purpose MESFET of 6 μm $\times$ 50 μm gate periphery, which exhibits a pinchoff voltage of nearly -1.35 V and an $Idss$ of 50 mA.

In Fig. 2, we show the derivatives' surfaces for the first-, second-, and third-order coefficients for the whole linear region and part of saturation (V_{GS} values from below pinchoff up to 0 V, and a V_{DS} range between 0–1.5 V). The authors have not found any previous complete nonlinear characterization of this kind.

Some important conclusions can be drawn from these surfaces. We have detected two sites of interest: one corresponding to the pinchoff evolution and another to the linear-to-saturation border. The first site, represented with a broad discontinuous line, contains a set of V_{GS} and V_{DS} points where the second derivatives have a peak and the third derivatives a null. In Fig. 3(a), these points represent the well-known pinchoff modulation with the drain–source voltage. Since the pinchoff is of soft nature, it can not be precisely defined by

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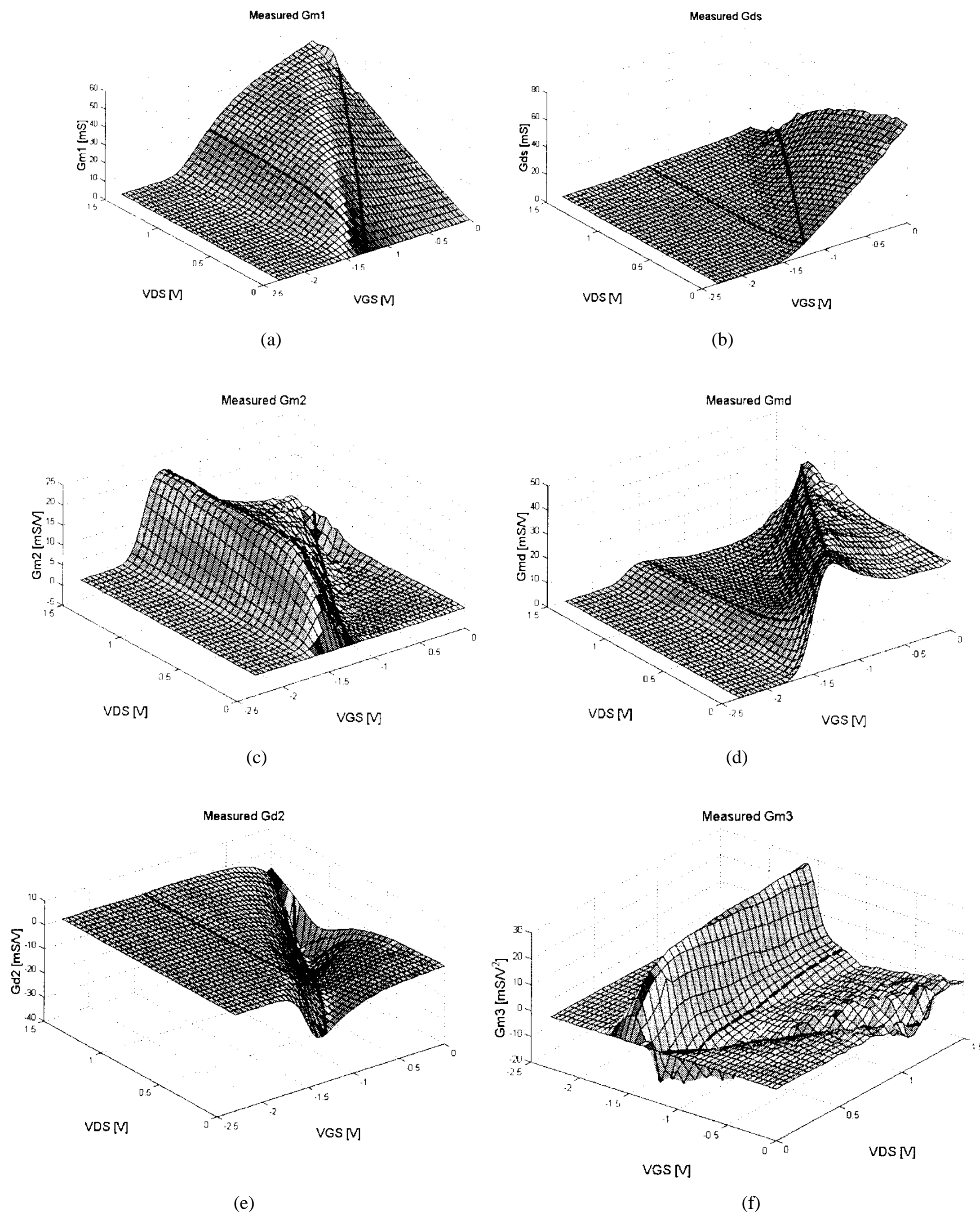

Fig. 2. Extracted $Ids(Vgs, Vds)$ derivatives. (a) $Gm1$. (b) $G_{\rm ds}$. (c) $Gm2$. (d) Gmd. (e) $Gd2$. (f) $Gm3$. Thick lines representing the cutoff and linear-to-saturation transitions.

a step in $Gm1$ and $G_{\rm ds}$, but as an inflection in the first-order coefficients along the $V_{\rm GS}$ direction. The second site has been emphasized with a continuous broad line. This set of $V_{\rm GS}$ and $V_{\rm DS}$ points also corresponds to a peak in the second derivatives and a null in the third ones. They represent in Fig. 3(b) the border between the linear and saturated regions, a soft border (not abrupt) and, consequently, with a change of curvature in the first-order terms.

Both sites are strongly nonlinear, but with a quadratic nature revealed by a high magnitude of the second derivatives and a null in the third-order ones. Such a strong nonlinear behavior is not always adverse, and we will deal with it below.

III. A Modeling Approach

If extracting the derivatives in the linear region can be a complex task, trying to reproduce them with an analytical expression may be even worse. Extending well-known and robust expressions [11]–[12], [14] to the derivative fitting in the linear region can be limited by the use of the hyperbolic tangent function, which generally determines a null of $Gd2$ in cold FET operation, an unreal situation. A general power law [13] conceived from the linear region leads to a better starting point and has recently been considered as an excellent way to improve the distortion prediction in cold FET operation

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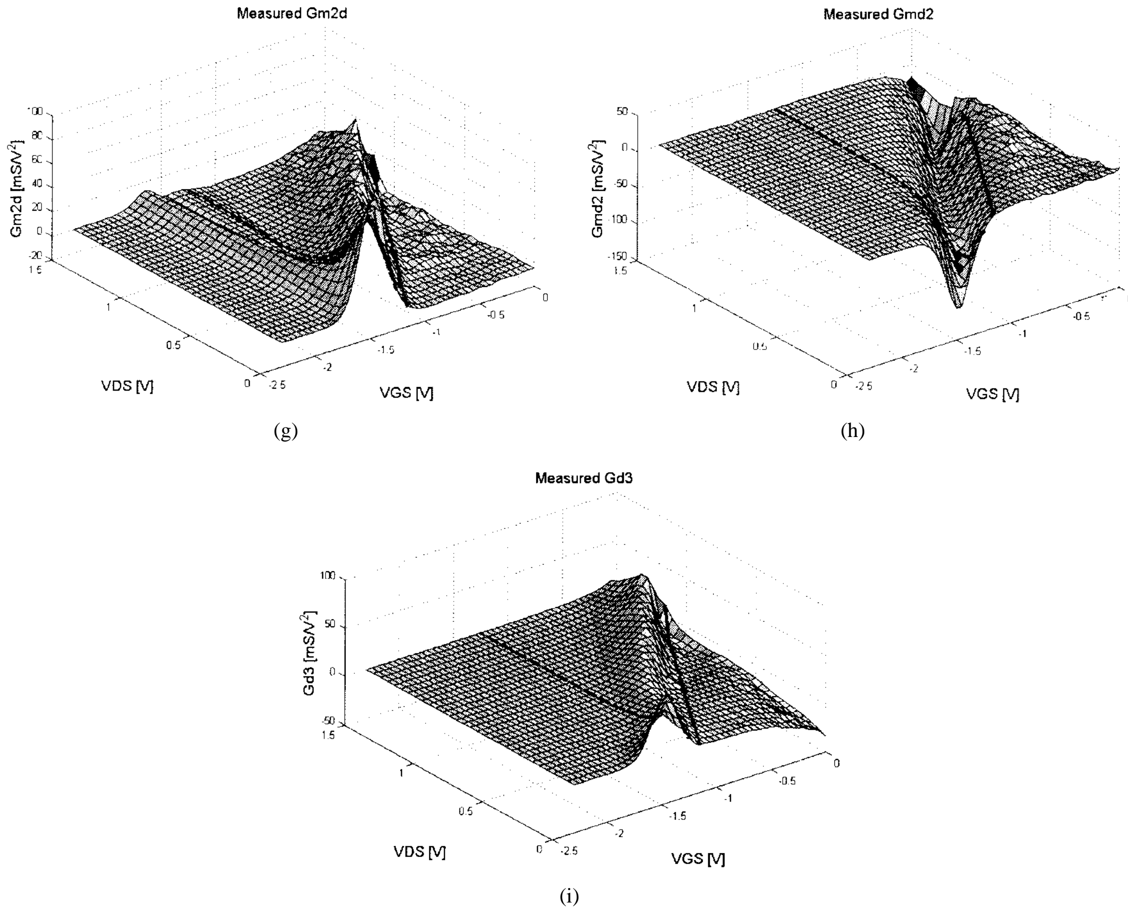

Fig. 2. *(Continued.)* Extracted $Ids(Vgs, Vds)$ derivatives. (g) $Gm2d$. (h) $Gmd2$. (i) $Gd3$. Thick lines representing the cutoff and linear-to-saturation transitions.

[22]. The modified Shockley approach [8] could also be quite interesting with some new arrangements to avoid the problems outside the linear region.

We decided to employ a philosophy similar to [13], and to take the starting point in a robust approach for this region, the elegant Shockley solution [23] reproduced as follows:

$$Ids = Go \cdot \left\{ Vds - \frac{2}{3}\left[\frac{(Vds+\phi-Vgs)^{3/2}-(\phi-Vgs)^{3/2}}{(\phi-Vp)^{1/2}}\right]\right\}. \tag{5}$$

This expression is limited for $Vp < Vgd < \phi$ and $Vp < Vgs < \phi$, corresponding to the linear operation of a JFET device. Since it is generally accepted that the effective voltage control of the depletion region is limited by the voltage that closes the channel Vp and the built-in potential ϕ, this problem could be overcome by using Vgd instead of Vds in (5), and by transforming both voltages in effective quantities $Vgseff$ and $Vgdeff$ always between Vp and ϕ.

This transformation can be done in different ways to ensure a continuous and differentiable transition. As Vp and ϕ magnitudes can be very close in some very thin channel devices, it was necessary to avoid the influence of a transition on the other. Thus, we decided to employ the following equation to transform Vgx into $Vgxeff$ as is plotted in Fig. 4:

$$Vgxaux = Vpo + \frac{1}{2\cdot\alpha x}\cdot\left\{\alpha x\cdot(Vgx-Vpx) + \ln\Big(2\cdot\cosh\big(\alpha x\cdot(Vgx-Vpx)\big)\Big)\right\} \tag{6a}$$

$$Vgxeff = \phi + \frac{1}{2\cdot\beta x}\cdot\left\{\beta x\cdot(Vgxaux-\phi) - \ln\Big(2\cdot\cosh\big(\beta x\cdot(Vgxaux-\phi)\big)\Big)\right\} \tag{6b}$$

with $x = s$ for Vgs and $x = d$ for Vgd.

Vpo represents the pinchoff voltage at $Vds = 0$ V, while Vpx accounts for the pinchoff modulation with Vds. Such modulation is quite evident for Vgs in normal operation, $Vds > 0$, and has been included in most models. This is not the case with Vgd, where the pinchoff modulation stands for the deviation of the border between the linear and saturated regions from a constant Vgd, typical in a MESFET device, and

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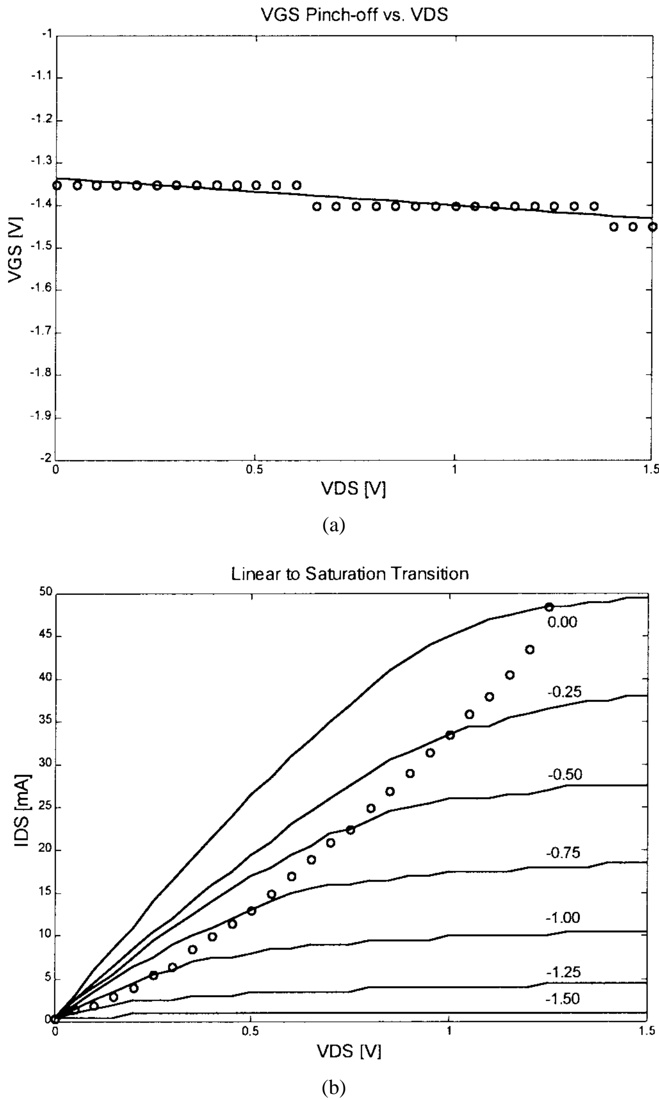

Fig. 3. $V_{\rm GS}$ and V_{GD} pinchoff transitions. (a) $V_{\rm GS}$ Pinchoff voltage modulation with $V_{\rm DS}$. (b) Border between the linear and the saturated regions.

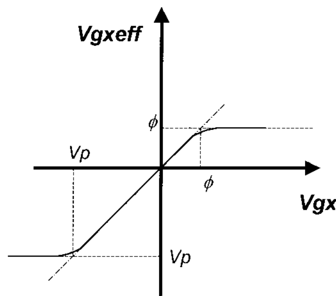

Fig. 4. Effective control voltage definition.

related to the velocity saturation and the two regions saturated channel description [24]. In inverse operation, $Vds < 0$, the roles of Vgs and Vgd are interchanged. The transition of Vgs through the pinchoff value thus defines the linear-to-saturation border

$$Vpx = Vpo + \gamma x \cdot (Vgs - Vgd). \tag{7}$$

This is a simple way of representing the pinchoff modulation. Other more complex relations could be employed if we were interested in improving the linear-to-saturation-border definition.

The parameters βs and βd are related to the built-in voltage transition and are not critical in the derivative reproduction. The contrary occurs with αs and αd since they define the continuous transition in the pinchoff value. As we mentioned in the previous section, the cutoff site and the linear-to-saturation border seem to significantly determine the device's derivatives. Here, we are defining both sites through the pinchoff voltage transition of Vgs (cutoff) and Vgd (linear to saturation) in normal operation.

The abruptness of this transition can be defined from the corresponding maximum in the second-order derivatives. It seems that there are two quite definite values for this maximum: one when the Vgx transition defines the cutoff region and the other when it represents the linear-to-saturation border, with a soft behavior when we move from one to another. Thus, we decided to employ the following equation to define αs and αd depending on the other control voltage:

$$\alpha x = \frac{1}{2} \cdot \Big\{ (\alpha x_c + \alpha x_{ls}) + (\alpha x_c - \alpha x_{ls}) \cdot \tanh\left[\mu \cdot (Vgy - Vpo)\right] \Big\}. \tag{8}$$

if $x = s, d$ then $y = d, s$.

αs_c and αd_c define the values at cutoff for the Vgs and Vgd transitions, while αs_{ls} and αd_{ls} define them in the linear-to-saturation transition. μ controls the softness of the maximum evolution between the two above-mentioned values.

With (7), (8), and (6) in respective order, we can accurately control the transitions defining the derivatives. Once we have obtained the effective control voltages $Vgseff$ and $Vgdeff$, we employ a modification of (5). We have detected that the exponent defined by 3/2 may result in a poor reproduction of the derivatives, as it was derived from an ideal uniform doping profile. Having the possibility of representing the third derivative nulls that may appear in these devices in the region of high transconductance [5], [6] and in the region of high output conductance was one of our goals due to their usefulness. For that reason, we propose an empirical exponent similar to the one used in [25], resulting in (9), shown at the bottom of this page.

In Fig. 5, we present the derivative prediction for the device characterized in the previous section. A very good agreement between both sets is evident. The important effects related to power dissipation and frequency dispersion in MESFET's could be taken into account with approaches such as [13] and [25]. Since we want to concentrate on the small-signal

$$Ids = Go \cdot \left\{ Vgseff - Vgdeff - \frac{2}{3} \cdot \left[\frac{(\phi - Vgdeff)^{E + Ke \cdot Vgdeff} - (\phi - Vgseff)^{E + Ke \cdot Vgseff}}{(\phi - Vpo)^{1/2}} \right] \right\} \tag{9}$$

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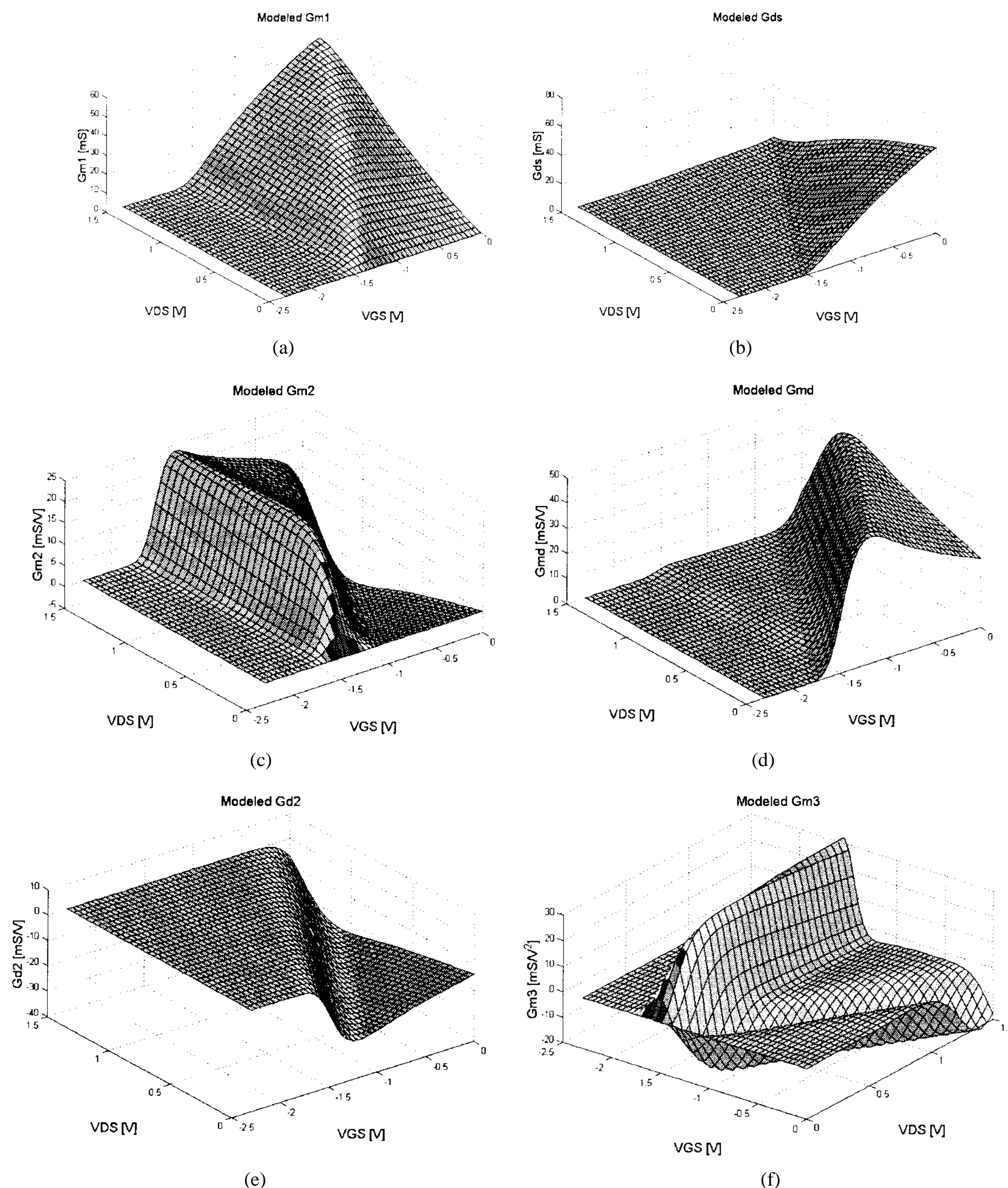

Fig. 5. Modeled $Ids(Vgs, Vds)$ derivatives. (a) $Gm1$. (b) $G_{\rm ds}$. (c) $Gm2$. (d) Gmd. (e) $Gd2$. (f) $Gm3$.

nonlinear distortion prediction, we will not deal with them in detail here.

IV. Resistive FET Mixer Conversion Loss and IMD Optimization by Selective Bias

To introduce the resistive FET mixer analysis from the derivative behavior, we should remember that this mixer, proposed in [26], is based on the gate–voltage control of the FET channel resistance (Rds) in cold operation ($V_{\rm DS} = 0$ V). As is explained in [27], an ideal mixer could be obtained from a time-varying linear system, in that case, without IMD products. This idea, followed in the resistive FET conversion, resulted in a mixer with excellent linearity properties when compared to its competitors.

In Fig. 6(a), we show $G_{\rm ds}$, Gmd, and $Gm2d$ across $V_{\rm GS}$ for a constant $V_{\rm DS} = 0$ V. Gmd and $Gm2d$ describe the variation of the nonlinear channel resistance (in fact of the output conductance $G_{\rm ds}$) as a function of the input control voltage, the role played by the LO drive in an FET resistive mixer [26]. In this way, they could be easily employed to approximately predict the optimum $V_{\rm GS}$ bias point for minimum conversion loss when the LO level is not too high. For the present device, this point is expected to be located around $V_{\rm GS} = -1.30$ V, the point where the coefficient $Gmd \equiv \partial G_{\rm ds}/\partial Vgs$ has a maximum. This point will be considered as the effective pinchoff voltage V_T for the mixer analysis.

In Fig. 6(b), the output conductance derivatives $Gd2$ and $Gd3$ are also plotted with $G_{\rm ds}$ in $V_{\rm DS} = 0$ V. $Gd2$ and $Gd3$ represent the residual nonlinearity of the FET channel resistance, the $G_{\rm ds}$ dependence on Vds mainly responsible for the device's IMD behavior in a resistive mixer (the RF signal is applied between the drain and source terminals). In

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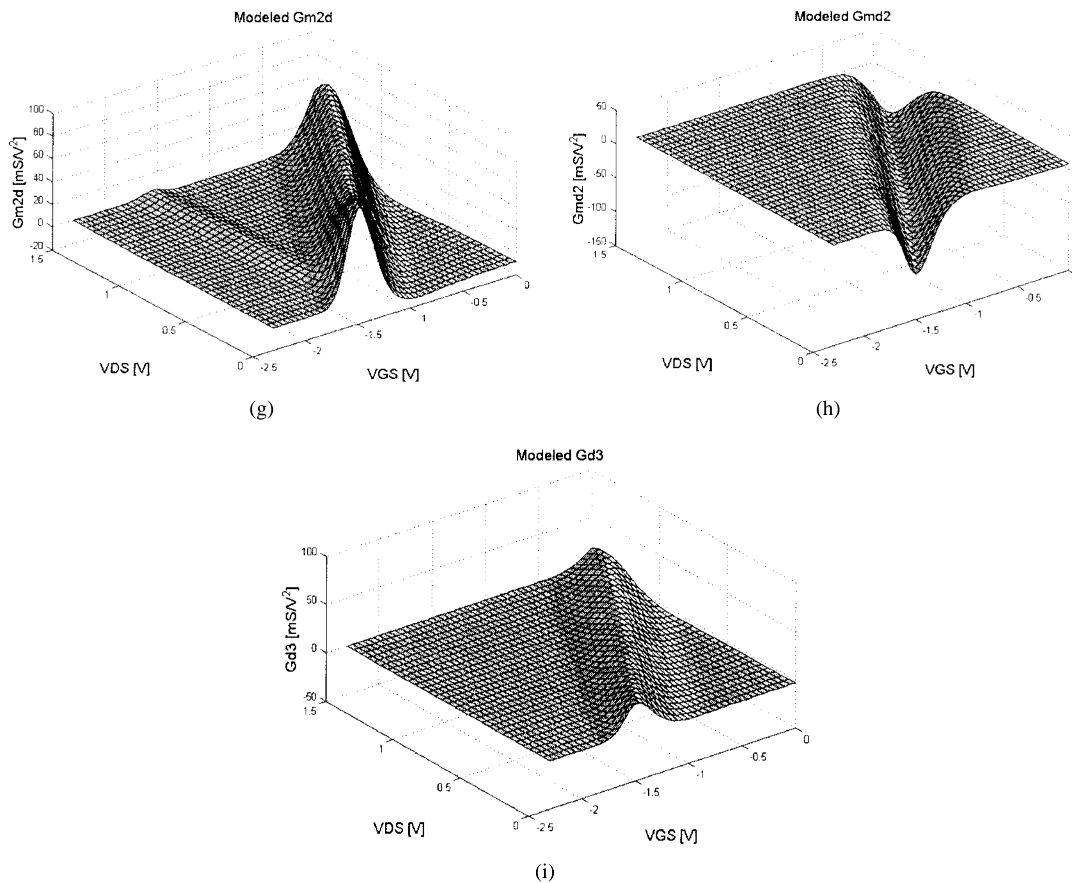

Fig. 5. *(Continued.)* Modeled $Ids(Vgs, Vds)$ derivatives. (g) $Gm2d$. (h) $Gmd2$. (i) $Gd3$.

an ideal time-varying linear mixer, these derivatives should be null along the LO trajectory.

Fig. 7(a) displays $G_{\rm ds}$, $Gd2$, and $Gd3$ evolution across $V_{\rm DS}$ for a constant $V_{\rm GS}$ of -0.9 V. A careful observation of these curves reveals a $Gd3$ null near $V_{\rm DS} = 0.25$ V, which could be a clear indication that the device can present its best in-band linearity performance not exactly under cold bias, but for a slightly positive $V_{\rm DS}$. In Fig. 7(b), the above-mentioned terms are also plotted versus $V_{\rm GS}$ for this interesting $V_{\rm DS}$ value, confirming a lower residual nonlinearity along the whole $V_{\rm GS}$ range when compared to the values in $V_{\rm DS} = 0$ V represented in Fig. 6(b). A conclusion that may be anticipated from the existence of these $Gd3$ nulls and from a lower $Gd3$ variation with $V_{\rm GS}$ is that, in a similar way as bias is used to improve conversion loss in a diode mixer, a small amount of $V_{\rm DS}$ bias could also be applied to optimize IMD performance of a MESFET switch or resistive mixer.

To study the practical usefulness of the above remarks, an illustrative resistive FET mixer was designed and simulated using a combination of strong nonlinear harmonic balance technique (for finding LO induced quiescent point excursion) and time-varying Volterra series (for mixer conversion loss and IMD analysis). The results can be suitably extended to the FET switch since it is no more than a resistive mixer where the equivalent LO, the control voltage, slowly switches between two very definite values. The circuit, which is a simple 50-Ω source and load impedance design, was then implemented and its performance evaluated for $f_{\rm LO} = 1.7$ GHz and $f_{\rm RF} = 2$ and 2.005 GHz, frequencies not too high in order to avoid important contributions from the reactive nonlinearities [28].

First, the conversion loss dependence on $V_{\rm GS}$ bias was studied, as is shown in Fig. 8. The comparison of these measurements and simulated results with the Gmd curve of Fig. 6(a) clearly proves the usefulness of our approach.

For an LO drive of 6 dBm, the intrinsic $Vgs(\omega_{OL})$ amplitude control voltage was found to be around 1.25 V. Assuming, as a first-order estimate, that the FET channel conductance waveform induced by the LO excitation is a rectified sinusoid, its equivalent dc voltage should be about $Vgs(\omega_{OL})/\pi$ or 0.4 V. Thus, the equivalent dynamic device's quiescent point would be above the bias (V_T) by this amount $(V_{\rm GS} = V_T + Vgs(\omega_{OL})/\pi = -0.9$ V). Looking at Fig. 7, it can be seen that, for this $V_{\rm GS}$ bias, the $Gd3$ null is located at $V_{\rm DS} = 0.25$ V, which could predict an in-band IMD sweet spot at this $V_{\rm DS}$ bias point.

Fig. 9(a) and (b) shows measured and simulated conversion loss and extrapolated output IP_3 for the implemented mixer when the auxiliary drain bias was varied from 0 to $+0.5$ V. An optimum IMD point is indeed found to be near the predicted sweet spot. In comparison to the previous design methods, which recommended a cold bias point ($V_{\rm DS} =$ 0 V), the addition of the auxiliary drain bias has allowed an improvement of 7 dB on IP_3 with only a slight degradation ($<$1 dB) in conversion loss. This proves the validity of the new MESFET resistive mixer and switch linearity optimization method proposed here.

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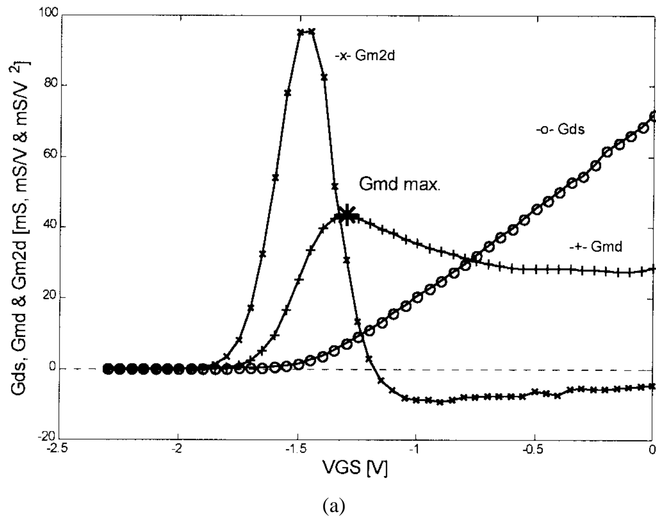
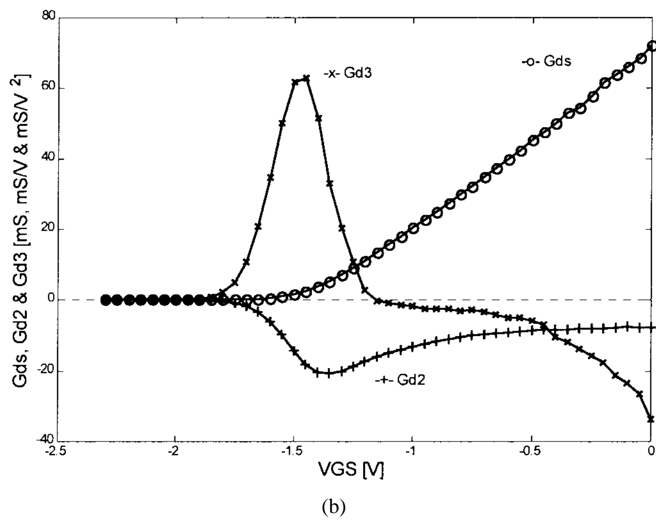
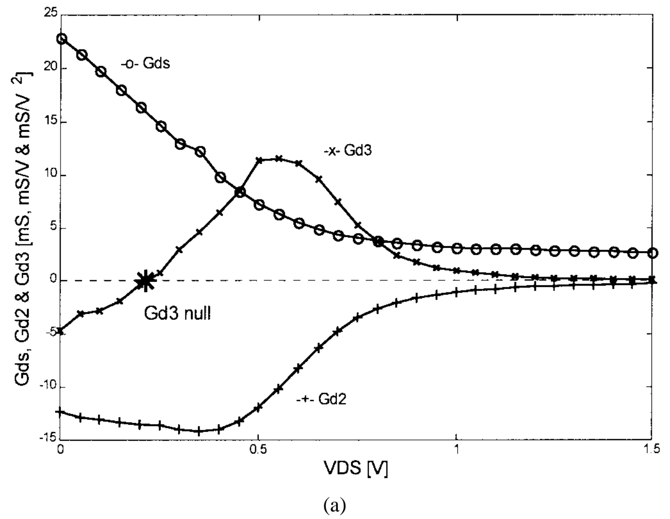


(a)

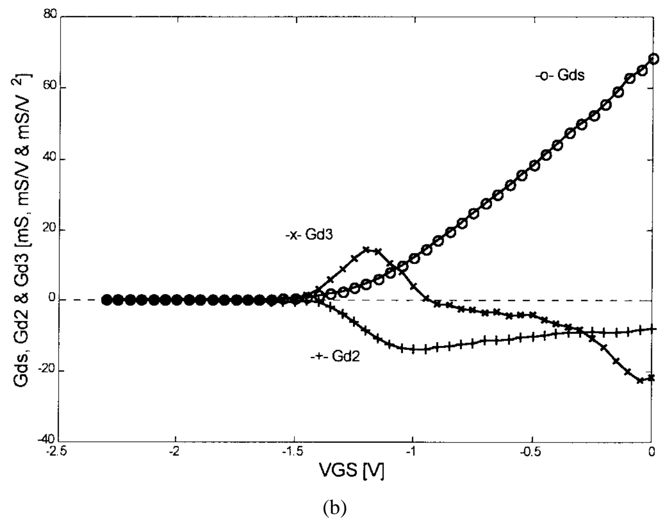


(b)

Fig. 6. Cold FET nonlinear characterization versus V_{GS} bias. (a) G_{ds} and its derivatives with Vgs. (b) Residual nonlinearity (G_{ds} and its derivatives with Vds).



(a)



(b)

Fig. 7. Output conductance description: (a) with V_{DS} bias ($V_{GS} = -0.9$ V) and (b) with V_{GS} bias ($V_{DS} = 0.25$ V).

The $Gd3$ null behavior [see Fig. 2(i)] would also give us the possibility of finding a V_{DS} value for optimum linearity with different LO power levels. For higher power levels, this sweet spot would be shifted to higher V_{DS} values. As has been previously reported [26], [27], while the LO excursion does not enter in gate junction conduction, the third-order intercept point would increase with LO level. A suitable higher V_{DS} bias may also add some improvement.

V. Load–Pull Conversion Loss and IMD Behavior

Recently, interesting experimental results have confirmed that by varying the IF load of a resistive mixer, both the conversion loss and IMD performance could be improved [15]. The time-varying Volterra-series analysis constitutes a direct and robust technique to investigate this behavior and compare the load improvements with the drain bias considerations of the previous section.

Load–pull simulations were made in our resistive mixer ($V_{GS} = -1.3$ V and $V_{DS} = 0$ V) with similar power levels. In Fig. 10(a), we represent the relative conversion loss, defined

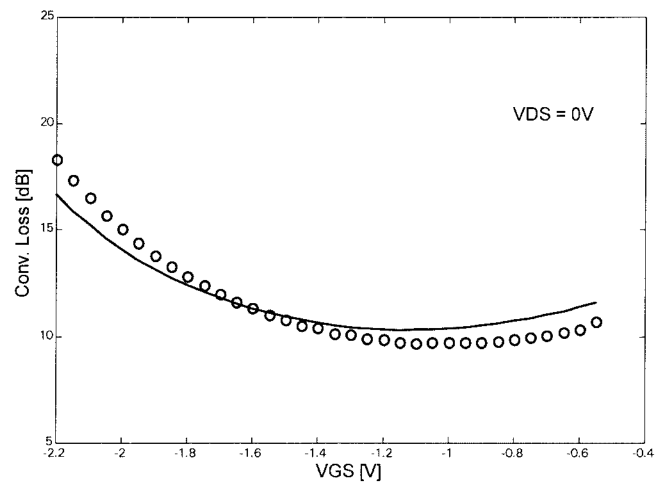


Fig. 8. Conversion loss [in decibels] versus V_{GS} at $V_{DS} = 0$ V. (o): Measured values. (−): Time-varying Volterra simulations.

with respect to its value in 50-Ω condition and, in Fig. 10(b), the relative third-order intercept point, equally defined It seems to be difficult to get a good tradeoff between an improvement in the conversion loss and IMD behavior. Here however, the

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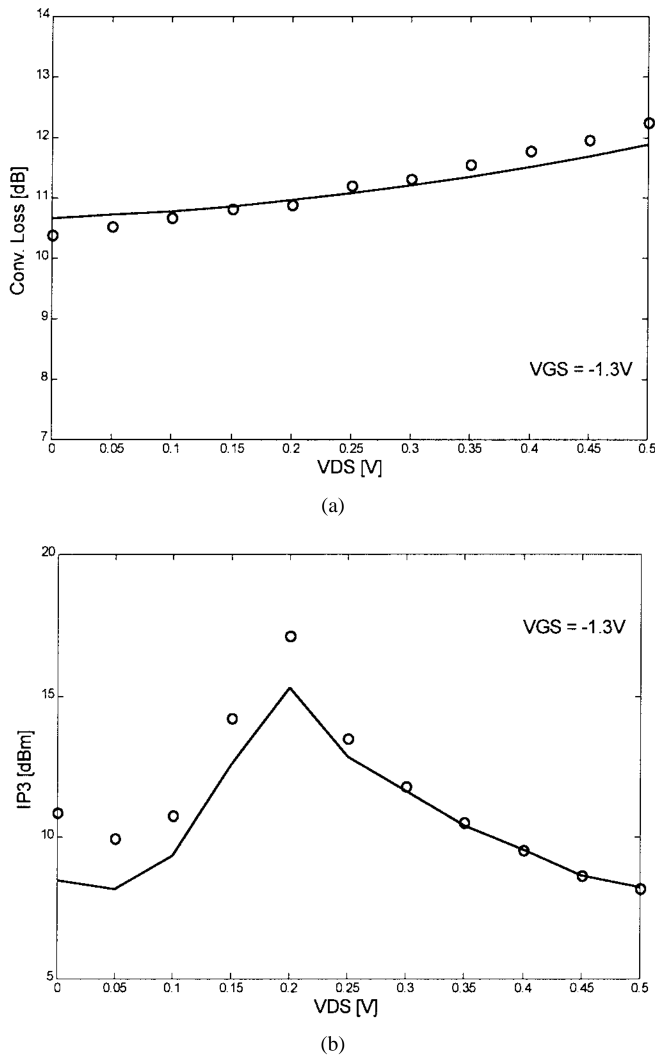

Fig. 9. (o): Measured and (−) simulated performance versus $V_{\rm DS}$ at $V_{\rm GS} = -1.3$ V and $P_{LO} = 6$ dBm. (a) Conversion Loss [in decibels]. (b) Third-order intercept point.

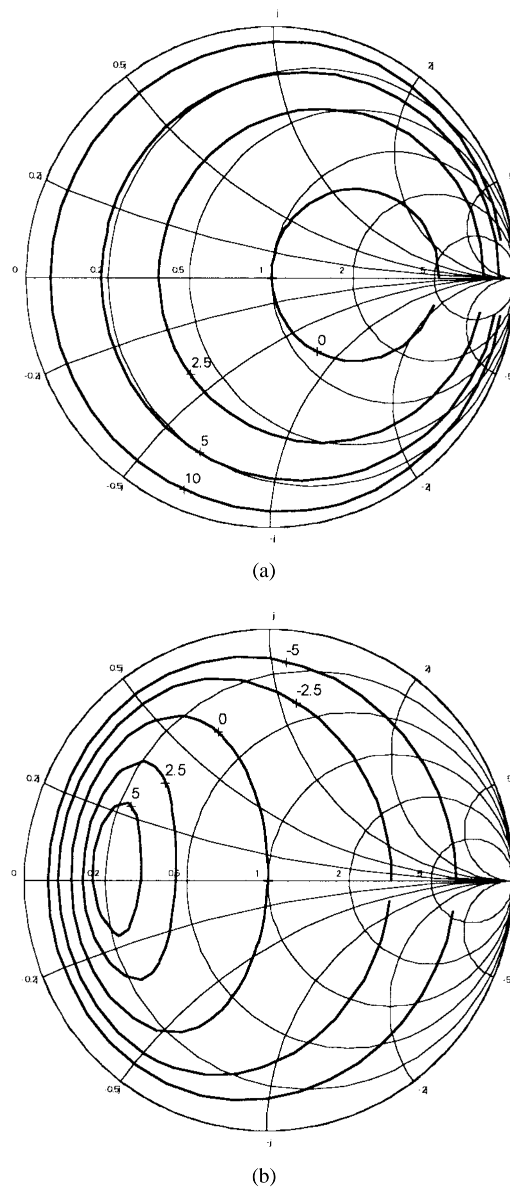

Fig. 10. Time-varying Volterra-series load–pull prediction. (a) Relative conversion loss [in decibels]. (b) Relative third-order intercept point. Relative values defined with respect to 50-Ω condition.

possible improvement is not better than the one obtained with a small drain bias.

VI. A Quadratic Mixer?

In Section I, we discussed the presence of sites with nulls in the third-order derivatives, one in the cutoff region and the other on the border delimiting the linear and saturated regions. If we were able to make the LO waveform move through a site of this nature, we could expect a highly linear performance from a mixer. However, we should also guarantee a first-order coefficient variation along the same LO trajectory in order to have useful conversion properties. Moving along the cutoff site does not seem to be interesting at first glance because of the latter consideration, but this is not the situation of the other site.

We could certainly think about a resistive or even an active mixer where the LO moves around the mentioned trajectory. We would need both Vgs and Vds to vary with the LO pumping signal with an appropriate amplitude and phase relation, something experimentally explored in [15] through an active load–pull system, and in [29], through a negative feedback arrangement. In those works, quite good third-order IMD improvements were obtained, but without a strong theoretical support. We certainly believe it could be related to the third-order derivative null in the linear to saturated region transition.

This topology is quite complex in normal operation $(Vds > 0)$ using a common source transistor, but it may become much simpler when we do not have that terminal connected to ground. In fact, applying the LO signal by source and guaranteeing a LO short circuit at gate and drain, we could manage to get the same LO variation in Vgs and Vds for a device with a border of approximately $Vgd = \text{constant}$. In general, FET transistors may have a border with $Vgd \neq \text{constant}$, and a convenient network should be designed for obtaining the proper LO excursion. The RF signal could be applied by gate or drain, although a better IMD behavior is expected for the resistive kind of

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operation. The frequency difference between the RF and LO signals can not be too low because of the above-mentioned LO short circuits.

The term "quadratic" for a mixer of this kind would be derived from the fact that in the mentioned site, the third-order derivatives are almost null, while the second-order ones have a peak. Although it is a highly nonlinear site, it is mainly of quadratic nature, which can be quite advantageous for an extremely low in-band IMD performance in a mixer. Finally, this "quadratic" site could also support a good frequency doubler application [30].

VII. Conclusions

In this paper, the experimentally extracted second- and third-order derivatives for the $Ids(Vgs, Vds)$ Taylor-series expansion in the linear region have been considered to be related to the location of optimum $V_{\rm GS}$ bias (for minimum conversion loss) and $V_{\rm DS}$ sweet spots (for low IMD) in a MESFET resistive mixer. The linearity improvements are better and simpler with this approach, than with the IF load–pull control. The third-order derivative null in the limit between the linear and saturated regions has been introduced as the possible cause of some interesting experimental results with simultaneous LO injection for gate and drain terminals. A global MESFET model has also been proposed in order to accurately predict the small-signal nonlinear distortion behavior in this kind of applications. The time-varying Volterra series has proven its accuracy for this nonlinear circuit analysis situation.

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