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Resistorless Memristor Emulator Using CFTA and Its Experimental Verification

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ABSTRACT This article presents a novel charge-controlled memristor emulator circuit. The proposed memristor emulator utilizes a single Current Follower Transconductance Amplifier (CFTA) as an active current mode analog building block and a grounded capacitor as a passive element. The circuit presented follows all the fingerprints of an ideal memristor. It operates in both incremental as well as decremental mode. The functional performance of the emulator circuit is verified at different operating frequencies and performs well up to *9 MHz*. The theoretical and non-ideal analyses are verified for the proposed emulator. Moreover, Monte Carlo sampling and non-volatility analysis are performed to investigate the robustness of the emulator circuit. The functionality of the proposed model has been verified through PSPICE simulation using TSMC *0.18* μm CMOS technology at the supply voltage of $\pm 1.2\ V$. The experimental confirmation of the presented circuit is also performed by building a breadboard micromodel using ICs CA3080 and AD844AN. Memristor based Chua's circuit model is included as one of its applications.

INDEX TERMS Current mode, memristor emulator, Chua's circuit, CMOS, Monte Carlo, pinched hysteresis loop.

I. INTRODUCTION

Memristor is a two terminal nonlinear resistor with memory postulated by Chua [1] in 1971 as the missing circuit element. The anticipation was established on the basis of symmetry and the missing relationship between charge (q) and flux (ϕ) linkage. Memristor becomes the fourth basic circuit element after resistor, inductor and capacitor. Chua and Kang [2] show some unique behavior of memristor elements different from previous fundamental circuit elements, as it displays some strange nonlinear dynamic behavior, including governing equations defining the memristor systems. In 2008, Stanley Williams and his team [3] fabricated the first nanoscale model of memristor using thin film of TiO_2 in HP Laboratory. There are some opposing views [4]–[6] on the claimed fundamental nature of the memristor. Abraham illustrated that the physically realizable memristor [4] is nonlinear composition of resistor with hysteresis and the presence of real memristor is hypothesis [5], [6]. This finding drew the attention of many researchers/scholars worldwide.

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Memristors are of two types (based on memristance relation) flux controlled and charge controlled, depending on the memristance relation with the flux and charge linkage respectively. Memristors are characterized by three basic fingerprint properties [7], as there should be a pinched hysteresis loop in the V-I plane when excited by periodic bipolar signal, the loop area is inversely proportional to the applied signal frequency, and it starts to act like a linear resistor as the applied frequency approaches to infinity. Another important property of a memristor is non-volatility, i.e., it can retain its previous value until the next input appears. This property of memristor gives the capability to act as nonlinear resistance with memory. All of these unique properties of memristive elements, along with their compatibility with CMOS technology, have led to the development of a simple and specific SPICE model to emulate the dynamic nature of the memristor. The emulator circuits are more convenient than real memristor-based systems because of the fact that it is simple to control and modify their properties as well as operating frequency for different potential applications. Hence simplicity in modeling makes it much easier for researchers to work on emulator models rather than the real ones. Recently memristive concept has

been further extended to memcapacitor and meminductors emulator circuits [8]–[10]. Memristor emulators and their circuits have been utilized for various applications in recent years, such as memristive diode bridge, filters, chaotic circuits, oscillators, neuromorphic systems, memory computing, analog and digital circuits [11]–[26].

The literature survey reveals various SPICE simulation models available for memristor emulators [27]–[31]. On further advancement, different memristor models are designed using current mode analog building blocks such as Multi-Output Operational Transconductance Amplifier (MO-OTA) and an analog multiplier [32], single Current Backward Transconductance Amplifier (CBTA) and an analog multiplier [33], Differential Difference Current Conveyor (DDCC) and an analog multiplier [34], Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) [35], Multi-output Operational Transconductance Amplifier [36], Current Conveyor Transconductance Amplifier (CCTA) [37], Second-Generation Current Conveyor (CCII) and Current Conveyor Transconductance Amplifier (CCTA) [38], Second-Generation Current Conveyor (CCII) and Operational Transconductance Amplifier (OTA) [40], and Voltage Difference Transconductance Amplifier (VDTA) [41]. Also, in [32]–[41], the memristor models are experimentally validated by current mode commercially available integrated circuits (ICs) such as Current Feedback Operational Amplifier (CFOA/AD844), analog multiplier (AD633) and Operational Transconductance Amplifier IC (OTA/CA3080). On the other hand, memristor models [29], [42]–[45] are implemented using commercially available ICs only, which require a large number of passive components like capacitors and resistors and having an operating frequency of few kHz. In [46], [47], grounded memristors are realized using MOSFETs that operate in decremental mode only. In literature, very few articles included real-world application like memristor emulator model along with its application as memristor diode bridge in RC filter [11], [12], memristor based passive RC filters [38]–[40], neuromorphic systems and burst firing synapse neural model [13]–[15], [41]. Memristor based amplitude modulation circuit [35], [39] and memristor based chaotic oscillators [12], [13], [29], [40]. This article also includes a memristor based chaos oscillator for a better understanding of the proposed design.

In this scientific literature, a new Z-copy Current Follower Transconductance Amplifier (ZC-CFTA) based grounded memristor emulator is proposed. The presented design consists of a single CFTA as an active block and only a grounded capacitor as a passive element which makes it suitable for integrated circuits implementation. The presented circuit operates well up to *9 MHz* in both incremental as well as decremental configurations. The organization of this report is: section II has a brief discussion about CFTA followed by the proposed memristor emulator circuit. This section also includes frequency analysis and non-ideal analysis. Section III contains hysteresis fingerprints, Monte Carlo and non-volatile tests using Cadence Virtuoso and section IV has physical implementation using commercial ICs. Its comparison with available models is discussed in section V. Section VI has proposed memristor based Chua's circuit as its application and the article has concluded in section VII.

II. CFTA AND PROPOSED MEMRISTOR EMULATOR

The current follower transconductance amplifier (CFTA) is a current mode active block. It is a combination of current follower (CF) and operational transconductance amplifier (OTA) at the output stage. The schematic representation of CFTA [48] is shown in Fig. 1 and its port relationship is governed by Eqn. 1. The current at terminal z follows the current in terminal f and voltage across z-terminal is transformed into current by transconductance parameter g_m at output port o. Auxiliary port $\pm z_c$ copies the current flowing in terminal z. In Fig. 2, the CMOS based implementation of the CFTA block is shown.

$$V_f = 0, \quad I_{Z,\pm Z_c} = \pm I_f, \; I_O = gmV_Z \tag{1}$$

where g_m is the transconductance of CFTA, which is controlled by V_b. The expression for transconductance (g_m) is given by:

$$g_m = \frac{k}{\sqrt{2}}(V_b - V_{ss} - 2V_{th}) \tag{2}$$

where k is the process parameter of M_{18-19} and can be expressed as:

$$k = \mu_n C_{OX} \frac{W}{L} \tag{3}$$

Here μ_n, W/L and C_{OX} are respectively the mobility of charge carrier, the aspect ratio and the oxide capacitance per unit area of MOS.

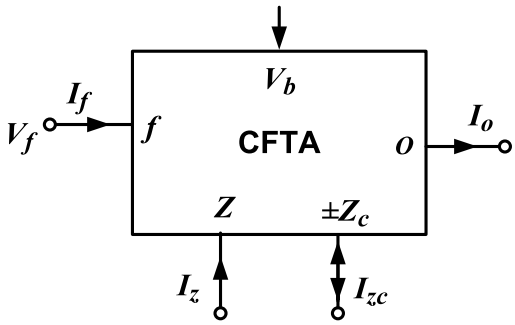

FIGURE 1. Schematic representation of CFTA block.

The proposed CMOS based new memristor emulator circuit as given in Fig. 3 consists of a single CFTA as an active current mode building block and a grounded capacitor as a passive element. Output terminal O is shorted with the port *f*. Input has been provided through the z-terminal. The direction of flow of charge modifies the memristance value, when its value increases, it is called incremental type and if it decreases, it is called decremental type memristor. Presented

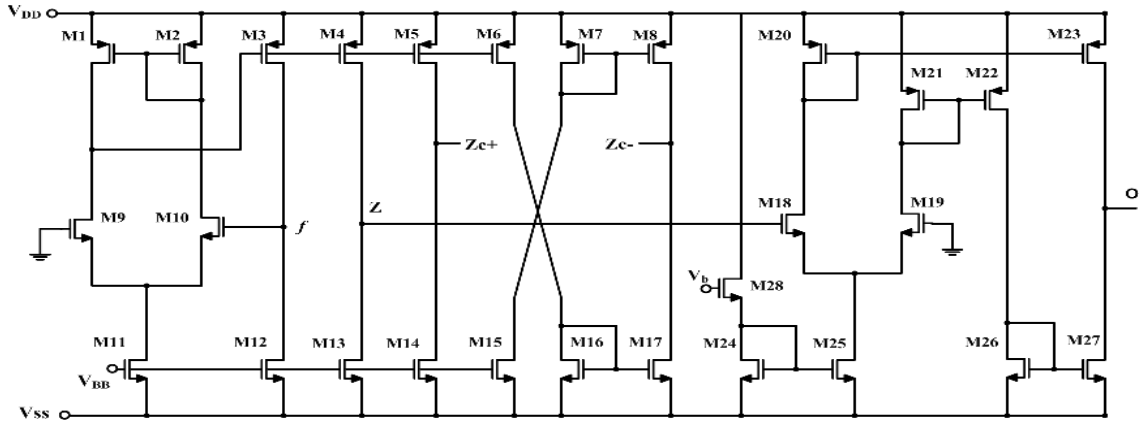

FIGURE 2. CMOS representation of CFTA block.

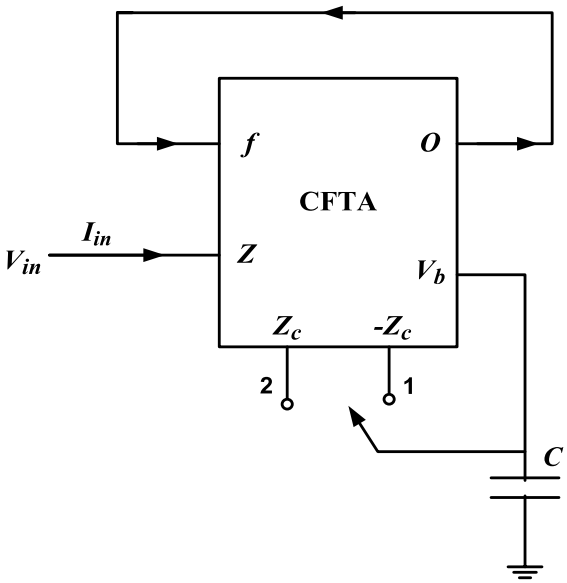

FIGURE 3. Proposed memristor emulator circuit.

emulator circuit act as incremental as well as decremental memristor depending upon the position of the capacitor, getting connected to either port *1* or *2* respectively. The capacitor will get connected to port *1* for the incremental configuration. The current across port *1* and *2* is given by:

$$I_{in} = I_Z = I_{Zc} = -I_{-Zc} \tag{4}$$

The voltage developed on the capacitor, when it is connected to port *1* or *2*, is given as:

$$V_{cap} = \pm\frac{1}{C}\int I_{in}dt \tag{5}$$

The potential across the capacitor is fed to the biasing voltage V_b of CFTA as:

$$V_{cap} = V_b = \pm\frac{1}{C}q_c(t) \tag{6}$$

where $\int I_{in}(t)$ is the charge on the capacitor and is denoted as $q_c(t)$. The output current of CFTA is given as:

$$I_o = g_m V_Z \tag{7}$$

As $I_o = I_f = I_Z$, using Eqn. 4 and substituting the value of bias voltage V_b from Eqn. 6 in Eqn. 2 of transconductance (g_m). Therefore, Eqn. 7 can be rewritten as:

$$I_{in} = \frac{k}{\sqrt{2}}\left(\pm\frac{q_c(t)}{C} - V_{ss} - 2V_{th}\right)V_{in} \tag{8}$$

So, the memductance of the proposed grounded type charge controlled memristor emulator circuit for incremental and decremental configuration is given as:

$$W\,(q_m) = \frac{I_{in}}{V_{in}} = \frac{k}{\sqrt{2}}\,(-V_{SS} - 2V_{th}) \pm \frac{k}{\sqrt{2}}\frac{q_c(t)}{C} \tag{9}$$

From Eqn. 8, it is observed that the memristance of the proposed emulator is the combination of initial memductance value and variable second parts. The overall memristance of the circuit depends on the charge flowing through it, so it is called a charge controlled memristor.

A. FREQUENCY RESPONSE ANALYSIS

To investigate frequency response of the proposed emulator design having time-invariant and time-variant part, a sinusoidal signal $V_{in}(t) = A_m sin(\omega t)$ having angular frequency ω and peak amplitude of A_m is applied. The average value of the input current $I_{in}(t)$ can be obtained by equating the time-variant part equal to zero and can be written as:

$$I_{in}(t) = \frac{k}{\sqrt{2}}\,(-V_{ss} - 2V_{th})\,V_{in}(t) \tag{10}$$

Thereafter, charge on the capacitor can be written as:

$$q_c(t) = \frac{k}{\sqrt{2}}\,(-V_{ss} - 2V_{th})\,\frac{V_m\cos(\omega t - \pi)}{\omega} \tag{11}$$

Substituting the value of charge ($q_c(t)$) of Eqn. 10 in Eqn. 8, the memductance can be written as:

$$W(q_c) = \frac{k}{\sqrt{2}}(-V_{SS} - 2V_{th}) \pm \frac{k^2(-V_{SS} - 2V_{th})A_m \cos(\omega t - \pi)}{2\omega C} \quad (12)$$

By observing the memductance given by Eqn. 12, the time-variant part is inversely proportional to the applied signal frequency. Therefore, as the frequency increases, the time-variant part tends to become negligible with respect to the time-invariant part, hence the memristor starts behaving like a linear time-invariant resistor at very high frequencies. The relation between time-variant and time-invariant part will be expressed by taking the ratio of their amplitudes, that is given by:

$$\alpha = \frac{kA_m}{2\sqrt{2}\pi fC} = \frac{1}{\tau f} = \frac{T}{\tau} \quad (13)$$

In Eqn. 13, α depends on both the applied frequency and value of the capacitor. Therefore, the time constant (τ) can be written as:

$$\tau = \frac{2\sqrt{2}\pi\alpha C}{kA_m} \quad (14)$$

From Eqn. 13 and Eqn. 14, it is illustrated that in order to hold the pinched hysteresis loop, the value of the time constant (τ) and frequency must be updated so that it starts to act like a linear resistor at very high frequencies.

B. NON-IDEAL ANALYSIS AND PARASITIC EFFECTS

For a more accurate assessment, the effect of non-idealities and parasitic present in the CFTA based design (*Fig. 3*) are to be considered. The occurrence of non-idealities is due to the presence of mismatch in the MOS transistors. The modified port relationship of CFTA along with its non-idealities is given as:

$$V_f = 0, \quad I_{Z,\pm Z_c} = \pm\alpha_i I_f, I_O = \gamma g m V_Z \quad (15)$$

where α_i is the current tracking error from port f to Z and Zc terminals. Similarly, γ is the trans-conductance inaccuracy factor from port Z to O terminal. Ideally, the tracking errors α_i and γ are unity. The parasitic impedances present at the port Z, Z_C and O are $R_Z//C_Z$, $R_{ZC}//C_{ZC}$ and $Ro//Co$ respectively. R_f is the parasitic impedance at port f, its value is very close to zero, but for the sake of simplicity, it is chosen as zero. The value of parasitic impedances R_Z, R_{ZC} and Ro are equal to infinity and the corresponding value of parasitic capacitances C_Z and Co are approximately equal to zero. Since C_{ZC} appears in parallel with the capacitor C, hence the total capacitance will add up. Fig. 4 shows the equivalent circuit. The overall performance of the circuit is affected by the parasitic capacitances, resistances and the non-idealities in the MOS transistors. By considering the tracking error due to non-idealities and parasitic, the memductance equation is given by:

$$W(q_m) = \frac{I_{in}}{V_{in}} = \frac{\gamma k}{\sqrt{2}}(-V_{SS} - 2V_{th}) \pm \frac{\alpha\gamma k}{\sqrt{2}}\frac{q_c(t)}{(C + C_{Zc})} \quad (16)$$

From Eqn. 16, it is seen that the memductance value may get deviated from the ideal one due to parasitic and non-idealities.

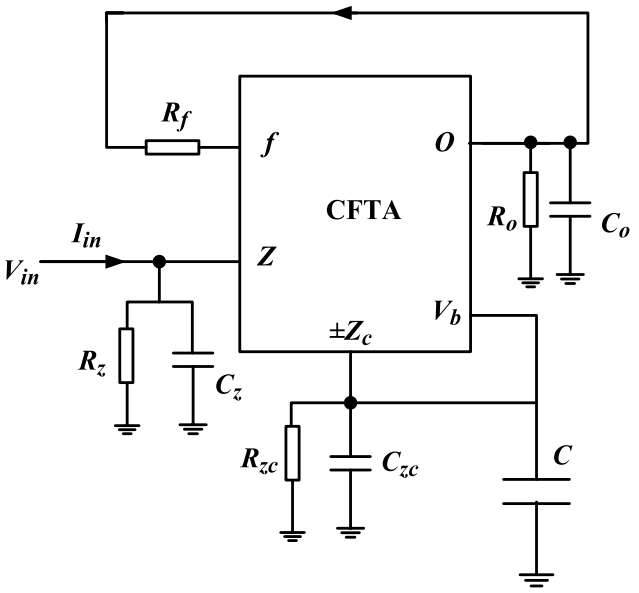

FIGURE 4. CFTA emulator circuit with port parasitic.

III. SIMULATION RESULTS

In this section, the theoretical explanation of proposed grounded memristor emulator circuit as discussed in the previous section has been justified through simulation as well as experimental verification. The computer simulation of the proposed memristor emulator is performed using Cadence Virtuoso Analog Design Environment tool, where the CFTA block is designed using *TSMC 0.18 μm* process parameters. The aspect ratio for NMOS and PMOS is mentioned in Table 1. The biasing voltage (V_{BB}) is taken as $-0.4\ V$. The supply voltage ($V_{DD} = -V_{SS}$) needs $1.2\ V$. All the MOS transistors are working in saturation mode and the bulk

TABLE 1. MOS transistors dimension.

NMOS Transistors	W (μm) / L (μm)
$M_9 - M_{10}$	2/0.35
$M_{11} - M_{19}$	4/0.35
$M_{24} - M_{28}$	14/0.35
PMOS Transistors	**W (μm) / L (μm)**
$M_1 - M_8$	3/0.35
$M_{20} - M_{23}$	17/0.35

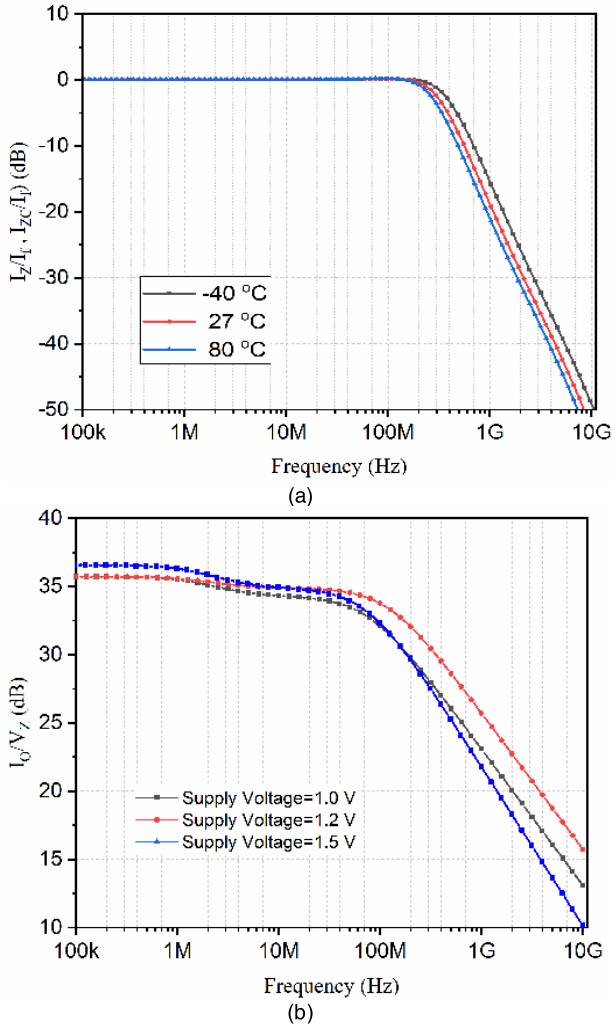

FIGURE 5. AC response of presented CFTA (a) current gain at different temperatures (b) Transconductance gain at different supply voltages.

of NMOS and PMOS transistors are connected to V_{SS} and V_{DD} respectively. The *AC* response at different temperature and power supply variations of CFTA block is performed. Fig. 5 (a) shows that the current gain at different temperatures and Fig. 5 (b) shows the transconductance gain at different supply voltages. The performance at *1.2 V* of power supply is optimized. Fig. 6 (a) shows the pinch hysteresis curve in the current- voltage plane for the sinusoidal input voltage of *500 mV* and the value of capacitor is *22 pF* for frequency up to *1 MHz*. Similarly, in Fig. 6 (b) and (c), the value of the capacitor is taken as *8 pF* and *3 pF* respectively. From Fig. 6, it is observed that area under pinched hysteresis loop keeps on decreasing as frequency increases and hence validates the fingerprint property of the memristor.

The shape and area of the bow-tie curve in *V-I* plane depends on the applied frequency of the input signal and the value of the capacitor. The capacitor holds the inverse relation with α as mentioned in Eqn. 13, which means that the hysteresis loop area decreases as the capacitor value increases. This effect is justified in Fig. 7 at a frequency of *900 kHz*.

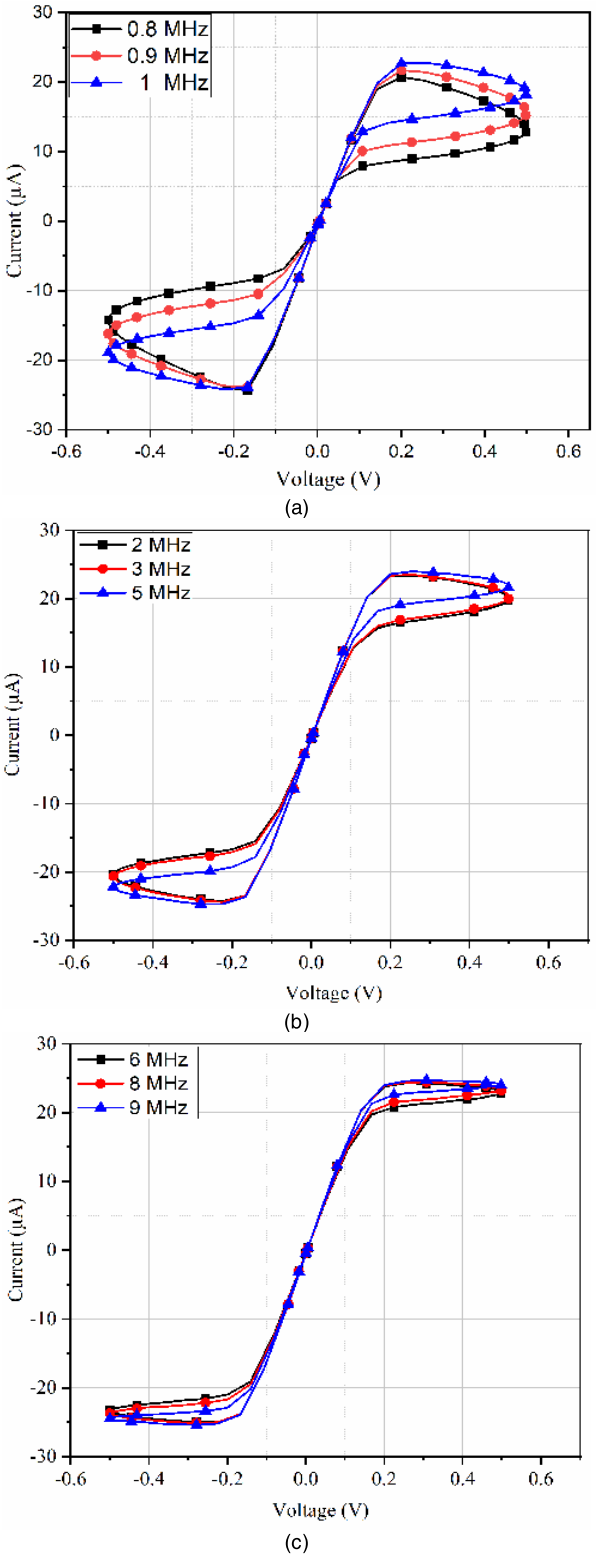

FIGURE 6. Voltage-current plane pinched hysteresis loop for various frequency (a) 0.8, 0.9 and 1 MHz at 22pF capacitor value (b) 2, 4 and 5 MHz with capacitor value of 8pF (c) 6, 8 and 9 MHZ with capacitor value of 3pF.

Non-volatility is another important characteristic of an ideal memristor. It means that it can remember its past value and is hence capable of acting as a memory besides

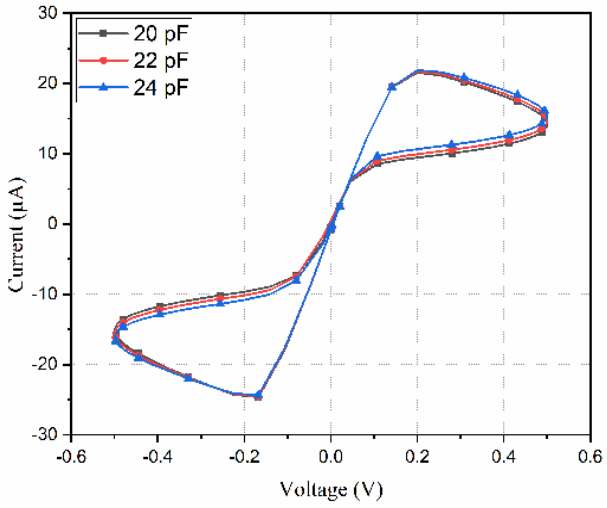

FIGURE 7. Pinched hysteresis loop in the current-voltage plane for different values of capacitor.

depicting the frequency dependent pinched hysteresis loop. It has ability to retain its last value until the next input signal arrives as signified by its name memory with resistor. This characteristic is verified by providing a train of pulses as an input signal. In order to test the non-volatility of the proposed emulator model, a periodic pulse signal of amplitude *500 mV* having time period of *1 ms* and duty cycle of *20%* is applied as input. The value of the capacitor is taken as *22 pF*. Fig. 8 shows the memductance variation in incremental and decremental topologies. It can be said that the memductance value remained unaltered in the absence of input pulse and changes as the next pulse arrived in both topologies.

In order to examine the performance and robustness of the proposed emulator circuit against the transistor mismatch and statistical process variation, Monte Carlo Sampling (MCS) simulation was performed for incremental configuration at an input frequency of *1 MHz*. MCS simulation was performed for *120* runs by considering Gaussian distribution method for transistor mismatch and process variation. Fig. 9 shows the Monte Carlo performance analysis with a slight variation in the pinched hysteresis loop and it is found that it operates within the acceptable corner limits.

IV. EXPERIMENTAL VERIFICATION

The experimental verification of the proposed grounded memristor emulator circuit using current mode approach is performed using breadboard implementation. Since the monolithic IC of CFTA is not available commercially, the practical realization of CFTA has been done using discrete ICs AD844 and CA3080. The proposed model requires two CA3080 and one AD844 ICs with a capacitor as the passive element. The prototype circuit as shown in Fig. 10 is the IC-based model for incremental configuration of the proposed memristor emulator circuit. In order to check the workability of the proposed model (i.e., frequency dependent pinched hysteresis loop) a sinusoidal input voltage of *1 V* is

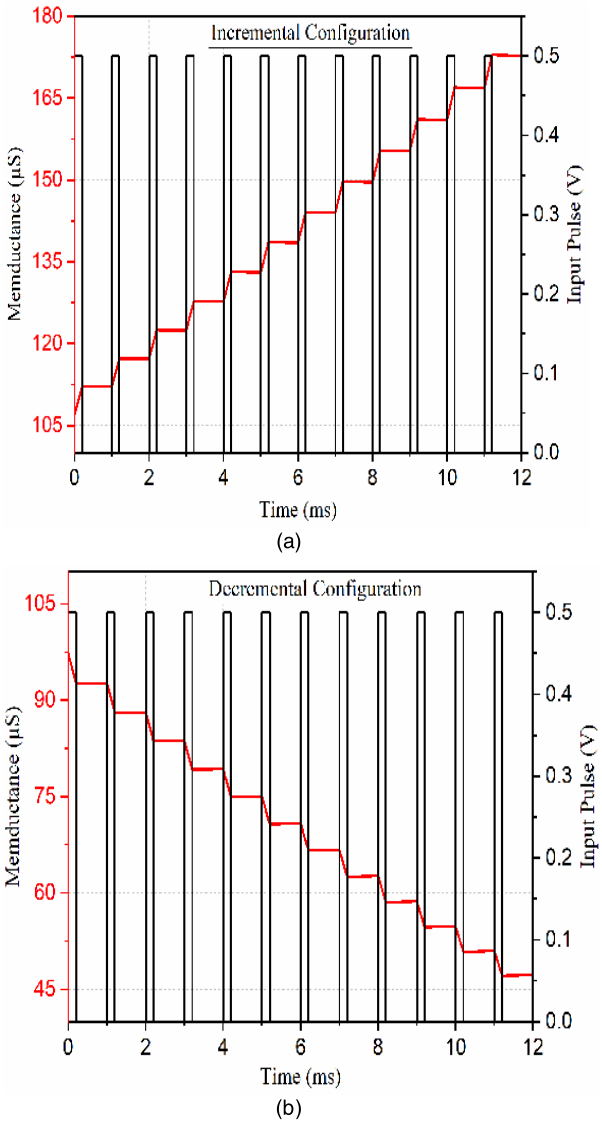

FIGURE 8. Non-volatile nature of memristor (a) Incremental Mode (b) Decremental Mode.

fed through the digital storage oscilloscope (DSO) itself and the DC power supply of $\pm 10\ V$ is applied across the circuit.

The value of the capacitor (C) varies according to the applied frequency. The resistor (R) of *10* Ω is used as a current shunt for the available voltage probe of DSO to obtain the corresponding input current.

The pinched hysteresis loop is captured through Dual Channel Keysight DSOX2022A series. Fig. 11 shows the complete setup of the experiment. Fig. 12 shows frequency dependent pinched hysteresis loop is obtained for an applied frequency of *960 kHz*. The value of capacitor (C) is taken as *30 pF* (in parallel combination of three *10 pF* capacitors). Only a capacitor used as a passive element in this implementation is advantageous over the other models proposed in [32]–[41]. It can be noted that the deformation and asymmetricity observed in the hysteresis loop are due to the

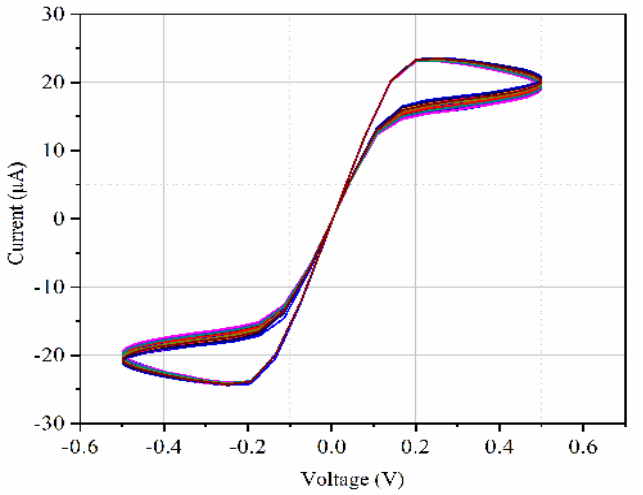

FIGURE 9. Monte Carlo analysis of proposed memristor model for 120 runs at 1 MHz.

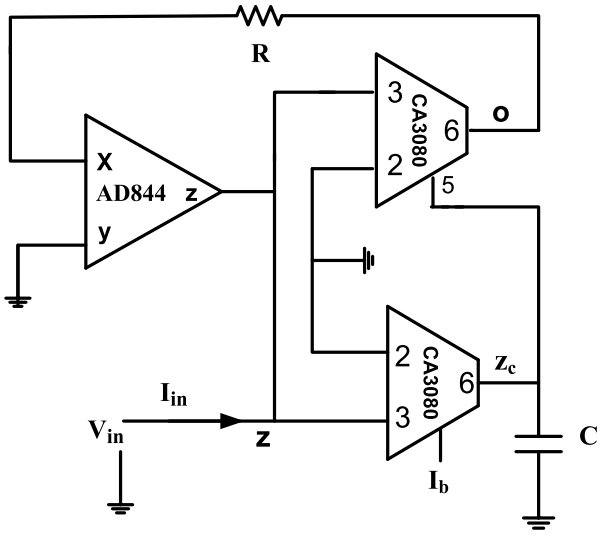

FIGURE 10. IC based proposed emulator model.

tracking error, frequency limitation of ICs and interconnects. On further increasing the frequency (more than *1 MHz*), the loop becomes narrower and starts to look more like a linear resistance, as shown in Fig. 13. At higher frequency the linear nature of the memristor is more dominant and thus justifies the theoretical and simulation analysis.

V. COMPARISON WITH EXISTING WORK

The presented work includes both MOS based design and its experimental verification using off-the-shelf ICs available in the market. The performance comparison in terms of active/passive components, the technology used, number of MOS required, power supply and the maximum operating frequency of the proposed MOS based memristor emulator with the other existing emulator models are illustrated in Table 2. The maximum attained frequency in [32], [33]

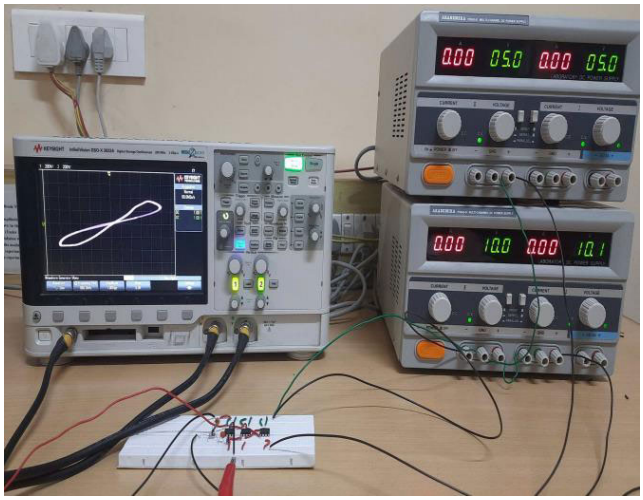

FIGURE 11. Pinched hysteresis loop of proposed memristor emulator model with experimental setup.

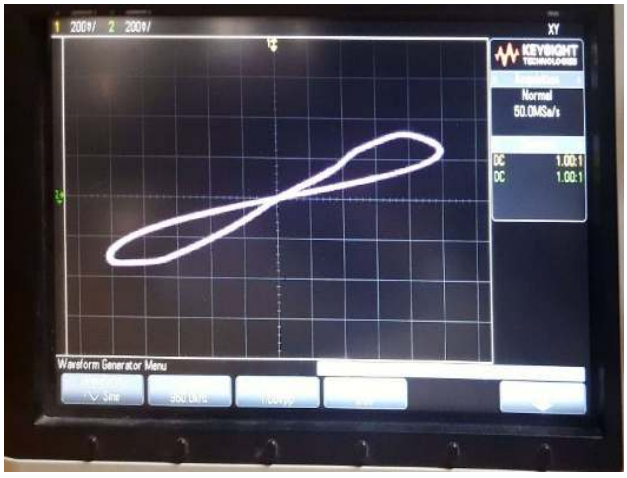

FIGURE 12. Pinched hysteresis loop in I-V plane at 960 kHz.

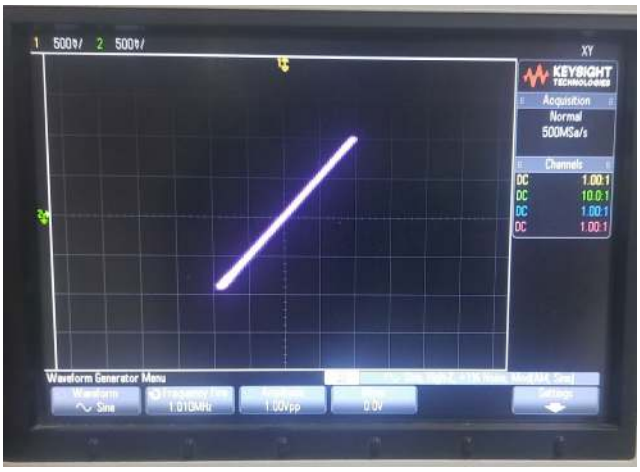

FIGURE 13. Linear nature of proposed model at the frequency of 1 MHz.

are in *kHz* and for [34]–[39] are up to the *8 MHz* range. The present model operates well up to *9 MHz*, except [40], [41], which has the operating frequency of *25.3 MHz* and *50 MHz,*

TABLE 2. Comparison of proposed memristor with existing active blocks.

Reference	No. of active components	No. of passive components	Incremental/ Decremental	Sim./ Exp.	Techno -logy used	No. of MOS	Power supply	Max. operating frequency
[32]	1 MO-OTA 1 MUL	R-2, C-1	Both	Both	CMOS	38#	±1.2V	Few kHz
[33]	1 CBTA 1 MUL.	R-2, C-1	Both	Sim	CMOS	23#	±0.9 V	500 kHz
[34]	1 DDCC 1 MUL	R-1, C-1	Both	Sim.	CMOS	50	±1.5 V	1 MHz
[35]	1 DVCCTA	R-3, C-1	Both	Both	CMOS	29	±1.5 V	1 MHz
[36]	1 MO-OTA	C-1	Decremental	Sim	CMOS	17	±0.9 V	1 MHz
[37]	1 CCTA	R-3, C-1	Both	Both	CMOS	30	±1.5 V	1 MHz
[38]	1 CCII 1 CCTA	R-3, C-1	Both	Both	CMOS	38	±1.5 V	5 MHz
[39]	2 OTA	C-1	Both	Both	CMOS	34	±1.2 V	8 MHz
[40]	1 CCII 1 OTA	R-1, C-1	Both	Both	CMOS	24	±1.2 V	25.3 MHz
[41]	1 VDTA	R-1, C-1	Both	Both	CMOS	16	±0.9 V	50 MHz
Proposed CMOS Design	**1 CFTA**	**C-1**	**Both**	**Sim**	**CMOS**	**28**	**±1.2 V**	**9 MHz**
IC based Design	**1 AD844AN 2 CA3080**	**R*-1, C-1**	**Both**	**Exp.**	**BJT**	**----**	**±10 V**	**995 kHz**

Number of CMOS used for multiplier is not mentioned.* Resistance used for taking voltage across it.

respectively. Moreover, only the proposed model and [39] are resistorless, whereas all other models include resistance as its passive component. The total number of components (active and passive) used for the proposed memristor emulator circuit is only two, which is minimum with respect to other models [32]–[41].

VI. CHUA'S CIRCUIT IMPLEMENTATION

Finally, the Chua's circuit is implemented as a memristor based application to validate the utility of the proposed design. The Chua's circuits are simple oscillators, which shows chaotic behavior. It consists of a capacitor, two inductors as linear energy storing elements and a memristor (as nonlinear Chua's diode). It is dual canonical Chua's circuit [19] with memristor. The governing equation for the Chua's circuit using charge controlled memristor is given as:

$$\begin{aligned} L_1\frac{di_1}{dt} &= V_c - M(q)i_1 \\ L_2\frac{di_2}{dt} &= Ri_2 - V_c \\ C\frac{dV_C}{dt} &= i_2 - i_1 \\ \frac{dq}{dt} &= i_1 \end{aligned} \tag{17}$$

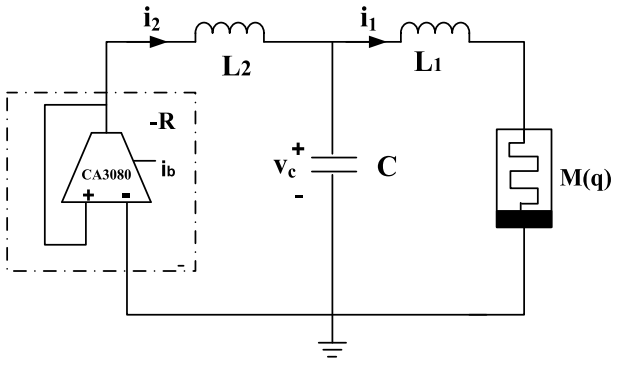

FIGURE 14. Chua's circuit implementation using memristor.

For the given state model, the equilibrium point and its stability analysis are performed by inspecting the dissipative behavior of the system. The divergence of the vector field is given as:

$$div(\Delta) = -aM(q) + b \tag{18}$$

Here $a = 1/L_1$, $b = R/L_2, c = 1/L_2$ *and* $d = 1/C$ respectively. In order to obtain the Chaotic nature of the given model, the divergence should be less than zero and

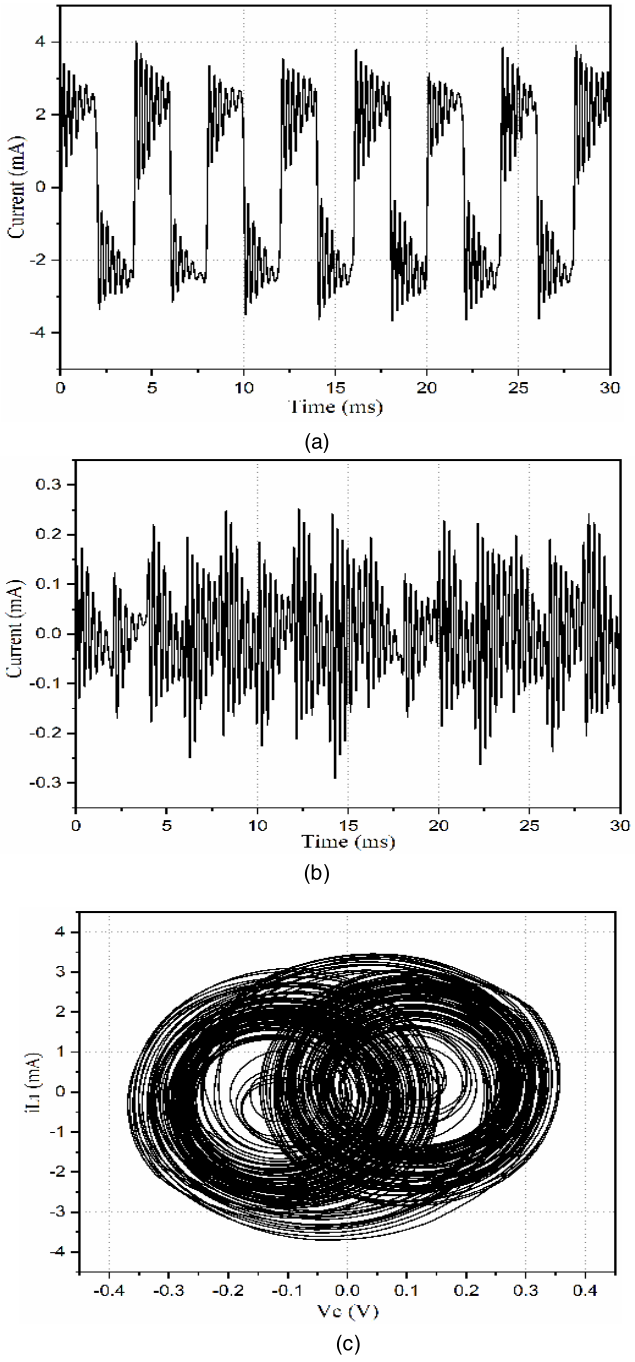

FIGURE 15. Simulated chaotic output (a) current across L_1 (b) current across L_2 (c) current i_{L1} verses capacitor voltage (V_c).

this is valid for $M(q) > b/a$. From Eqn. 17, the equilibrium point is given by $E_0 = (0, 0, 0, \beta)$ for the piecewise-linear memristor [19].

The Jacobian matrix J at equilibrium is given by,

$$J = \begin{pmatrix} -aM(q) & 0 & a & 0 \\ 0 & b & -c & 0 \\ -d & d & 0 & 0 \\ 1 & 0 & 0 & 0 \end{pmatrix} \tag{19}$$

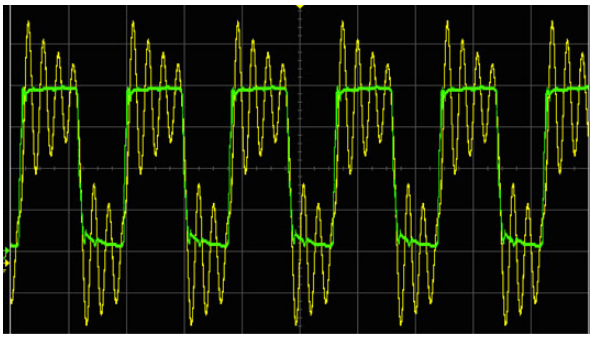

FIGURE 16. Experimental result of Chua's circuit implemented using memristor (yellow trace – current across L_1, green trace- voltage across capacitor (C)).

Thus at the equilibrium point E_0, the corresponding characteristic equation $|J - \lambda I|$ will be expressed as:

$$\lambda^4 + (aM(q) - b)\lambda^3 + (cd + ad - baM(q))\lambda^2 + (cdM(q) - dbc)\lambda = 0 \tag{20}$$

Thus, for M(q) < b/a the system becomes unstable and it is characterized by unstable saddle-focus except for the zero eigenvalues. The value of the capacitor (C), inductors L_1 and L_2 are taken as *3nF, 4.4 mH* and *50 mH*. The negative resistance is designed using IC 3080, which is commercially available and the value of biasing current i_b is taken as *100 μA*. Fig. 14 shows Chua's circuit and Fig. 15, shows the simulated outputs for current through the inductors L_1 and L_2. The Chua's circuit has been also assembled on breadboard and the experimental output has been originated, which is shown in Fig. 16. The chaotic output may appear periodic but they are strictly unpredictable. This property is useful for various applications such as secure communication [49], noise generator test circuits [50] and cellular neural networks [51].

VII. CONCLUSION

In this article, a charge-controlled grounded memristor emulator is presented. It requires a single CFTA as an active block and a grounded capacitor as a passive element, which makes the whole design simple and attractive for integrated circuits. The theoretical analysis is successfully defended using simulations as well as experimental tests. The proposed memristor emulator operates in both incremental and decremental configurations. The non-ideal and parasitic are analyzed for the proposed model. Moreover, non-volatility tests and Monte Carlo sampling analyses are also included. A breadboard prototype is made using off-the-shelf current mode commercially available ICs and grounded capacitor. In addition, the Chua's system model is included as one of the potential applications for the proposed memristor emulator and the simplicity in the proposed model will also be useful for implementing other applications.

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REFERENCES

[1] L. Chua, "Memristor-the missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, Sep. 1971.
[2] L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proc. IEEE*, vol. 64, no. 2, pp. 209–223, Feb. 1976.
[3] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008.
[4] I. Abraham, "The case for rejecting the memristor as a fundamental circuit element," *Sci. Rep.*, vol. 8, no. 1, Dec. 2018, Art. no. 10972.
[5] S. Vongehr and X. Meng, "The missing memristor has not been found," *Sci. Rep.*, vol. 5, no. 1, Dec. 2015, Art. no. 11657.
[6] K. M. Sundqvist, D. K. Ferry, and L. B. Kish, "Memristor equations: Incomplete physics and undefined passivity/activity," *Fluctuation Noise Lett.*, vol. 16, no. 04, Dec. 2017, Art. no. 1771001.
[7] S. P. Adhikari, M. P. Sah, H. Kim, and L. O. Chua, "Three fingerprints of memristor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 11, pp. 3008–3021, Nov. 2013.
[8] M. Di Ventra, Y. V. Pershin, and L. O. Chua, "Circuit elements with memory: Memristors, memcapacitors, and meminductors," *Proc. IEEE*, vol. 97, no. 10, pp. 1717–1724, Oct. 2009.
[9] Z. Yin, H. Tian, G. Chen, and L. O. Chua, "What are memristor, memcapacitor, and meminductor?" *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 4, pp. 402–406, Apr. 2015.
[10] D. Yu, X. Zhao, T. Sun, H. H. C. Iu, and T. Fernando, "A simple floating mutator for emulating memristor, memcapacitor, and meminductor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 7, pp. 1334–1338, Jul. 2020.
[11] B. Bao, J. Yu, F. Hu, and Z. Liu, "Generalized memristor consisting of diode bridge with first order parallel RC filter," *Int. J. Bifurcation Chaos*, vol. 24, no. 11, Nov. 2014, Art. no. 1450143.
[12] B. Bao, P. Wu, H. Bao, M. Chen, and Q. Xu, "Chaotic bursting in memristive diode bridge-coupled Sallen-Key lowpass filter," *Electron. Lett.*, vol. 53, no. 16, pp. 1104–1105, Aug. 2017.
[13] M. Chen, M. Sun, H. Bao, Y. Hu, and B. Bao, "Flux–charge analysis of Two-Memristor-Based Chua's circuit: Dimensionality decreasing model for detecting extreme multistability," *IEEE Trans. Ind. Electron.*, vol. 67, no. 3, pp. 2197–2206, Mar. 2020.
[14] C. Chaen, H. Bao, M. Chen, Q. Xu, and B. Bao, "Non-ideal memristor synapse-coupled bi-neuron Hopfield neural network: Numerical simulations and breadboard experiments," *AEU-Int. J. Electron. Commun.*, vol. 111, pp. 1–6, Nov. 2019, Art. no. 152894.
[15] H. Bao, A. Hu, W. Liu, and B. Bao, "Hidden bursting firings and bifurcation mechanisms in memristive neuron model with threshold electromagnetic induction," *IEEE Trans. Neural Netw. Learn. Syst.*, vol. 31, no. 2, pp. 502–511, Feb. 2020.
[16] H. Bao, M. Chen, H. Wu, and B. Bao, "Memristor initial-boosted coexisting plane bifurcations and its extreme multi-stability reconstitution in two-memristor-based dynamical system," *Sci. China Technological Sci.*, vol. 63, no. 4, pp. 603–613, Nov. 2019.
[17] S. C. Yener and H. H. Kuntman, "Fully CMOS memristor based chaotic circuit," *Radioengineering*, vol. 23, no. 4, pp. 1140–1149, 2014.
[18] B. Muthuswamy, "Implementing memristor based chaotic circuits," *Int. J. Bifurcation Chaos*, vol. 20, no. 5, pp. 1335–1350, May 2010.
[19] M. Itoh and L. O. Chua, "Memristor oscillators," *Int. J. Bifurcation Chaos*, vol. 18, no. 11, pp. 3183–3206, Nov. 2008.
[20] D. Yu, H. H.-C. Iu, A. L. Fitch, and Y. Liang, "A floating memristor emulator based relaxation oscillator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2888–2896, Oct. 2014.
[21] M. Hu, Y. Chen, J. J. Yang, Y. Wang, and H. H. Li, "A compact memristor-based dynamic synapse for spiking neural networks," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 36, no. 8, pp. 1353–1366, Aug. 2017.
[22] H. Kim, M. P. Sah, C. Yang, T. Roska, and L. O. Chua, "Neural synaptic weighting with a pulse based memristor circuit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 148–158, Jan. 2012.
[23] Y. V. Pershin and M. Di Ventra, "Practical approach to programmable analog circuits with memristors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1857–1864, Aug. 2010.
[24] Y. V. Pershin, E. Sazonov, and M. D. Ventra, "Analog-to-digital and digital-to-analog conversion with memristive devices," *Electron. Letters.*, vol. 48, no. 2, pp. 73–74, Jan. 2012.
[25] M. Escudero, I. Vourkas, A. Rubio, and F. Moll, "Memristive logic in crossbar memory arrays: Variability-aware design for higher reliability," *IEEE Trans. Nanotechnol.*, vol. 18, pp. 635–646, Jan. 2019.
[26] W. Bae and K. J. Yoon, "Comprehensive read margin and BER analysis of one selector-one memristor crossbar array considering thermal noise of memristor with noise-aware device model," *IEEE Trans. Nanotechnol.*, vol. 19, pp. 553–564, 2020.
[27] H. Abdalla and M. D. Pickett, "SPICE modeling of memristors," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Rio, Brazil, May 2011, pp. 1832–1835.
[28] Á. Rak and G. Cserey, "Macromodeling of the memristor in SPICE," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 29, no. 4, pp. 632–636, Apr. 2010.
[29] H. Kim, M. P. Sah, C. Yang, S. Cho, and L. O. Chua, "Emristor emulator for memristor circuit applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 10, pp. 2422–2431, Apr. 2012.
[30] C. Yakopcic, T. M. Taha, G. Subramanyam, and R. E. Pino, "Generalized memristive device SPICE model and its application in circuit design," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 32, no. 8, pp. 1201–1214, Aug. 2013.
[31] G. A. Patterson, J. Sune, and E. Miranda, "Voltage-driven hysteresis model for resistive switching: SPICE modeling and circuit applications," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 36, no. 12, pp. 2044–2051, Dec. 2017.
[32] Y. Babacan, A. Yesil, and F. Kacar, "Memristor emulator with tunable characteristic and its experimental results," *AEU-Int. J. Electron. Commun.*, vol. 81, pp. 99–104, Nov. 2017.
[33] U. E. Ayten, S. Minaei, and M. Saäba, "Memristor emulator circuits using single CBTA," *AEU-Int. J. Electron. Commun.*, vol. 82, pp. 109–118, Dec. 2017.
[34] A. Yeäil, Y. Babacan, and F. Kaçar, "A new DDCC based memristor emulator circuit and its applications," *Microelectron. J.*, vol. 45, no. 3, pp. 282–287, Mar. 2014.
[35] R. K. Ranjan, N. Raj, N. Bhuwal, and F. Khateb, "Single DVCCTA based high frequency incremental/decremental memristor emulator and its application," *AEU - Int. J. Electron. Commun.*, vol. 82, pp. 177–190, Dec. 2017.
[36] A. Yesil, "Floating memristor employing single MO-OTA with hard-switching behaviour," *J. Circuits, Syst., Comp.*, vol. 28, no. 2, pp. 195–207, 2018.
[37] R. K. Ranjan, N. Rani, R. Pal, S. K. Paul, and G. Kanyal, "Single CCTA based high frequency floating and grounded type of incremental/decremental memristor emulator and its application," *Microelectron. J.*, vol. 60, pp. 119–128, Feb. 2017.
[38] R. K. Ranjan, S. Surendra, S. Raushan, N. Garg, B. Kumari, and F. Khateb, "High frequency floating memristor emulator and its experimental results," *IET Circuits, Devices Syst.*, vol. 13, no. 3, pp. 292–302, May 2019.
[39] G. Kanyal, P. Kumar, S. K. Paul, and A. Kumar, "OTA based high frequency tunable resistorless grounded and floating memristor emulators," *AEU-Int. J. Electron. Commun.*, vol. 92, pp. 124–145, Aug. 2018.
[40] N. Raj, R. K. Ranjan, and F. Khateb, "Flux-controlled memristor emulator and its experimental results," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 4, pp. 1050–1061, Apr. 2020.
[41] J. Vista and A. Ranjan, "Flux controlled floating memristor employing VDTA: Incremental or decremental operation," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 40, no. 2, pp. 364–372, Feb. 2021.
[42] A. S. Elwakil, M. E. Fouda, and A. G. Radwan, "A simple model of double-loop hysteresis behavior in memristive elements," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 8, pp. 487–491, Aug. 2013.
[43] C. Sánchez-López, J. Mendoza-López, C. Muñiz-Montero, and M. A. Carrasco-Aguilar, "A floating analog memristor emulator circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 309–313, May 2014.
[44] Z. G. Cam and H. Sedef, "A new floating memristance simulator circuit based on second generation current conveyor," *J. Circuits, Syst. Comput.*, vol. 26, no. 2, pp. 29–43, 2017.
[45] P. K. Sharma, R. K. Ranjan, F. Khateb, and M. Kumngern, "Charged controlled mem-element emulator and its application in a chaotic system," *IEEE Access*, vol. 8, pp. 171397–171407, 2020.

[46] Y. Babacan, A. Yesil, and F. Gul, "The fabrication and MOSFET-only circuit implementation of semiconductor memristor," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1625–1632, Apr. 2018.
[47] A. Yesil, "A new grounded memristor emulator based on MOSFET-C," *AEU-Int. J. Electron. Commun.*, vol. 91, pp. 143–149, Jul. 2018.
[48] R. S. Tomar, S. V. Singh, and C. Chauhan, "Fully integrated electronically tunable universal biquad filter operating in current-mode," in *Proc. Int. Conf. Signal Process. Integr. Netw. (SPIN)*, Feb. 2014, pp. 549–554.
[49] T. Wang, D. Wang, and K. Wu, "Chaotic adaptive synchronization control and application in chaotic secure communication for industrial Internet of Things," *IEEE Access*, vol. 6, pp. 8584–8590, 2018.
[50] V. Grigoras and C. Grigoras, "Chaotic noise generators with periodic nonlinearities," in *Proc. Int. Symp. Signals, Circuits Syst.*, Jun. 2011, pp. 1–4.
[51] A. Buscarino, L. Fortuna, M. Frasca, L. V. Gambuzza, and G. Sciuto, "Memristive chaotic circuits based on cellular nonlinear networks," *Int. J. Bifurcation Chaos*, vol. 22, no. 03, Mar. 2012, Art. no. 1250070.

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