GUEST EDITORIAL

RESOLUTION ENHANCEMENT TECHNIQUES AND DESIGN FOR MANUFACTURABILITY: CONTAINING AND ACCOUNTING FOR VARIABILITIES IN INTEGRATED CIRCUIT CREATION

Continuous integrated-circuit miniaturization challenges lithographers to push the limit of optical lithography by ever more precise engineering and innovations. As shrinkage of device dimension outpaced the introduction of shorter-exposure wavelengths and higher-numerical-aperture lenses, resolution enhancement techniques (RETs) have become an integral part of low-k_1 manufacturing.

The first RETs are, in retrospect, rudimentary. Annular illumination, for example, was almost synonymous with off-axis illumination (OAI); lithography models used in optical proximity correction (OPC) marginally characterized photoresist dissolution. With further and further decrease of the k_1 factor, some previously insignificant phenomena are becoming material. The article entitled "Rigorous electromagnetic field mask modeling and related lithographic effects in the low k_1 and ultrahigh numerical aperture regime," by Erdmann and Evanschitzky, shows that mask topography should be considered when mask feature sizes are comparable to the exposure wavelength, and the numerical aperture approaches and exceeds one. Apodization, too, is deserving notice, as Zhang et al. point out in "Novel apodization and pellicle optical models for accurate optical proximity correction modeling at 45 and 32 nm." At 45 nm, critical dimensions can be affected by as much as 5 nm.

Lower k_1 factors also demand a higher degree of OPC sophistication. In "True process variation aware optical proximity correction with variational lithography modeling and model calibration," Yu et al. propose an OPC model that considers dose and focus fluctuations. The possibility of balancing OPC mask complexity with circuit timing constraints is explored by Gupta et al. in "Performance-driven optical proximity correction for mask cost reduction."

The last study mentioned above is an example of co-optimization, an area that is becoming indispensible as our industry seeks a holistic solution to maintain its economic well-being. In another example described by Fühner and Erdmann in "Direct optimization approach for lithographic process conditions," a genetic algorithm is used to derive the optimal mask shapes and illumination intensity distribution simultaneously.

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The RETs and co-optimization techniques discussed thus far fall into the manufacturing realm; they focus on earnest reproduction of layouts. Design for manufacturability (DFM) attempts design–manufacturing co-optimization, possibly through modification of the target layout, with the goal of reducing physical and, ultimately, electrical variability. From this angle, we can perceive DFM as a RET that takes co-optimization to a broader level, and, in the process, necessitates modification of the design–manufacturing interface.

The traditional design to silicon flow revolves around design rules. When a layout—geometrical shapes that collectively describe a circuit—adheres to all design rules, the fabricated circuit will function according to the design. Design rules are thus the embodiment of traditional DFM. By allowing for division of labor, design rules and the associated circuit models and geometrical description formats have enabled the exponential increase in integrated circuit creation productivity over the last few decades. Any successful modification to the design–manufacturing interface must respect this encapsulation of design and manufacturing expertise.

Complementing design rules with a process model has emerged as a promising DFM approach. Two fundamental issues nevertheless linger: the model form and its use model. In "Through-process modeling for design-for-manufacturability applications," Mansfield et al. elucidate that the attributes of a DFM model are dependent on the particular DFM application. Complicating matters further is the time axis. Physical design of the most advanced circuits commences prior to stabilization of the process; an accurate DFM model may initially be unavailable.

With regard to the use model, Ho et al., in "Lithography-simulation-based design for manufacturability rule development: an integrated circuit design house's approach," propose a method to derive DFM rules based on an approximate process model without OPC knowledge. Balasinski et al. also take such a correct-by-construction approach in "Layout techniques and rules to reduce process related variability." Rather than placing layout restrictions via DFM rules, Kobayashi et al., in "Automated hot-spot fixing system applied for metal layers of 65-nm logic devices," introduce small-scale modifications to regions in the layout that are susceptible to lithography variability, the assumption being that such slight modifica-

tions do not have noticeable impact on timing and power characteristics.

Jhaveri et al. describe an adaptive restricted design rules (RDR) approach in "Maximization of layout printability/manufacturability by extreme layout regularity." Prior to physical design, the set of logic functions needed to realize a circuit is first analyzed and minimized. Imposing RDR on the physical designs of this limited set of logic functions holds the promise of yield improvement without (excessive) chip size increase.

Underlying all these investigations is the realization that DFM is multidisciplinary optimization. We seek a global optimum among design complexity, manufacturing yield, and opportunity cost. It is likely that the DFM use model will also be multiple. The *Journal of Micro/Nanolithography, MEMS, and MOEMS* would like to offer this special section as a snapshot record of the continuous evolution of resolution enhancement techniques and design for manufacturability.

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Guest Editor