Resonance Analysis in Parallel Voltage-Controlled Distributed Generation Inverters

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***Abstract*—Thanks to the fast responses of the inner voltage and current control loops, the dynamic behaviors of parallel voltage-controlled Distributed Generation (DG) inverters not only relies on the stability of load sharing among them, but subjects to the interactions between the voltage control loops of the inverters and the remaining system dynamics. This paper addresses the later interactions and the consequent resonances through the frequency-domain analysis of the inverters output impedances and the remaining equivalent network impedance. Furthermore, impacts of the virtual output impedance loop and the voltage feedforward loop in the current controller are evaluated based on such an impedance interactions analysis. Simulation results are presented to confirm the validity of the theoretical analysis.**

I. INTRODUCTION

Driven by the emerging active distribution networks in the development of smart grids, the inverter-interfaced Distributed Generation (DG) systems have been undergoing a fast growth in the power grid [1], [2]. These DG inverters are expected to operate in both current- and voltage-controlled modes, thereby providing more reliable and efficient electricity services to the customers [3]. Consequently, the islanded networks that are dominated by multiple DG inverters are becoming important components of the smart distribution grids [4]. The increasing concerns over the control and stability of such inverter-based islanded systems have been raised [5].

The active power-frequency (P-ω) droop that mimics the speed-governing mechanism of synchronous generators, and the reactive power-voltage (Q-V) droop are usually used for the load sharing in the parallel DG inverters [6]. Furthermore, to overcome the power coupling caused by a high R/X ratio of the low-voltage distribution lines, several improved droop-based power control schemes have been reported [7]. Among them, the virtual output impedance loop that is similar to the load compensator in the excitation system of the synchronous generator shows superior performances [8].

In order to properly design the droop coefficients and the virtual output impedance, small-signal stability analysis of the parallel voltage-controlled inverters have been well discussed in [9], [10]. However, notice that the dynamic behaviors of the inner current and voltage control loops are neglected in those analyses, due to the well separation between the bandwidth of the outer power control loop and the inner control loops. As a result, the interactions between the output voltage control loop of the DG inverter and the remaining network dynamics are often overlooked [11]. Unlike traditional power systems where synchronous generators usually have large time constants, the much faster responses of the voltage and current control loops in the DG inverters tend to result in the additional resonances and small-signal oscillations at the frequencies higher than the system fundamental frequencies. Therefore, there is an urgent need to explore the dynamic interactions between the inner control loops of the parallel DG inverters.

In this paper, the dynamic interactions between the output voltage control loops of the parallel voltage-controlled DG inverters are addressed. The potential voltage resonances and unstable oscillations caused by such interactions are identified through the impedance-based stability analysis. The influences of the virtual output impedance loop and the output voltage feedforward term in the inner current control loop are assessed in the frequency-domain. Finally, simulations are performed to validate the theoretical analysis results.

II. MODELING OF PARALLEL DG INVERTERS

Fig. 1 represents an islanded three-phase network, where two parallel inverter-interfaced DG units are connected via the distribution feeders to the common load bus, respectively. Constant DC-link voltages of the DG inverters are assumed.

Fig. 2 illustrates the control block diagrams for the i-th DG inverter (i=1, 2). The multiloop control scheme is employed, including 1) the inner voltage and current control loops, 2) the intermediate virtual output impedance loop, and 3) the outer droop-based power controller. Since the interactions between the inner voltage and current control loops of DG inverters are of the main concerns, the low-frequency power oscillations caused by the dynamics of the droop controls are disregarded. In the inner control loops, the proportional current controller is adopted for the over-current protection and a better LC-filter resonance damping [12], and the Proportional Resonant (PR) voltage controller is used for the zero steady-state error.

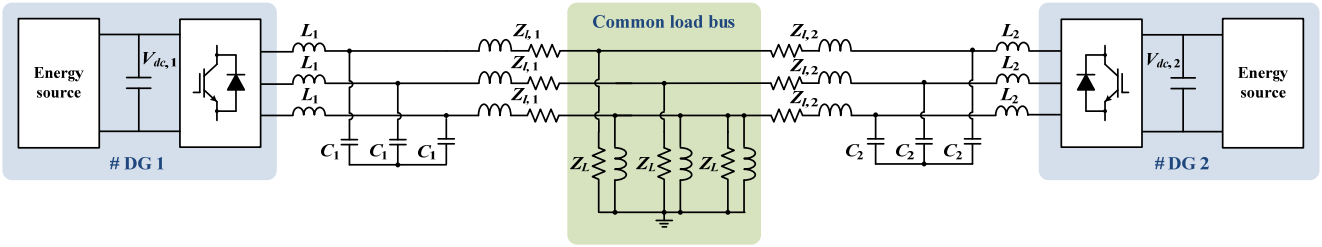


Fig. 1. An islanded three-phase network with two inverter-interfaced DG units and a common load.

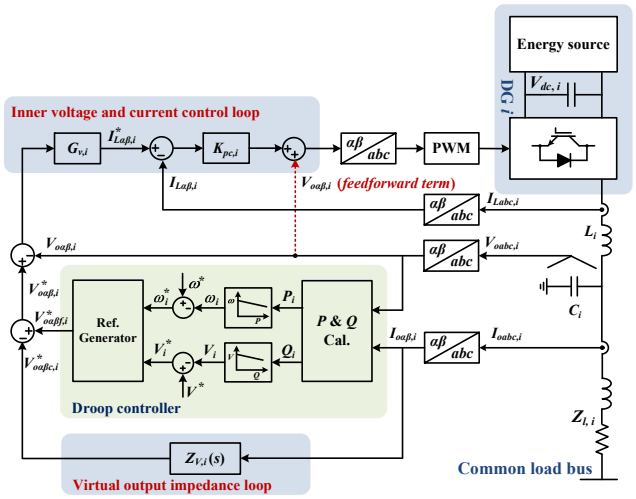


Fig. 2. Control block diagram for the *i*-th DG inverter (*i*=1, 2).

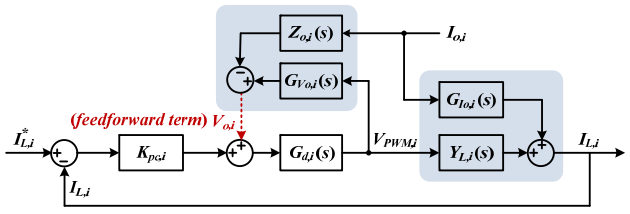


Fig. 3. Simplified inner current control loop for the *i*-th DG inverter.

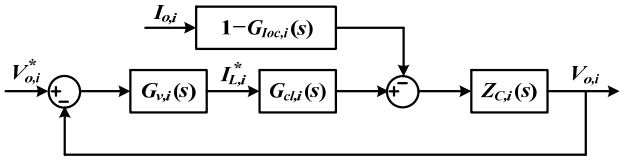


Fig. 4. Simplified inner voltage and current control loops for the *i*-th DG inverter.

It is known that the terminal behavioral model of the DG inverter is essential to perform an impedance-based stability analysis [13]. Since the DC voltage is assumed to be constant, the DC inverter can be seen as a linear system for small-signal stability analysis [14].

From Fig. 2, it is observed that the output *LC*-filter can be modeled by a two-input, two-output system as follow

$$\begin{bmatrix} I_{L,i}(s) \\ V_{o,i}(s) \end{bmatrix} = \begin{bmatrix} G_{Io,i}(s) & Y_{L,i}(s) \\ -Z_{o,i}(s) & G_{Vo,i}(s) \end{bmatrix} \begin{bmatrix} I_{o,i}(s) \\ V_{PWM,i}(s) \end{bmatrix} \tag{1}$$

$$G_{Io,i}(s) = \frac{Z_{C,i}(s)}{Z_{L,i}(s) + Z_{C,i}(s)}, \quad Y_{L,i}(s) = \frac{1}{Z_{L,i}(s) + Z_{C,i}(s)} \tag{2}$$

$$Z_{o,i}(s) = \frac{Z_{L,i}(s) Z_{C,i}(s)}{Z_{L,i}(s) + Z_{C,i}(s)}, \quad G_{Vo,i}(s) = \frac{Z_{C,i}(s)}{Z_{L,i}(s) + Z_{C,i}(s)} \tag{3}$$

where $V_{PWM,i}$ (*s*) is the output voltage of the *i*-th inverter, $Z_{C,i}$ (*s*) and $Z_{L,i}$(*s*) are the impedances for the output capacitor and inductor, respectively. Thus, the inner current control loop can be simplified, as shown in Fig. 3. Supposing that without the voltage feedforward term first, the dynamic behavior of the current control loop can be given as

$$I^*_{L,i}(s) = G_{cl,i}(s) I_{L,i}(s) + G_{Ioc,i}(s) I_{o,i}(s) \tag{4}$$

where $G_{cl,i}$ (*s*) is the closed-loop gain of the current control loop and $G_{Ioc,i}$ (*s*) denotes the closed-loop effect of the load current, which are given by

$$G_{cl,i}(s) = \frac{T_{c,i}(s)}{1 + T_{c,i}(s)}, \quad G_{Ioc,i}(s) = \frac{G_{Io,i}(s)}{1 + T_{c,i}(s)} \tag{5}$$

$$T_{c,i}(s) = K_{pc,i} G_{d,i}(s) Y_{L,i}(s) \tag{6}$$

$$G_{d,i}(s) = e^{-1.5 T_s s} \approx \frac{1 - 0.75 T_s s + (1.5 T_s s/12)^2}{1 + 0.75 T_s s + (1.5 T_s s/12)^2} \tag{7}$$

where $T_{c,i}(s)$ is the open-loop gain of the current control loop. $G_{d,i}(s)$ is the approximated 1.5 sampling period (T_s) delay. By closing the output voltage control loop, the inner voltage and current control loops are simply represented in Fig. 4. Thus, the output voltage control loop can be modeled as

$$V_{o,i}(s) = G_{clv,i} V^*_{o,i}(s) - Z_{ov,i}(s) I_{o,i}(s) \tag{8}$$

$$G_{clv,i}(s) = \frac{T_{v,i}(s)}{1 + T_{v,i}(s)}, \quad Z_{ov,i}(s) = \frac{Z_{C,i}(s)}{1 + T_{v,i}(s)} \left(1 - G_{Ioc,i}(s)\right) \tag{9}$$

$$T_{v,i}(s) = G_{v,i}(s) G_{cl,i}(s) Z_{C,i}(s) \tag{10}$$

where $G_{clv,i}(s)$ is the closed-loop gain of the voltage control loops, $Z_{ov,i}(s)$ is the closed-loop output impedance, and $T_{v,i}(s)$ is the open-loop gain of the voltage control loop. $G_{v,i}(s)$ is the PR voltage controller, which is given by [15]

$$G_{v,i}(s) = K_{pv,i} + \frac{K_{rv,i}\omega_{c,i}s}{s^2 + \omega_{c,i}s + \omega_0^2} \tag{11}$$

Considering the virtual output impedance loop $Z_{V,i}(s)$, the voltage control systems can be derived by

$$V_{o,i}(s) = G_{clv,i}(s)V_{o,i}^*(s) - \left(Z_{ov,i}(s) + G_{clv,i}(s)Z_{V,i}(s)\right)I_{o,i}(s) \tag{12}$$

$$Z_{tov,i}(s) = Z_{ov,i}(s) + G_{clv,i}(s)Z_{V,i}(s) \tag{13}$$

where $Z_{tov,i}(s)$ is the total closed-loop output impedance. It can be seen that the actual effect of the virtual output impedance is affected by the bandwidth of the inner control loops, and the virtual impedance loop has no effect on the closed-loop gain of the inner control loops.

On the other hand, taking the output voltage feedforward term into account, the dynamic behavior of the current control loop is modified as follows

$$T'_{c,i}(s) = \frac{T_{c,i}(s)}{1 - G_{Vo,i}(s)G_{d,i}(s)} \tag{14}$$

$$G'_{cl,i}(s) = \frac{T'_{c,i}(s)}{1 + T'_{c,i}(s)} \tag{15}$$

$$G'_{loc,i}(s) = \frac{G_{Io,i}(s)}{1 + T'_{c,i}(s)} - \frac{Z_{o,i}(s)G_{d,i}(s)Y_{L,i}(s)}{\left(1 + T'_{c,i}(s)\right)\left(1 - G_{d,i}(s)G_{Vo,i}(s)\right)} \tag{16}$$

Substituting (14), (15) and (16) into (9) and (10), the terminal behavioral model of the *i*-th inverter is modified as

$$V_{o,i}(s) = G'_{clv,i}V_{o,i}^*(s) - Z'_{ov,i}(s)I_{o,i}(s) \tag{17}$$

$$G'_{clv,i}(s) = \frac{T'_{v,i}(s)}{1 + T'_{v,i}(s)}, \quad Z'_{ov,i}(s) = \frac{Z_{C,i}(s)}{1 + T'_{v,i}(s)}\left(1 - G'_{loc,i}(s)\right) \tag{18}$$

$$T'_{v,i}(s) = G_{v,i}(s)G'_{cl,i}(s)Z_{C,i}(s) \tag{19}$$

It is worthy to note that the output voltage feedforward term affects both the closed-loop gain of the inner control loops and the closed-loop output impedance, which is markedly different from the virtual output impedance loop.

Following the derivation of the terminal behavioral model of the *i*-th DG inverter, the closed-loop model for the islanded three-phase network shown in Fig. 1 is thus built, as shown in Fig. 5. The equivalent load impedance $Z_{load,i}(s)$ can be used to represent the remaining network dynamics, which includes the closed-loop output impedance of the other DG inverter and the distribution lines, as well as the common load. Consequently, the interactions between the inner control loops of the *i*-th DG inverter and the remaining network dynamics can be modeled by a minor feedback loop, as shown in Fig. 6. The loop gain of such a minor feedback loop $T_{m,i}(s)$ can be given by

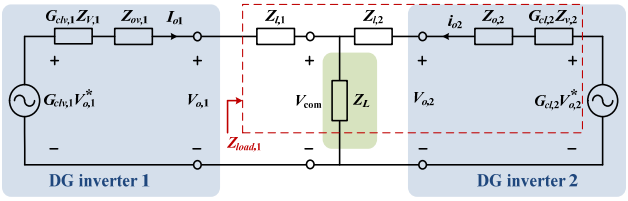


Fig. 5. Closed-loop model of the islanded three-phase network.

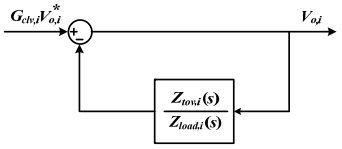


Fig. 6. Minor feedback loop for the *i*-th DG inverter.

$$T_{m,i}(s) = \frac{Z_{tov,i}(s)}{Z_{load,i}(s)} \tag{20}$$

Thus, the voltage resonances caused by such interactions can be clarified via the frequency response of the loop gain $T_{m,i}(s)$.

III. Impedance-Based Stability Analysis

On the basis of the derived closed-loop system model, the impedance-based stability analysis is performed in frequency-domain. For the sake of simplicity, only the balanced network is considered here, and the two DG inverters are assumed to have the same filter constants and controller parameters. Table I summarizes the system electrical constants, and Table II lists the main controller parameters of the DG inverters.

First, supposing that neither the virtual output impedance loop nor the output voltage feedforward term is applied, the frequency response of the open-loop gain for the inner voltage control loop $T_{v,i}(s)$ is shown in Fig. 7. It is seen that a stable closed-loop terminal behavior of the *i*-th DG inverter across the output capacitor is obtained.

Then, considering the loading effect of the equivalent load impedance $Z_{load,i}(s)$, the interactions between the *i*-th inverter and the remaining network dynamics is assessed. Fig. 8 shows the frequency responses of $Z_{ov,i}(s)$ and $Z_{load,i}(s)$. The phase differences at the intersection points of two impedances imply the phase margin of the minor feedback loop. The intersection points where the phase differences are larger than 180° denote the resonance frequencies.

From Fig. 8, notice that $Z_{o,i}(s)$ behaves as a capacitance at high frequencies, whereas $Z_{load}(s)$ becomes an inductance due to the feeders impedances. As a consequence, the series RLC circuit is formed in the minor feedback loop. Furthermore, it is clear that the phase difference at the intersection point, 1770 Hz, is larger than 180 degrees, which represents the resonance

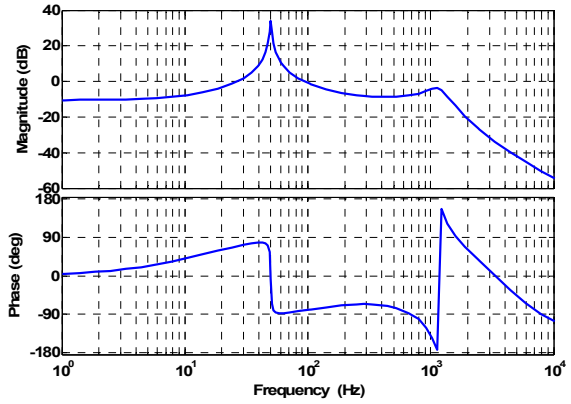


Fig. 7. Frequency response of the open-loop gain of the inner voltage control loop for the *i*-th DG inverter.

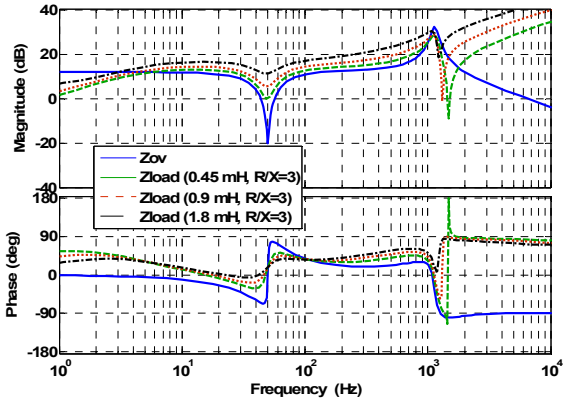


Fig. 9. Frequency responses of $Z_{load,i}(s)$ with the different distribution line impedances and $Z_{ov,i}(s)$.

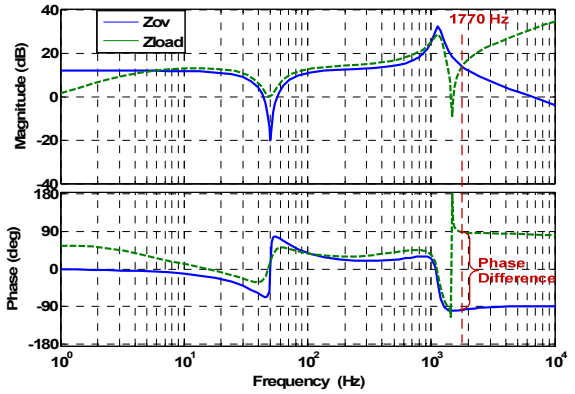


Fig. 8. Frequency responses of $Z_{ov,i}(s)$ and the equivalent load impedance $Z_{load,i}(s)$.

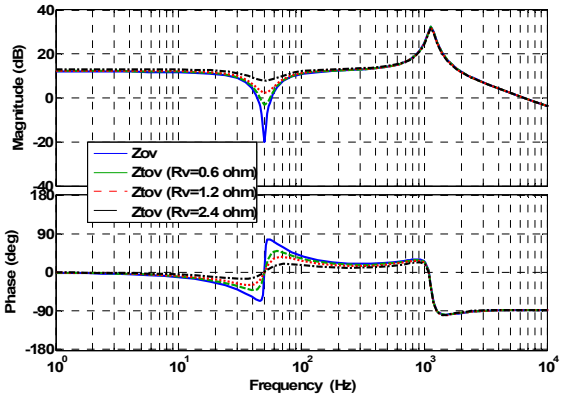


Fig. 10. Frequency responses of $Z_{ov,i}(s)$ and the equivalent load impedance $Z_{load,i}(s)$.

frequency. Hence, even though a stable terminal behavior of single inverter is obtained, the interactions between the inner control loops of parallel inverters can still lead to small-signal instability problem.

Fig. 9 compares the frequency responses of $Z_{load,i}(s)$ with the different distribution line impedances and $Z_{ov,i}(s)$. It can be observed that the phase margin of the minor feedback loop is increased with the increase of the line impedances. This fact implies that such an undesired resonance can be avoided by reshaping the interconnecting impedances between the parallel DG inverters. Under the given common load and distribution lines, this can be achieved by changing the closed-loop output impedances of inverters.

From (9), (13) and (18), it can be noted that there are three ways to change the closed-loop output impedance of the *i*-th inverter, which include 1) adjusting the open-loop gain of the voltage control loop, 2) applying the virtual output impedance loop, and 3) using the output voltage feedforward term in the current control loop. In [11], the damping of resonance via reducing the open-loop gain of the voltage control system has been discussed. Thus, the damping effects of the latter two control methods are investigated in this work.

Fig. 10 shows the frequency behavior of the total closed-loop output impedance $Z_{tov,i}(s)$ with the different virtual output impedances and the original output impedance $Z_{ov,i}(s)$. Notice that only the virtual resistance is considered. It is observed that the total closed-loop output impedance has very few changes at the resonance frequency, which implies the virtual output resistance loop has no effect on damping of such a resonance.

In order to see the effect of the output voltage feedforward term in the current control loop, the frequency responses of the open-loop gain of the current control loop and the closed-loop effect of load current are plotted in Fig. 11. Fig. 11 (a) shows a comparison of the open-loop gains before and after using the output voltage feedforward term. It is clear that the resonance peak caused by the output *LC*-filter is damped by the voltage feedforward term. Fig. 11 (b) compares the closed-loop effect of the load current derived in (5) and (16). It can be seen that the response magnitude is reduced.

Fig. 12 (a) compares the frequency responses of the open-loop gains of the voltage control loop derived in (10) and (19). It is seen that the loop gain at the low frequencies is increased with the output voltage feedforward term. Fig. 12 (b) shows the frequency behaviors of the closed-loop output impedances in (9) and (18). It is obvious that the resonance peak in $Z_{ov,i}(s)$ is damped by the output voltage feedforward term.

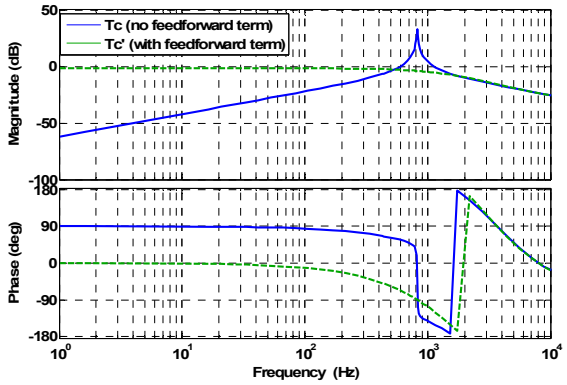
Fig. 13 depicts the frequency responses of the closed-loop output impedance and the equivalent load impedance with the

TABLE I. SYSTEM ELECTRICAL CONSTANTS (SEE FIG.1)

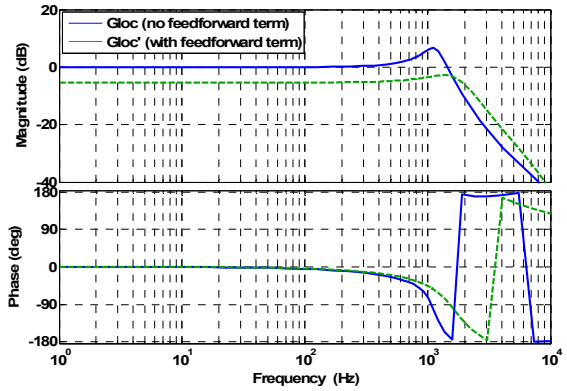
Electrical Constants		Values
DG inverters (DG1 and DG2)	DC voltage ($V_{dc,1} = V_{dc,2}$)	750 V
	Filter inductor ($L_1 = L_2$)	1.5 mH
	Filter capacitor ($C_1 = C_2$)	25 μF
	Switching frequency (f_{sw})	10 kHz
Distribution feeders ($Z_{l,1} = Z_{l,2}$)	Line inductance ($L_{l,1} = L_{l,2}$)	0.45 mH
	R/X ratio	3
Common load (Z_L)	Resistance load (R_L)	80 Ω
	Inductance load (L_L)	166 mH

TABLE II. MAIN CONTROLLER PARAMETERS OF DG INVERTERS

Controller Parameters		Values
Sampling period	$T_{s,1} = T_{s,2}$	10^{-4} s
Current controller	$K_{pc,1} = K_{pc,2}$	5
PR voltage controller	$K_{pv,1} = K_{pv,2}$	0.06
	$K_{rv,1} = K_{pv,2}$	10
	$\omega_{c,1} = \omega_{c,2}$	8 rad/s
	ω_0	100π rad/s
Active power droop controller	$n_1 = n_2$	10^{-5}
Reactive power droop controller	$m_1 = m_2$	10^{-5}

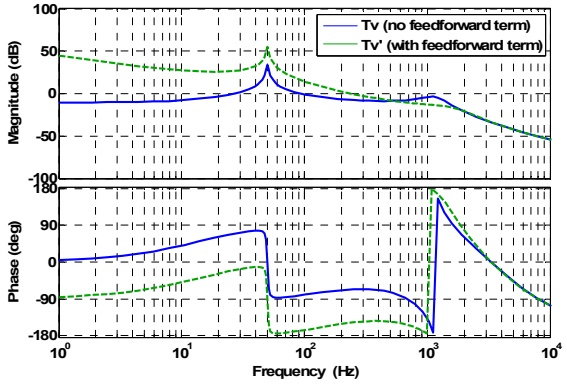


(a)

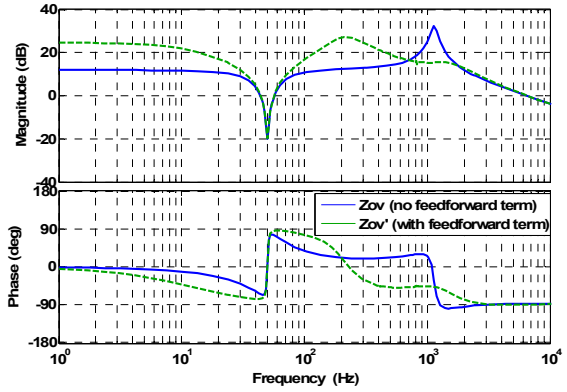


(b)

Fig. 11. Frequency responses of the current control loop with and without the output voltage feedforward term. (a) Open-loop gain. (b) Closed-loop effect of the load current.



(a)



(b)

Fig. 12. Frequency responses of the voltage control loop with and without the output voltage feedforward term. (a) Open-loop gain. (b) Closed-loop output impedance.

output voltage feedforward term in the current control loop. Compared to Fig. 8, it is evident that the phase differences at the intersection points are smaller than 180°, which indicates that the resonance resulting from the interactions between the inner control loops of the parallel DG inverters are effectively damped by using the voltage feedforward term.

IV. SIMULATION RESULTS

To validate the above frequency-domain stability analysis, the time-domain simulations of the islanded network shown in Fig. 1 is performed in MATLAB/Simulink, and the electrical circuit is built with the SimPowerSystems toolbox. The model parameters are referred to Table I and Table II.

Fig. 14 shows the simulated output voltages of the parallel inverters without using the virtual output impedance loop and the output voltage feedforward term. The two DG inverters are connected in parallel at the instant of 0.2 s. It is evident that the voltage resonances arise when the inverters are connected in parallel. Fig. 15 gives the harmonic spectra for the resonant voltages, where a good match with the impedance interactions

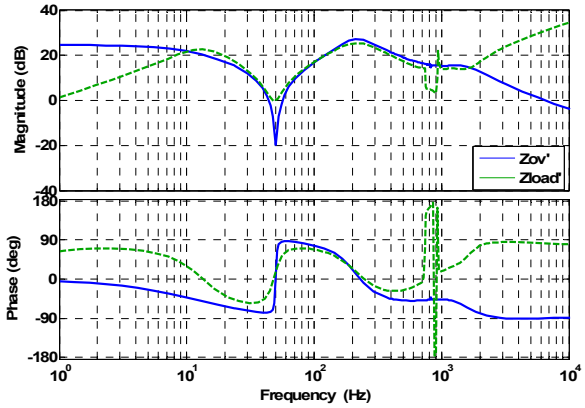


Fig. 13. Frequency responses of the closed-loop output impedance and the equivalent load impedance with the voltage feedforward term.

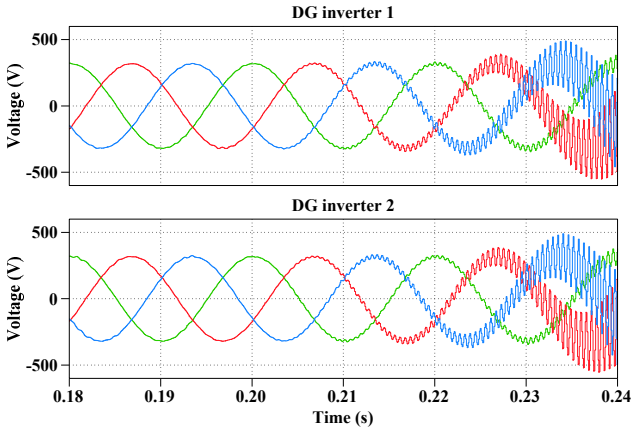


Fig. 14. Simulated output voltages of the parallel inverters without using the virtual output impedance loop and the output voltage feedforward term.

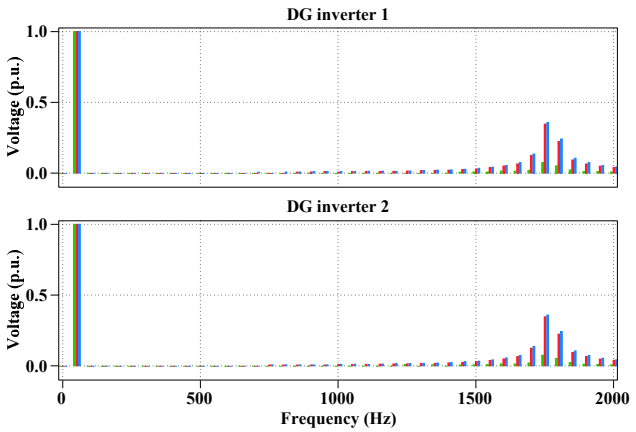
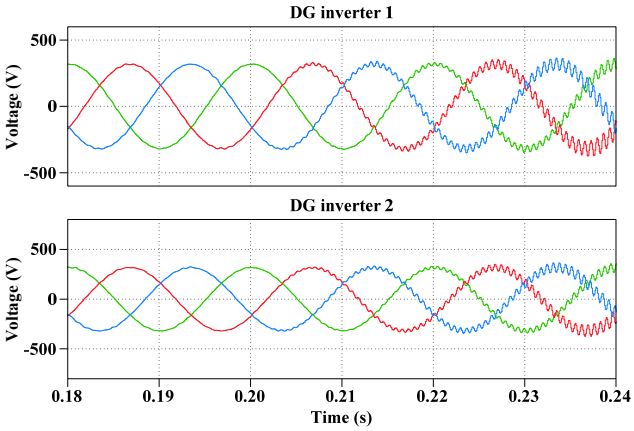


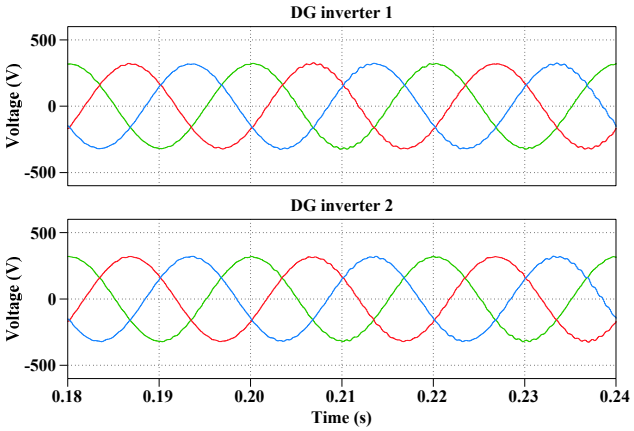
Fig. 15. Harmonic spectra for the resonant voltages shown in Fig. 14.

analysis in Fig. 8 can be observed.

Fig. 16 shows the output voltages of the parallel inverters with the increase of the distribution line impedances. It is seen that once connecting the two inverters in parallel at the instant of 0.2 s, the resonances still arise when the line inductances are 0.9 mH, but disappear for the case that the line inductances



(a)



(b)

Fig. 16. Simulated output voltages of the parallel inverters with the increase of the distribution line impedance. (a) $L_{l,i}$=0.9 mH. (b) $L_{l,i}$=1.8 mH.

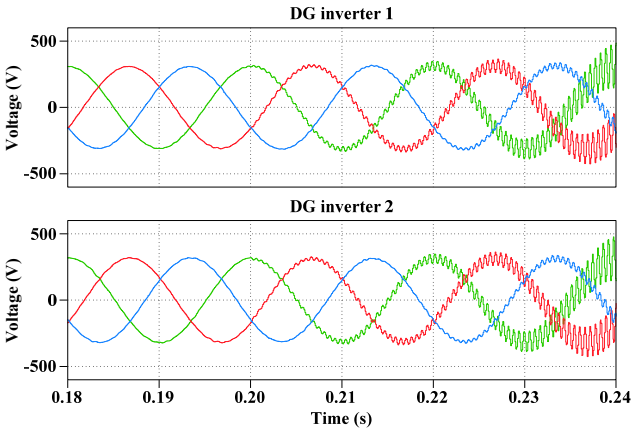


Fig. 17. Simulated output voltages of the parallel inverters when the virtual resistance, 2.4 Ω, is applied to the control system.

are 1.8 mH. This phenomenon validates the frequency-domain analysis of the minor-loop gain in Fig. 9.

Fig. 17 shows the output voltages of the parallel inverters when the virtual resistance, 2.4 Ω, is applied. It is obvious that the voltage resonances still arise after 0.2 s, which implies that

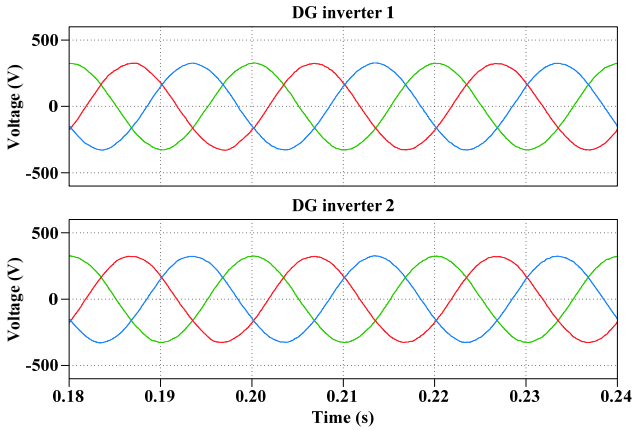


Fig. 18. Simulated output voltages of the parallel inverters when the output voltage feedforward term is used in the current control loop.

very little damping effect can be obtained via using the virtual output impedance loop. This confirms the frequency behaviors of the total output impedance shown in Fig. 10.

In contrast, Fig. 18 depicts the output voltages of parallel inverters for the case that the output voltage feedforward term is applied in the current control loop. It is observed that the voltage waveforms keep sinusoidal after connecting the DG inverters in parallel, which validates the frequency-domain analysis shown in Fig. 13. Hence, it can be concluded that the use of the output voltage feedforward term in the inner current control loop can help to stabilize the interactions of parallel voltage-controlled DG inverters.

V. CONCLUSIONS

This paper has discussed the potential voltage resonances caused by the control loop interactions of the parallel voltage-controlled DG inverters. In order to clarify the nature of such undesired resonances, the impedance-based analysis has been performed on an islanded network with two parallel voltage-controlled inverters. It has shown that a series *LC* resonance may be raised depending on the phase difference between the inverter output impedance and the equivalent load impedance of the remaining network. The damping effects of the virtual output impedance loop and the output voltage feedforward term in the inner current control loop have been evaluated in the frequency domain. It has found that the virtual impedance has no effect on stabilizing the controller interactions, whereas an output voltage feedforward term can help to dampen out the potential resonances. Simulation results are presented to validate the frequency-domain analysis.

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