IEEE Transactions on Nuclear Science, Vol.NS-25, No.6, December 1978

RESPONSE OF MNOS CAPACITORS TO IONIZING RADIATION AT 80°K

Nelson S. Saks

Abstract

MNOS capacitors with oxide thicknesses 85Å-600Å and silicon nitride thicknesses 200-2000Å have been irradiated with 2 MeV electrons at 80°K. Measured flatband shifts are found to depend on both polarity and magnitude of the applied field, oxide thickness, nitride thickness, and variations in device processing. For negative gate bias and effective applied fields 1-2x10^6 V/cm, ΔV_{FB} is independent of device processing and magnitude of the applied field. For these bias conditions, it is shown that flatband shifts in all MNOS samples may be explained by considering only generation and trapping of holes in the oxide. The holes travel a mean free path of 125±25Å in the oxide before being trapped. For positive gate bias, electrons generated in the oxide are trapped at the oxide-nitride interface and/or in the bulk of the nitride, compensating the effect of the positively charged trapped holes in the oxide, and producing a relatively smaller ΔV_{FB} for positive bias. The electron trapping process is considerably processing dependent. For high effective applied fields exceeding ± 2x10^6 V/cm, a strongly field-dependent mechanism of charge generation in the gate insulator is observed.

Introduction

The subject of radiation damage in MNOS (metal-silicon nitride-silicon dioxide-silicon) devices has been of interest to the radiation community for many years. Work by Stanley,[1] Perkins et al,[2] and Newman and Wegener,[3] among others, in the late 1960's established that MNOS devices often show substantial improvement in tolerance to ionizing radiation when compared with most pure SiO_2 MOS devices.[4] Recently, interest in the radiation attributes of the MNOS structure has decreased since the development of radiation hard "clean" SiO_2 MOS devices. However, at low temperatures, all SiO_2 films, including the radiation hard "clean" oxides, show the same build-up of trapped holes in the oxide, and are highly sensitive to ionizing radiation.[5] Consequently, a gate insulator structure more tolerant to ionizing radiation than SiO_2 is needed for certain low temperature applications of MOS devices such as CCD signal processors for infrared arrays.

The purpose of this work is to study the radiation sensitivity of the MNOS structure at 80°K. Also, we hoped that performing the irradiation at low temperatures would prove to be an advantage in the interpretation of the experimental results because of recent advances in the understanding of irradiation effects in SiO_2. It now appears that the buildup of trapped holes in SiO_2 when exposed to ionizing radiation at 80°K is the same in all thermally grown SiO_2 layers, independent of variations in processing (this is not true for irradiation of SiO_2 at ~300°K).[6,7] Consequently, any differences between charge buildup in the MNOS structure and that expected for the SiO_2 alone should be due to charge generation and trapping in the nitride or at the oxide-nitride interface. It is assumed throughout this work that the thermally grown SiO_2 layer in the MNOS structure behaves exactly the same as other SiO_2 films. It is also assumed that both the oxide and nitride have uniform bulk properties and are separated by an infinitely thin interface layer.

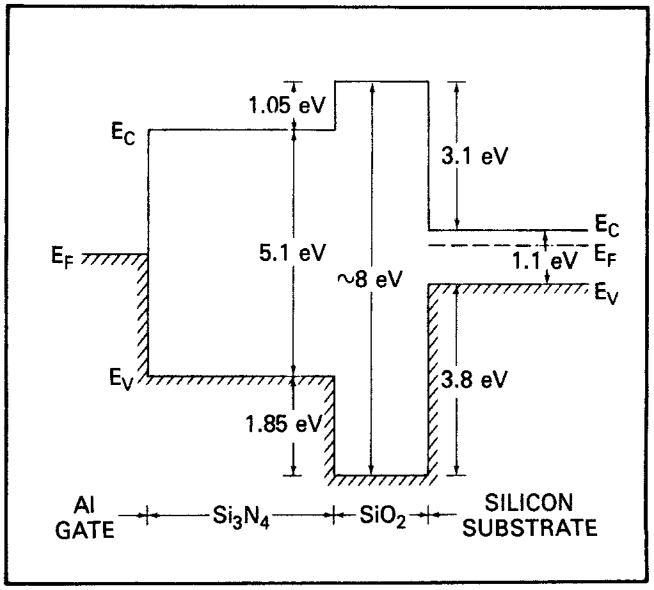

Fig. 1. Energy-band diagram of the MNOS structure.

A band diagram of the MNOS structure is shown in Figure 1.[8] Ionizing radiation incident on this structure will create electron-hole pairs in both the oxide and nitride layers. For applied fields greater than 10^6 V/cm, most of the electron-hole pairs created in the oxide will escape recombination.[9] The electrons are mobile and are swept out of the oxide by the applied field.[6] At low temperatures (~80°K), the holes created by the radiation are trapped near the point of creation.[9] For carriers generated in the SiO_2, it is apparent from Figure 1 that no potential energy barriers to either electron or hole motion exist at either of the oxide interfaces.

Much less is known about the generation and trapping of free carriers created by ionizing radiation in silicon nitride compared to SiO_2. For a radiation exposure of 2 MeV electrons required to produce one Rad (Si), 1.0-1.5x10^{13} electron-hole pairs/cm^3 will be created in Si_3N_4 and 8.5x10^{12} pairs/cm^3 in the SiO_2. (The value for SiO_2 is based on 18 eV/pair,[6] while the value for Si_3N_4 is calculated based on the approximation that the production of one electron-hole pair consumes 2-3 times bandgap in energy for high energy radiation.) Although these generation rates for SiO_2 and Si_3N_4 are not significantly different, previous MNOS radiation experiments appear to show that charge buildup in the nitride is substantially smaller than in SiO_2. Referring to Figure 1, it is unlikely that either electrons or holes created in the nitride which escape recombination will have sufficient energy to surmount the potential barriers at the oxide-nitride interface (1.05 volts for electrons in the nitride conduction band, and 1.85 volts for holes in the nitride valence band). Consequently, it appears that most of electron-hole pairs created by ionizing radiation in silicon nitride must recombine before being separated by the applied field. Fast recombination of carriers has been proposed by P. F. Schmit et al. to explain cathodoluminescence studies of silicon oxynitride[10] with a composition of about 80% silicon nitride.

Considering only hole generation and trapping in the SiO_2 region of the MNOS capacitor, and assuming uniform trapping of the holes within the SiO_2 at the

---

The author is with the Naval Research Laboratory, Washington, D. C. 20375.

point of creation, the trapped holes contribute to the flatband shift by:

$$\Delta V_{FB} = -\rho_h \, t_{ox} \left[\frac{t_N}{\epsilon_N} + \frac{t_{ox}}{2\epsilon_{ox}}\right] \qquad (1)$$

where t_N, t_{ox}, ϵ_N, and ϵ_{ox} are the thickness and dielectric constant of the nitride and oxide, respectively. ρ_h is the charge density of uniformly trapped holes created in the SiO_2 by the ionizing radiation, and is dependent on the applied electric field. In the MNOS structure, for $t_{ox} \ll t_N$, Eq. (1) reduces to:

$$\Delta V_{FB} = -\rho_h \, t_{ox} \, t_N/\epsilon_N \qquad (2)$$

Therefore, for MNOS structures with thin SiO_2 layers, this simple model predicts ΔV_{FB} linearly proportional to t_{ox}, and not proportional to the square of the oxide thickness as observed for pure oxide MOS structures at 80°K.[5]

Sample Preparation and Irradiation

The MNOS capacitors were fabricated on <100> 3-5 Ω-cm n-type silicon wafers as follows: (1) peroxide clean, (2) thermal oxide growth in O_2 at 900°C, (3) 30 min anneal in H_2 at 900°C to reduce the fast surface state density, (4) CVD nitride deposition at 800°C, (5) aluminum deposition and photoengraving of aluminum gate capacitors, and (6) aluminum sinter at 450°C in N_2 for 30 min. The CVD nitride is obtained from decomposition of $SiCl_2H_2$ with NH_3, and has a dielectric constant of 7.8 as deposited. The thickness of this nitride will sometimes be referred to here as "effective thickness," defined as the thickness required to contribute the same capacitance to the gate insulator if the dielectric constant were the same as for SiO_2 (3.9). The effective thickness of the CVD nitride in this work equals 3.9/7.8 or 1/2 its real thickness. Likewise, effective applied field is defined as applied bias divided by the sum of oxide thickness and effective nitride thickness.

A few selected wafers received additional high temperature processing after the nitride deposition as follows: (1) CVD SiO_2 deposition at 400°C, (2) photo-engraving of capacitors, (3) 900°C phosphorus diffusion between the capacitors, (4) removal of CVD oxide, (5) 900°C wet oxide growth in the phosphorus doped regions, and (6) aluminum evaporation and photo-engraving. In addition, one sample (14-11 in Fig. 6) was fabricated with this 900°C processing and phosphorus doped polysilicon gates. All samples were bonded and checked to insure dc leakage currents less than 10^{-12} amp. at 10V gate bias.

After cooling to 80°K in a vacuum dewar, the MNOS capacitors were irradiated under bias with 2 MeV electrons. Flatband shifts were obtained within 10 min. of each sequential irradiation using 1 MHz C-V curves. Annealing of ΔV_{FB} was measured for several samples irradiated to several volt shifts for both positive and negative bias. Annealing of ΔV_{FB} from 5 min. to 6 hrs was ~5%, indicating that very little annealing of the flatband shift occurs over this time scale.

Previous measurements of fast surface state densities (N_{ss}) generated by ionizing radiation in MNOS capacitors at 300° K indicate that generation of surface states is smallest for devices with thin SiO_2 layers.[11] For the radiation exposures used in these experiments (up to 3×10^6 Rad(Si.)), no significant distortion of the C-V curves was observed in samples irradiated at 80°K with less than 200Å thick SiO_2 layers. Measurements of N_{ss} using the conductance technique were made at 300°K on several samples with 100Å SiO_2 before and after irradiation at 80°K.[12] For total doses exceeding 1 Mrad(Si), there was no measurable increase in N_{ss} at midgap. Consequently, it is assumed that the radiation-induced flatband shifts are entirely due to buildup of trapped charge in the gate insulators with negligible contribution from the generation of charged surface states.

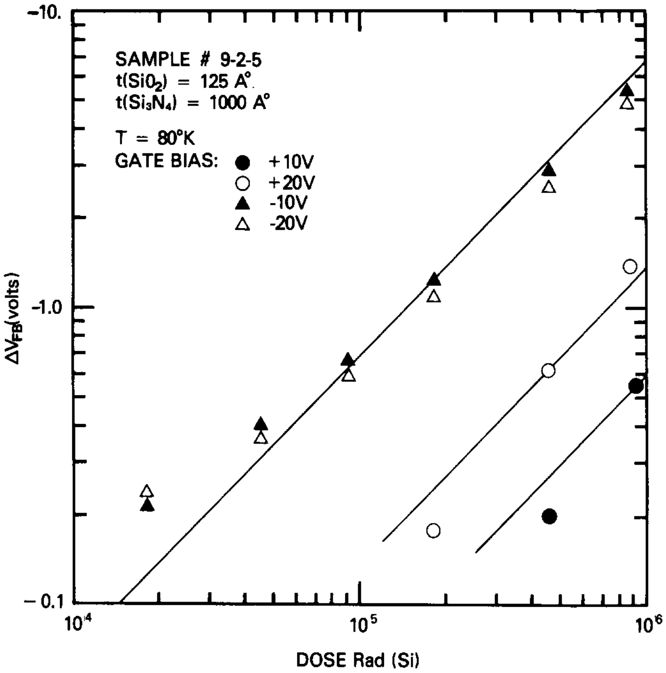

Fig. 2. Flatband shift (ΔV_{FB}) at 80°K vs radiation dose (2 MeV electrons) for a set of MNOS capacitors with different gate bias.

Flatband shift (ΔV_{FB}) vs. dose is shown in Figure 2 for a typical set of MNOS capacitors at 80°K under different gate bias conditions. These capacitors are from a single wafer with 125Å SiO_2 and 1000Å Si_3N_4 layers. The solid lines with unity slope are drawn for best fit to the data near ΔV_{FB} equal to 1 volt where all samples showed reasonably good fit to linear dependence. In the following graphs where the data is presented as ΔV_{FB} per unit dose, this data is obtained from the slope of the best fit straight line as in Figure 2.

Experimental Results

Field Dependence

In Figure 3, ΔV_{FB} vs. applied gate bias is shown for a set of samples with 100Å SiO_2 and 1000Å Si_3N_4 for 5×10^5 Rad (Si) dose. The observed flatband shift shows a strong and complex dependence on both polarity and absolute magnitude of the applied bias. The data in Figure 3 is typical of most samples studied in the following respects: (1) For both positive and negative gate bias, ΔV_{FB} is very nearly bias independent over a range of effective applied field of ± 1-2×10^6 V/cm. In this range, ΔV_{FB} is always negative which indicates that the first moment of the trapped charge in the gate insulators is positive. (2) For effective applied fields smaller in absolute magnitude than 3.5×10^6 V/cm, ΔV_{FB} is smaller for positive gate bias compared to negative gate bias. (3) For high effective applied fields exceeding 2×10^6 V/cm in absolute magnitude, ΔV_{FB} is a strong function of the applied bias.

Negative Gate Bias, Low Field

In Figure 4, ΔV_{FB} data is shown for a number of MNOS capacitors which have the same oxide thickness (t_{ox} = 100Å) but different nitride thickness (t_N = 200-2000Å). Samples 12R-3 were all fabricated

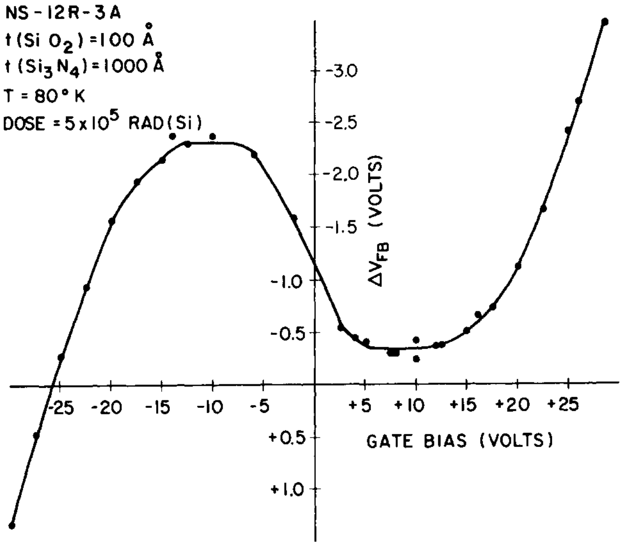

Fig. 3. Dependence of ΔV_{FB} on gate bias. ΔV_{FB} is approximately independent of gate bias over two narrow ranges in bias from -6 to -12 volts, and +6 to +12 volts.

from a single wafer after oxide/nitride growth by etching back the nitride. Consequently, these samples have essentially identical oxide, nitride, and interface layers. The oxide for sample 12R-4 was grown simultaneously with 12R-3 but had a thicker nitride deposition. Each sample was irradiated at an effective applied field of approximately -1.5×10^6 V/cm, or in the negative bias "plateau" region of Figure 3 where ΔV_{FB} is nearly independent of applied bias. The results are plotted in Figure 4 as ΔV_{FB} per 1×10^5 Rad (Si) vs total effective gate insulator thickness.

The data in Figure 4 shows a very good fit to a straight line (curve 4(b)), indicating that ΔV_{FB} is linearly proportional to nitride thickness. This is the expected dependence for no (net) charge trapping in the nitride (Eq. (2)). Fig. 4(a) is calculated from Eq. (1) for an electron-hole pair yield of 0.85 at the oxide field of 1.5×10^6 V/cm.

Flatband shift data for samples with different oxide thicknesses (t_{ox} = 85-600Å) but the same nominal nitride thickness (t_N = 1000Å) is shown in Figure 5. Each sample was irradiated at approximately -1.5×10^6 V/cm effective applied field, the same bias condition as the data in Figure 4. Results for samples 9-1 to 9-4 are the most comparable because the oxides in these samples were grown sequentially under identical conditions (except for growth time) and the samples had the same nitride and aluminum depositions. The two samples designated by the open triangles in Figure 5 received the additional high temperature processing. It appears that this processing may have affected the flatband shift of sample 5-4 slightly, although 6-1 does not appear affected.

The data in Figure 5 shows a strong dependence on the oxide thickness which goes approximately as $\Delta V_{FB} \propto t_{ox}^2$. For comparison, curve 5(a) shows the flatband shift calculated from Eq. (1) for an electron-hole pair yield of 0.85. For all thin oxide samples, the magnitude of the observed flatband shift is smaller than predicted by (1). Agreement between experiment and Eq. (1) is reasonable only for the 600Å thick SiO$_2$ sample. For the thinnest oxide samples, the observed shift is about a factor of four smaller than calculated.

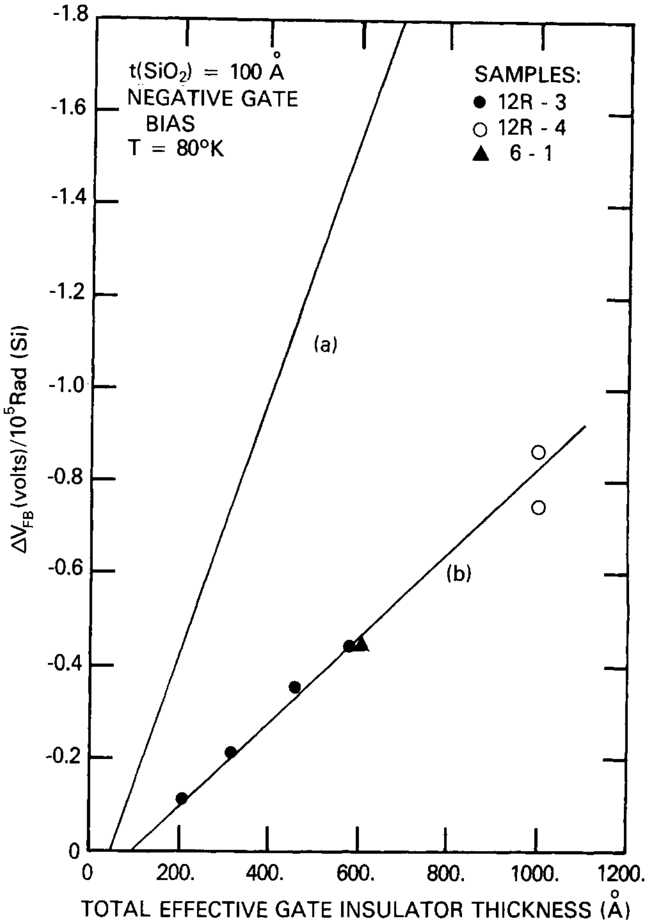

Fig. 4. $\Delta V_{FB}/10^5$ Rad (Si) vs total effective gate insulator thickness (t_{ox} + t_N (eff)). Each sample was irradiated with negative gate bias in the bias independent region. Samples 12R-3 were obtained from a single wafer by etching back the nitride layer. Curve 4(a) is calculated from Eq. (1), and 4(b) is the best fit of a straight line to the data.

Positive Gate Bias, Low Field

In Figure 6, flatband shift data is shown for samples irradiated under positive gate bias with effective applied fields ≅ + 1.5×10^6 V/cm such that the samples are in the nearly bias independent positive bias region of Figure 3. Samples 12R-3 are samples with the same oxide thickness (t_{ox} = 100Å) but different nitride thicknesses made by etching back the nitride. The data for 1×10^6 Rad (Si) dose is shown in Figure 6 plotted as ΔV_{FB} vs total effective gate insulator thickness (t_{ox} plus effective t_N). Where two data points are shown for the same nitride thickness, this indicates the spread in values obtained from one set of samples. The data in Figure 6 do not appear to show any clear dependence of ΔV_{FB} on effective nitride thickness. Sample 12R-4, which nominally received the same processing as 12R-3 except for the nitride deposition, appears to be in particularly poor agreement with the other samples. It is interesting to note that ΔV_{FB} data for the same set of samples irradiated under negative bias show a well-defined, monotonic dependence of ΔV_{FB} on nitride thickness (Fig. 4).

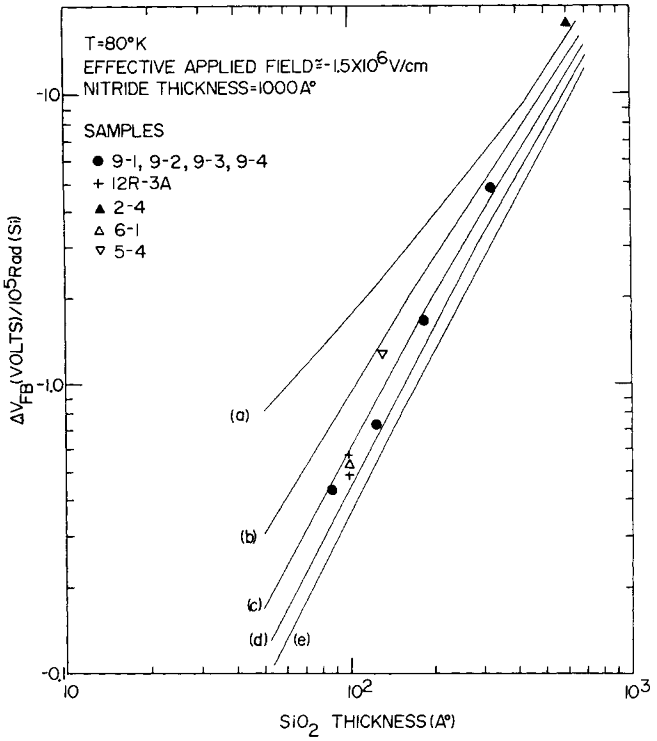

Fig. 5. $\Delta V_{FB}/10^5$ Rad (Si) for different samples with t_N = 1000Å but different oxide thicknesses. Each sample was irradiated with negative gate bias in the bias independent region. Samples with open triangles have received additional 900°C processing. Solid lines are calculated considering only hole generation and trapping in the SiO_2, assuming mean free paths of the holes before capture of (a) zero, (b) 50 Å, (c) 100Å, (d) 150Å, (e) 200Å.

In Figure 7, ΔV_{FB} per 10^6 Rad (Si) vs oxide thickness is shown for samples with the same nominal nitride thickness (1000Å) and varying oxide thicknesses. The samples are irradiated under positive gate bias with an effective applied field ≅ 1.5×10^6 V/cm. In this case ΔV_{FB} increases rapidly with increasing oxide thickness. Data from samples with open symbols in Figure 7, which have received additional 900°C high temperature processing as discussed previously, is not in good agreement with data from the other samples and appears to show that additional high temperature processing significantly degrades the radiation hardness of MNOS devices with ~ 100Å SiO_2 at positive gate bias.

The apparent conclusion from the data in Figures 6 and 7 is that ΔV_{FB} of these MNOS devices for positive gate bias is significantly processing dependent, and depends on some aspect of the processing in a way which is not reproducible. However, ΔV_{FB} for positive gate bias was always observed to be less than for negative gate bias, independent of processing.

High Field Regions

For applied effective fields exceeding ± 2×10^6 V/cm, ΔV_{FB} in all MNOS capacitors studied is a strong function of applied bias as shown in Figure 3. For increasing positive gate bias, ΔV_{FB} is increasingly negative, indicating that more positive charge is being trapped in the gate insulator. For increasing negative gate bias, more negative charge is trapped in the insulator, and for large enough negative bias, the first moment of the trapped charge is negative. There is no sign of saturation in this high field effect for either polarity of gate bias up to effective applied fields of ± 5×10^6 V/cm.

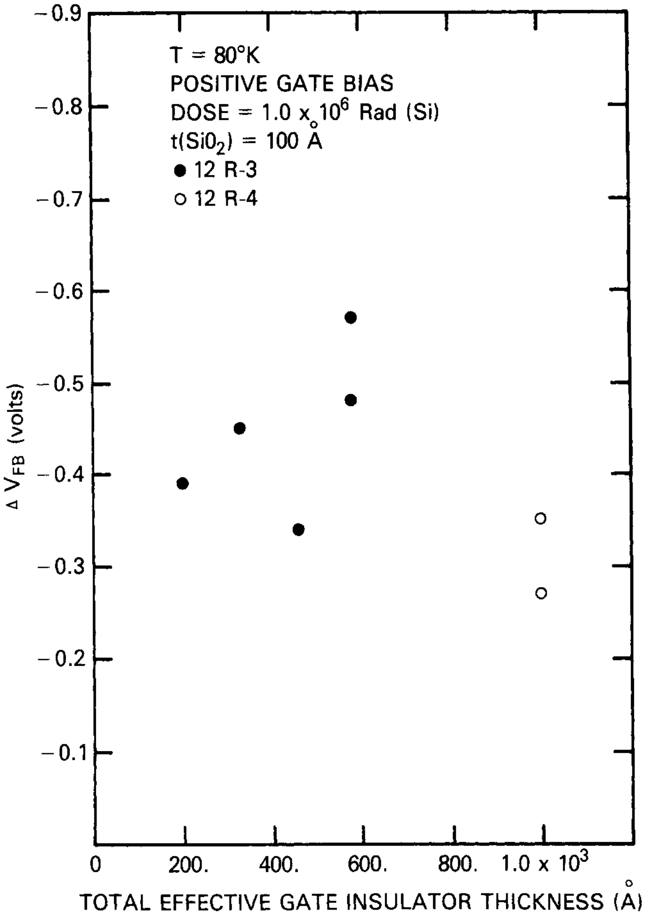

Fig. 6. ΔV_{FB} for samples irradiated to 10^6 Rad (Si) vs total effective gate insulator thickness (t_{ox} plus t_N (eff)). Samples have 100Å SiO_2 but different nitride thickness. Samples are irradiated with positive gate bias in the bias independent region. ΔV_{FB} shows no clear dependence on nitride thickness.

In Figure 3, the high field flatband shifts of the MNOS capacitors appear nearly symmetric for positive and negative gate bias. In order to test this possible symmetry, that part of the flatband shift $\Delta(\Delta V_{FB})$ due to the high field effect is here defined as the deviation of ΔV_{FB} from its value in the bias insensitive region at $1\text{-}2 \times 10^6$ V/cm applied effective field. From $\Delta(\Delta V_{FB})$, the charge trapped in the gate insulator is calculated assuming it is located at the oxide-nitride interface. The results are plotted in Figure 8 for samples 12R-3 and 12R-4 (t_{ox} = 100Å, t_N = 200-2000Å) as the absolute value of the trapped charge vs effective applied field in the insulator. The data in Figure 8 indicates that: (1) the high field flatband shifts are very nearly equal in magnitude but opposite in sign for oppositive polarity of gate bias, (2) the trapped charge appears approximately independent of nitride thickness for a very wide range of nitride thicknesses, and (3) all samples appear to conform reasonably well to a single curve of field dependence [except for sample 12R-3D (t_N = 200Å) for positive gate bias only].

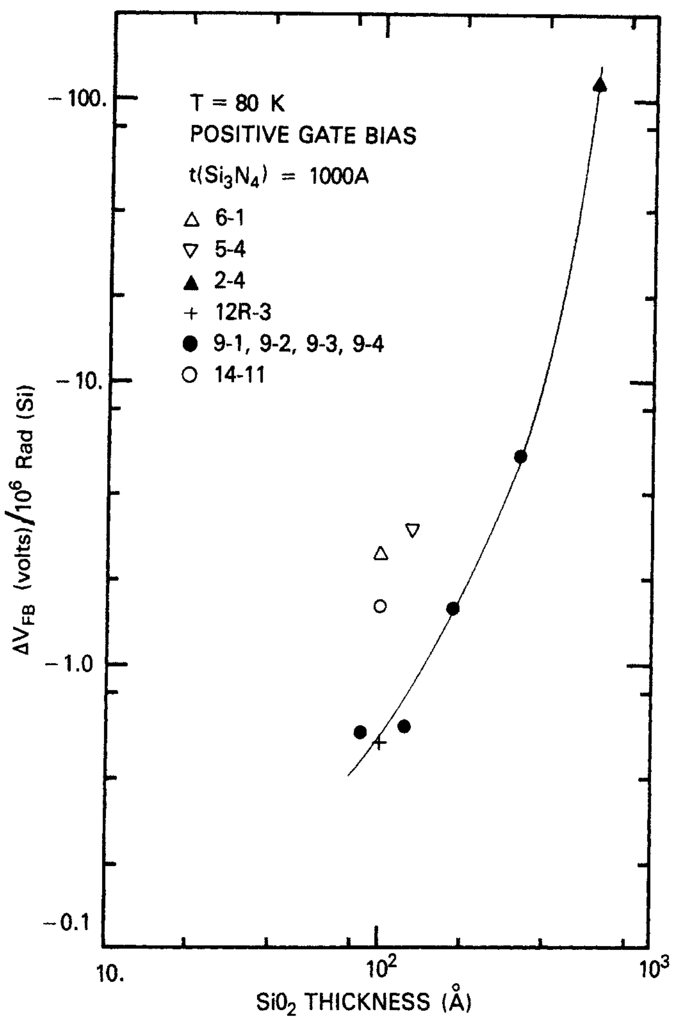

Fig. 7. $\Delta V_{FB}/10^6$ Rad (Si) for samples with t_N=1000Å and different oxide thicknesses. Samples are irradiated with positive gate bias in the bias independent region. Samples marked by open symbols have received additional 900°C processing and show that ΔV_{FB} is significantly processing dependent.

Discussion

The data just presented is, in a very general sense, in agreement with previously published data obtained at 300°K. Perkins et al observed that the radiation sensitivity of their MNOS capacitors increased with increasing oxide thickness and that ΔV_{FB} was smaller for positive gate bias compared to negative gate bias.[2] Recent data of Cricchi et al shows $\Delta V_{FB} \approx -0.5$ V/10^5 Rad for an MNOS transistor with 100Å SiO_2, 1000Å Si_3N_4 at -12V gate bias, very similar to the magnitude of ΔV_{FB} in this work for those conditions. Furthermore, their data appears to show the onset of a high field effect very similar to that discussed in this work.[13]

Negative Gate Bias, Low Field

Data from the negative gate bias, low effective field (1-2x10^6 V/cm) region appears to be very reproducible for different MNOS sample runs with the same processing sequence, and is only slightly affected by the high temperature processing. From samples with t_{ox} = 100Å but different nitride thicknesses, ΔV_{FB} shows a very good fit to linear dependence on nitride thickness (Figure 4). This dependence is a consequence of the MNOS geometry: for $t_{ox} \ll t_N$, the MNOS gate insulator capacitance (C_{ox}) will be inversely proportional to the nitride thickness, and ΔV_{FB} is inversely proportional to C_{ox}.

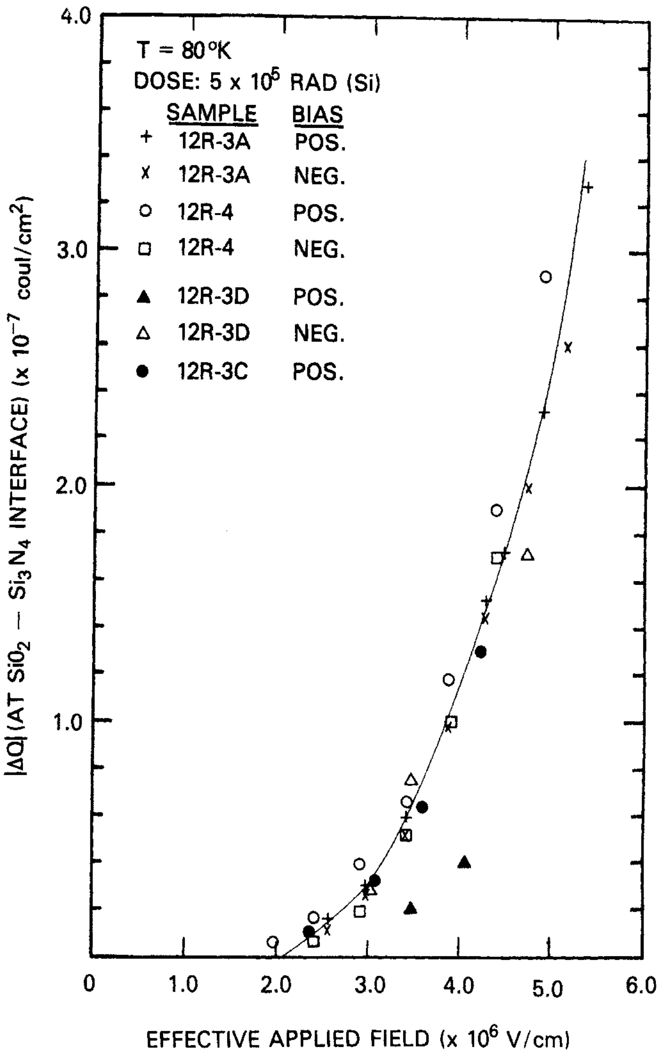

Fig. 8. Summary of high field ΔV_{FB} data for samples with t_{ox} = 100Å and different nitride thickness.

Electron-hole pairs generated by ionizing radiation in the nitride may recombine before being separated by the applied field as discussed previously. However, those carriers which escape recombination will drift in opposite directions due to the applied field. For negative gate bias, electrons will drift towards the SiO_2, and holes towards the gate. Both electrons and holes may be trapped in the bulk of the nitride or may be transported to the SiO_2-Si_3N_4 interface and gate, respectively. The electrons will most likely not have enough energy to cross the potential energy barrier at the SiO_2-Si_3N_4 interface (Figure 1) and should be trapped at the interface where, from MNOS memory experiments, many deep electron traps are known to exist. Holes in silicon nitride are believed to have higher mobility than electrons and so the holes may move through the nitride with relative ease.[14,15] However, it is not known if these results can be applied to hole mobility in nitride at 80°K. The result of generation of electron-hole pairs in the silicon nitride due to ionizing radiation would most likely appear to be net negative charge in the nitride, trapped either throughout the bulk of the nitride or at the oxide-nitride interface. This would result in a contribution to the flatband shift which is positive (but opposite to the observed negative shift), and proportional to the square of the nitride thickness[13] (rather than the observed linear dependence shown very clearly in Figure 4). Consequently, the simplest model which fits the observed dependence of ΔV_{FB} on nitride thickness is that there is no net charge trapping in the nitride under low field negative gate bias conditions and that carriers generated in the nitride are quickly recombined before separation by the applied field.

The data in Figure 5, ΔV_{FB} for samples with fixed nitride thickness and different oxide thickness, shows ΔV_{FB} varying approximately as the square of the oxide thickness for $t_{ox} < t_N$. Considering generation in the SiO_2, generated electrons are mobile in SiO_2 at 80°K, and due to the negative bias are rapidly swept out of the SiO_2 into the silicon substrate when they cannot contribute to ΔV_{FB}.[6] Holes are relatively immobile and are trapped at or near the point of creation at 80°K.[5,7] Assuming trapping of the holes at the point of creation, and 85% separation of the electron-hole pairs at the experimental applied field in the SiO_2 of -1.5×10^6 V/cm,[9] curves 4(a) and 5(a) show the expected dependence of ΔV_{FB} on nitride and oxide thickness, respectively, as calculated from Equation (1). For most MNOS capacitors, the magnitude of the experimental flatband shift is much smaller than calculated. It is possible that net negative charge generated and trapped in the nitride results in a smaller ΔV_{FB} by partially compensating the positively charged trapped holes. This appears unlikely, however, because as discussed previously the data in Figure 4 indicates no net charge generation mechanism in the nitride.

Another possible explanation for ΔV_{FB} being smaller than calculated is that the holes may move a short distance in the oxide before being trapped. Based on data which show slightly different flatband shifts for positively and negatively biased MOS capacitors with ~1000Å SiO_2 gate oxides, Boesch and McGarrity have proposed that holes in SiO_2 have an average transport distance of 85Å.[9] They suggest that this is caused by transport of the holes in extended states of the valence band before being trapped. For MNOS capacitors with oxides on the order of 100Å, many of the holes created in the SiO_2 by the radiation may reach the SiO_2-Si_3N_4 interface before being trapped. Since there is no potential energy barrier to holes crossing this interface (Figure 1), these holes may drift through the interface and the nitride (where they appear to have relatively high mobility at 300°K) without being trapped.[14,15]

In this work, it is assumed that the motion of radiation generated holes in the SiO_2 at applied fields of $\pm$ 1-2$\times10^6$ V/cm are characterized by a probability of being trapped which is constant per unit distance traveled in the SiO_2 and a pair creation efficiency of 0.85.[9] Furthermore, it is assumed that once a hole created in the SiO_2 reaches either interface, no trapping of the hole occurs at either interface or in the nitride. Very likely this last assumption is somewhat unrealistic, and is chosen only to provide the simplest possible model. Curves 5(a) through 5(e) were calculated for this model assuming a mean free path $\overline{\Delta X}$ from zero to 200Å in 50Å steps. The data forms a reasonable fit to the model for $\overline{\Delta X} = 125 \pm 25$Å, where $\pm$ 25Å represents the scatter in the data. The fact that $\overline{\Delta X} \simeq 125$Å is somewhat longer than the mean free path measured by Boesch and McGarrity may be explained by two effects: (1) ΔV_{FB} in this work is measured after longer times (~3×10^2 sec) compared to ~10^{-3} sec in ref. [9]. Because ΔV_{FB} anneals in time, the average hole transport distance is time dependent and increases with time. (2) ΔV_{FB} is measured at higher doses in this work. ΔV_{FB} is found to be slightly sublinear with dose in these MNOS samples, perhaps due to filling of trapping states, which implies that the hole transport distance increases as the number of empty traps decreases.

Positive Gate Bias, Low Field

For positive gate bias the ΔV_{FB} data for these MNOS capacitors is more difficult to interpret. Holes generated in the SiO_2 drift towards the silicon substrate under the influence of the positive gate bias, while electrons transport through the SiO_2 to the oxide-nitride interface and the nitride. It is known from MNOS memory effect measurements that electrons may be (permanently) trapped both at the interface and in the bulk of the nitride. In this case, it is believed that electrons created by radiation will be subject to the same trapping processes as electrons injected by a high electric field from the silicon substrate. By analogy with the MNOS memory effect, it is assumed that the centroid of trapped electrons is near the oxide-nitride interface.[16]

The smaller flatband shift observed for positive gate bias compared to negative gate bias is consequently believed to be due to the negatively charged trapped electrons near the oxide-nitride interface which compensate the effect of the holes trapped in the SiO_2. Presumably holes generated in the SiO_2 move the same ~125Å mean free path before being trapped independent of the polarity of the gate bias. From the negative bias data, for 100Å SiO_2 only about 25% of the holes generated in the SiO_2 are trapped. All MNOS samples irradiated under positive bias show a negative flatband shift. Consequently, if the centroid of trapped electrons is near the oxide-nitride interface, only about 25% of the electrons generated in the oxide are trapped for 100Å SiO_2 MNOS devices, with ~75% of the electrons either being trapped much deeper in the nitride or passing through the nitride altogether.

For negative gate bias, where only the trapping of holes was considered, ΔV_{FB} was observed to be only weakly (if at all) dependent on 900°C high temperature processing after deposition of the oxide/nitride layers. However, the ΔV_{FB} data in Figure 7 show that the radiation tolerance of the MNOS capacitors may degrade by as much as a factor of 4 when subjected to 900°C processing. This implies that it is the trapping of electrons which is affected, and that the processing reduces the electron trapping, perhaps by annealing of the electron traps at the oxide-nitride interface. This effect is similar to an effect observed in MNOS memory transistors, where the memory "window" decreases if the MNOS structure receives any high temperature processing after the oxide/nitride deposition.[17]

It is also believed that the processing dependence of the electron trapping may account for the lack of a monotonic dependence of ΔV_{FB} on nitride thickness as shown in Figure 6 for positive gate bias. It appears that the electron trapping depends on nitride deposition parameters and perhaps other processing steps in a way which is not reproducible for different sample processing runs.

High Field Regions

In the previous discussion of low field ΔV_{FB} data, it has been possible to model all experimental results based only on generation of free carriers in the SiO_2 and their subsequent transport and trapping. However, explaining the high field data (including data such as the fact that for very large negative gate bias the first moment of the trapped charge is negative), appears to require a different generation mechanism. Possible generation mechanisms include free carrier injection from either the gate or the silicon substrate into the gate insulators due to a combination of the radiation and high field, and free carrier generation in the nitride, where separation of the carriers rather than recombination might occur for high applied fields. These models all appear to be in conflict with some of the experimental data. For example, considering high field generation in the nitride, the total charge generated due to irradiation should be proportional to the nitride thickness, if either type of carrier is relatively mobile in the nitride, as previous data suggests. This is contrary to the experimental data in Figure 8 where total trapped charge is independent of nitride thickness for a factor of 10 variation in t_N. Likewise, for carrier injection over potential energy barriers, it is difficult to explain the symmetry of the ΔV_{FB} shifts for positive and negative bias. (However, the apparent high field symmetry may itself be incorrect because the assumption that the high field effect can be considered a deviation from the low field shift is questionable. Recent data by Sour and Chiu on pure SiO_2 MOS capacitors irradiated at 77°K indicates that at applied fields in the SiO_2 at greater than 3x10^6 V/cm, holes move an increasingly longer distance before being trapped.[18])

Conclusions

For applied effective fields less than 2x10^6 V/cm, the flatband shift in MNOS capacitors irradiated at 80°K may be explained by considering only generation of free carriers in the SiO_2 and their subsequent trapping after transport due to the applied field. Lack of net free carrier generation in the nitride, which is the thickest part of the gate insulator in the ideal MNOS radiation hard structure, accounts for the radiation hardness of the device. By making the thickness of the SiO_2 layer sufficiently thin (yet thick enough to exclude the MNOS memory effect, or $t_{ox} \gtrsim 50$Å), the MNOS structure shows improvement in radiation hardness at 80°K by one to two orders of magnitude depending on applied bias when compared with pure SiO_2 MOS devices. Consequently, the MNOS gate insulator shows considerable promise for use in radiation hard MOS devices if it can be shown that the MNOS structure can be fabricated with insulator properties, such as fixed charge density and fast surface state density, compatible with actual device requirements.

References

1. A.G. Stanley, "Comparison of MOS and MNS IGFET's under Electron Irradiation," IEEE Trans. Nucl. Sci. NS-13, p. 248, Dec (1966).
2. C.W. Perkins, K.G. Aubuchon, and H.G. Dill, "Radiation Effects and Electrical Stability of MNOS Structures," Appl Phys Letts. 12, p. 385 (1968).
3. P.A. Newman and H.A.R. Wegener, "Effect of Electron Radiation on Silicon Nitride IGFET's," IEEE Trans. Nucl. Sci. NS-14, p. 293 Dec (1967).
4. For a review, see J.T. Milek, Handbook of Electronic Materials, V. 6 "Silicon Nitride for Microelectronic Applications," Plenum Publishing, c. 1972, pp. 87-98.
5. H.H. Sander and B.L. Gregory, "Unified Model of Damage Annealing in CMOS, from Freeze-In to Transient Annealing," IEEE Trans. Nucl. Sci. NS-22, p. 2157 Dec (1975).
6. R.C. Hughes, "Hole Mobility and Transport in Thin SiO_2 Films," Appl. Phys. Letts. 26, p. 436 (1975).
7. R.C. Hughes, E.P. EerNisse, and H.J. Stein, "Hole Transport in MOS Oxides," IEEE Trans. Nucl. Sci. NS-22, p. 2227 Dec (1975).
8. J.J. Chang, "Theory of MNOS Memory Transistor," IEEE Trans. Elec. Dev. ED-24, p. 511 May (1977).
9. H.E. Boesch, and J.M. McGarrity, "Charge Yield and Dose Effects in MOS Capacitors at 80°K," IEEE Trans. Nucl. Sci. NS-23, p. 1520, Dec (1976).
10. P.F. Schmidt, M.J. Rand, J.P. Mitchell, and J.D. Ashner, "Radiation Insensitive Silicon Oxynitride Films for use in Silicon Devices," IEEE Trans. Nucl. Sci. NS-16, p. 211, Dec (1969).
11. T.P. Ma, B.H. Yun, D.J. DiMaria, and G.A. Scoggan, "Effects of Electron Beam Irradiation on the Properties of CVD Si_3N_4 Films in MNOS Structures," J. Appl. Phys. 47, p. 1599 Apr (1976).
12. E. Nicollian and A. Goetzberger, BSTJ 46, p. 1055, July-Aug (1967).
13. J.R. Cricchi, M.D. Fitzpatrick, F.C. Blaha, and B.T. Ahlport, "Hardened MNOS/SOS Electrically Reprogrammable Non Volatile Memory," IEEE Trans. Nucl. Sci. NS-24, p. 2185, Dec (1977).
14. B.H. Yun, "Electron and Hole Transport in CVD Si_3N_4 Films," Appl. Phys. Letts. 27, p. 256 Aug (1975).
15. Z.A. Weinberg, "Hole Conduction in Si_3N_4 Films on Si," Appl. Phys. Letts. 29, p. 617 Nov (1976).
16. B.H. Yun, "Measurements of Charge Propagation in Si_3N_4 Films," Appl. Phys. Letts. 25, p. 340, Sept (1974).
17. P.R. Reid, private communciation.
18. J.R. Srour and K.Y. Chiu, "Mos Hardening Approaches for Low Temperature Applications," IEEE Trans. Nucl. Sci. NS-24, p. 2140 Dec (1977).