Retarded oxidation of Si nanowires

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Retarded thermal oxidation of Si nanowires is investigated. The oxidation behavior strongly depends on the wire curvature. The effect starts to evolve for a curvature larger than 0.05 nm, i.e., an original nanowire radius of 35 nm. For longer oxidation time and lower oxidation temperature, the effect of retarded oxidation gets stronger. The average values of the oxidation rate for small wires are reduced nearly by a factor of 2 compared to bulk ⟨100⟩ silicon. The authors suggest that the increased stress is responsible for the mechanism of retarded oxidation which cannot be decreased by the viscous flow of the oxide. © *2006 American Institute of Physics*.
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Semiconductor nanowires have received increasing attention during the last years because of their possible application for new kinds of nanoscale devices.[1,2] Compared to nanowires from III-V or II-VI semiconductors, such as GaAs (Ref. 3) or ZnO,[4,5] Si nanowires (Si NWs) have the advantage of being compatible with today's technology for silicon integrated circuits. In addition, Si NWs are still an interesting and promising system for investigating phenomena associated with quantum size effects based on indirect semiconductor nanostructures.

Two basic mechanisms are currently mostly used for the growth of Si NWs. The first, the vapor-liquid-solid (VLS) process,[6] uses (nanosized) liquid metal droplets on the substrate. The vapor phase semiconductor supplied, e.g., silane (SiH_4) or silicon tetrachloride ($SiCl_4$), is absorbed by the liquid droplet, and continuous supply of the vapor-phase semiconductor precursor results in supersaturation and, consequently, the nanowire growth. The second mechanism is called the oxide-assisted growth[7] and is based on the thermal evaporation of silicon monoxide (SiO) or a mixture of silicon and silicon dioxide. A combination of both, using a metal catalyst in combination with the oxide-assisted growth, was called silicon monoxide vapor-liquid-solid (SiO-VLS), and combines the position control by the metal catalyst with the simple growth mechanism based on SiO powder.[8]

For very thin Si NWs having a diameter below 5 nm, as well as for microelectronic applications, the growth and investigation of an oxide shell around such wires are of great importance. Up to now, very little is known on the thermal oxidation of structures having a large curvature such as in the case of nanowires. Since the Deal-Grove model only considers planar bulk Si, some changes have to be made for cylindrical structures as described in detail for wet oxidation elsewhere.[9] Earlier investigations suggest that a retarded oxidation of the Si due to the development of a stress field during the oxidation process plays a role.[10] Here, we will report on the controlled thermal oxidation of Si NWs as a function of the nanowire radius and discuss the results in comparison to the oxidation behavior of bulk crystalline Si.

The (nominally undoped) Si/SiO_2 core-shell nanowires were grown via the SiO-VLS mechanism for 1 h in a tube furnace at a temperature of 875 °C using a constant nitrogen flow of 50 sccm (cubic centimeter per minute at STP) and a constant nitrogen pressure of 25 mbars as described earlier.[8] Since it is not possible to distinguish between the original SiO_2 shell oxide and the later grown artificial oxide, we removed the already grown oxide shell of the wires for a controlled starting point via hydrofluoric (HF) acid using 5 wt % HF for 4 min. A piece of a Si ⟨100⟩ wafer also etched was used as a reference sample. This allows to compare the different oxidation behaviors of planar bulk crystalline Si and cylindrically shaped Si NWs. Please note that the crystalline core of the Si NWs (and therefore also the surfaces of the NWs) might have different crystallographic orientations, which depend on the diameter, too.[11]

The samples were oxidized at 925 and 950 °C for 1, 2, 3, 5, and 7 h. N_2 atmosphere (100 sccm, 1000 mbars) was used while heating the furnace to the desired temperature to avoid any preoxidation during heating. Then, the atmosphere was switched to 100 sccm O_2. After completing the oxidation time, the gas flow was switched back to N_2.

The oxidized NWs and oxidized planar Si wafer pieces were investigated by transmission electron microscopy (TEM). The nanowires were removed from the substrate with a scalpel and dispersed into a few droplets of methanol. Then, a TEM grid with a carbon film on a copper net was pulled through the solution. A TEM cross section sample was prepared in case of the planar Si reference. All TEM images were then analyzed in terms of diameter of the Si core and thickness of the oxide or oxide shell.

Examples for the resulting core-shell structure of the Si/SiO_2 NWs are shown in the TEM images (Fig. 1). The image on the left shows a rather thick wire (106 nm, core: 40 nm), while the wire on the right image represents a smaller diameter (78 nm, core: 26 nm).

For the temperature of 925 °C and times of 1, 2, and 3 h, the results of the oxidation process of both Si nanowires and a planar bulk Si ⟨100⟩ reference sample are presented in Fig. 2. To follow the oxidation process and to interpret the data in terms of the original Si NW diameter, the relationship between the Si (core) radius and the oxide (shell) thickness is

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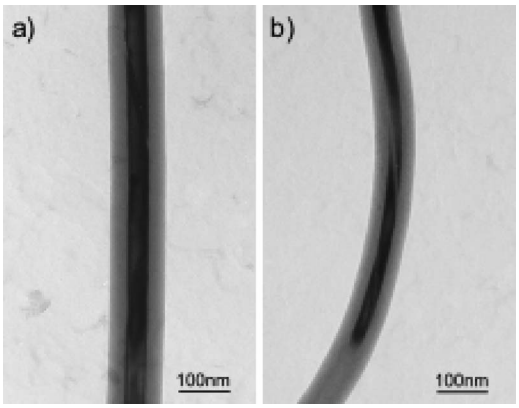

FIG. 1. TEM image of silicon nanowires after oxidation for 1 h at 925 °C. The darker inner part shows the silicon core which is 40 nm (a) and 26 nm (b) in diameter. The outer shell consists of silicon dioxide and is 33 nm (a) and 26 nm (b) thick.

displayed as a black curve in the background. During the oxidation process, the NW radii would follow these lines, starting with the original radius (intersection of the black curve with the x axis). With increasing oxidation, the initial radius gets smaller and the oxide thickness increases. So the black curves need to be followed from their intersection with the x axis until the initial Si is completely transferred to the oxide (intersection with the y axis). This relationship can be estimated by assuming that 1 mol of Si is transformed into 1 mol of SiO_2, and by taking into account the different atomic and molecular volumes of Si and SiO_2. Since the atomic volume of Si (Ω_{Si}) is with 20 Å^3 much smaller than that of SiO_2 ($\Omega_{SiO_2} \sim 45$ Å^3),[10] the overall thickness of the wires increases during the oxidation process. The correlation between the Si NW starting radius without any oxide $r_{NW,0}$, the remaining silicon core radius r_{Si}, and the thickness of the SiO_2 shell r_{ox} is estimated via Eq. (1) under conditions of volume conservation:

$$r_{ox} = -r_{Si} + \sqrt{\left(1 - \frac{\Omega_{SiO_2}}{\Omega_{Si}}\right) r_{si}^2 + \frac{\Omega_{SiO_2}}{\Omega_{Si}} r_{NW,0}^2}. \quad (1)$$

Comparing the oxidation of the planar Si and the NWs (Fig. 2), it was found that for NWs of a radius of 44 nm or more, the oxide thickness reaches the value observed for planar Si. With increasing Si core radius, the thickness of the oxide shell increases as well. However, the longer the oxidation time and the smaller the original wire diameter, the more the oxide shell *deviates* from the values of the planar Si.

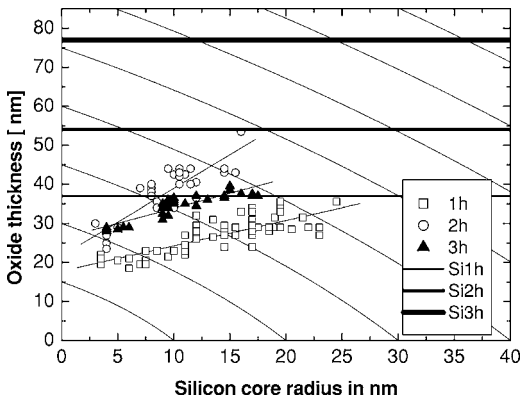

FIG. 2. Dependency of the oxide thickness from the remaining silicon core radius at 925 °C for 1, 2, and 3 h. The straight lines represent the bulk Si references. The black curves indicate the starting radii.

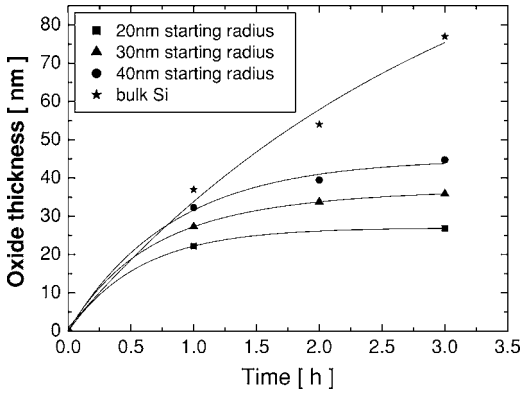

FIG. 3. Dependency of the oxide thickness from the oxidation time for different nanowire starting radii in comparison to bulk Si at 925 °C.

Please note here that we do find completely oxidized nanowires for longer oxidation times and higher temperatures. TEM investigations revealed that some, mostly the thicker nanowires, show a core-shell structure, while the thinner ones oxidize totally. Obviously the temperature (925 °C) used and a time of 1 h were enough to completely oxidize wires below a starting radius of 15 nm.

In Fig. 3, the dependency of the oxide shell thickness on the oxidation time is displayed. The data are obtained from Fig. 2 by taking the intersection between the linear fit of the oxidation data for each oxidation time and temperature, and the curves connecting the silicon core radius to the oxide shell thickness during the oxidation process. With increasing oxidation time, the thickness of the oxide shell increases, but we do see a retarded oxidation in our experiments which reduces the average oxidation rate with longer oxidation times and smaller starting radii of the nanowires.

The dependence of the oxide shell on the curvature (which is defined as $1/r$) is demonstrated in Fig. 4. With increasing curvature, as the radius gets smaller, the oxide shell also gets thinner. At higher oxidation temperatures, the oxide shell is thicker for the same value of curvature.

Figure 1 compares the core-shell structure of nanowires with (a) a thick wire having a nearly bulk equivalent behavior and (b) a retarded oxidation behavior of the thinner wires. Although the core is mostly single crystalline, some defects such as stacking faults and twins might occur. It cannot be

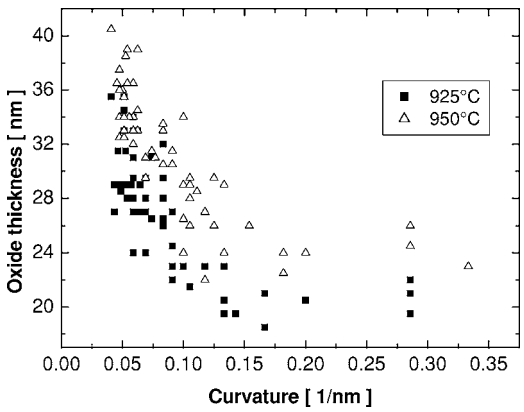

FIG. 4. Dependency of the oxide thickness from the curvature for 1 h oxidation time and two different temperatures.

ruled out, though, that those defects influence the oxidation process, but it will not be the main process.

Figure 2 summarizes a large number of experiments. Our reference (⟨100⟩) Si wafer showed average growth rates of 37 and 27 nm/h for the 1 and 2 h treatments at 925 °C. In comparison, a wire with a 25 nm core radius after oxidation (original core radius around 44 nm) has a growth rate of 34 nm/h, in good agreement with the bulk case. However, wires with a remaining core radius of 5 nm (original core radius around 17 nm) show a drastically reduced rate of 21 nm/h. This effect is even more obvious if going to longer times such as 2 h experiments. The oxidation rate of nanowires involves a balance of increasing stress as the volume expands and decreasing stress by viscous flow of the oxide. At lower temperature, the viscous flow is slow, and self-limiting oxidation is more likely. The fact that we do have a number of completely oxidized wires speaks for a still significant viscous flow at the temperatures used here, and we are planning to repeat the experiments for lower temperatures.

Under the conditions used we do not see a self-limiting oxidation as reported by Liu *et al.*[12] for nanocolumns (diameter: 30 nm, height: 1 μm) fabricated by a combination of electron beam lithography, Cr lift-off, and NF_3 reactive ion etching. Liu *et al.* gave no indication at which pressures and oxygen flow rates the experiments were realized. So, the experiments cannot be compared directly to our results.

As displayed in Fig. 3, the retarded oxidation shows evident diameter dependence. Such a behavior can be understood due to the increasing stress field at the curved Si/SiO_2 interface. When oxidizing planar silicon, a biaxial compressive stress is created at the interface and this leads to bending from a planar surface to a convex surface.[13] A retarded oxidation of the silicon nanowires occurs because of reduced oxygen diffusion and reduced chemical reaction at the interface of the $Si-SiO_2$ due to the viscous stress and the tensile stress in the oxide. The new oxide at the interface pushes the older oxide outwards and faces a resistance from the normal stress perpendicular to the surface, leading to a reduced oxidation reaction.[9] The effect of the viscous flow of thermal SiO_2 for Si wafer was investigated as early as 1977.[14] These old data show quite clearly that a viscous flow should be relevant even at temperatures as low as 925 °C for the long annealing times used here. A characteristic relaxation time, i.e., the time for viscous flow to relax the remaining stress to $1/e$ of their original value, was reported to be in the range of 22 s for 1000 °C and 83 s for 960 °C (dry oxidation). For temperatures above 960 °C, a viscous flow is possible and stress can be relieved. Oxidation of small radii nanowires shows a strongly reduced oxide growth, since the stress at the $Si-SiO_2$ surface is larger because of a more drastic deformation of the oxide having a small radius and a larger curvature. The dependency of the oxide shell on the curvature (as shown in Fig. 4) displays the lower oxide thickness for larger curvature. The oxide shell does not decrease with the curvature in a linear way. There seems to be a saturation point of around 20 nm oxide for a curvature larger than 0.2 nm^{-1}, i.e., a radius smaller than 5 nm, which represents a hint for the value where the retarded oxidation might play a role. Higher temperature seems to shift that to smaller curvature, hence, larger radius.

The large scattering of the data observed in the figures might be caused by an additional dependence of the results from the crystal orientation of the wires, which cannot be evaluated in detail since it is beyond the scope of this letter. It is well known that ⟨100⟩ Si oxidizes slower than ⟨110⟩ and both oxidize slower than a ⟨111⟩ orientation.[10,11,16] With increasing oxidation time, the oxidation is more and more diffusion controlled and the oxidation behavior changes from a linear to a root-time behavior.[15]

Since the Deal-Grove model only considers planar bulk silicon, some changes have to be made for cylindrical structures as described in detail for wet oxidation elsewhere.[16] The mechanism of initial oxide growth, however, cannot be explained with the Deal-Grove model. The initial oxidation rate is much larger than assumed, which might be because during oxidation there is not only oxidant diffusion from the oxide surface to the oxide/silicon interface and the oxidation reaction at the interface, there are also silicon atoms emitted at the interface during the oxidation.[17] However, other theories for initial oxidation are discussed, too.[13]

Silicon nanowires were grown via the VLS mechanism and oxidized artificially at specific temperatures and times. Some nanowires were oxidized completely and others showed a core-shell structure as demonstrated by TEM investigations. The dependence of the oxide thickness on the curvature shows an evidence of a self-limiting oxidation. A retarded oxidation was observed for nanowires due to the increase of stress at the Si/SiO_2 interface for larger curvature. Viscous flow of the oxide can at least partly relax the stress for the conditions used in our experiments. The oxidation of the planar silicon showed the normal square root time behavior, which can be explained roughly by the Deal-Grove theory. The oxide thickness of very thick nanowires approached the thickness of the planar silicon reference at lower oxidation time since the curvature is relatively small.

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