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ADVANCED MATERIALS

Revealing buried interfaces to understand the origins of threshold voltage shifts in organic field-effect transistors

Simon G. J. Mathijssen, Mark-Jan Spijkman, Anne-Marije Andringa, Paul A. van Hal, Iain McCulloch, Martijn Kemerink, René A. J. Janssen, Dago M. de Leeuw

Supporting Information

Field-effect transistors were prepared on heavily doped Si wafers, acting as common gate, covered by 200 nm thermally grown SiO_2 acting as the gate dielectric. Gold source and drain contacts were defined by conventional photolithography. The gate dielectric was passivated by vapour deposited hexamethyldisilazane, HMDS. As semiconductor we now use a perylene derivative (ActivInk^{TM} N1400, Polyera), an air-stable *n*-type semiconductor. The chemical formula is given as inset in Fig. S1. XPS as presented in Figure S1 shows that the perylene is completely removed upon delamination. The N1s peak before exfoliation has two contributions; the peak at 399 eV is attributed to the nitrile group. The contribution at a binding energy of 400.2 eV occurs due to the presence of the imide group.

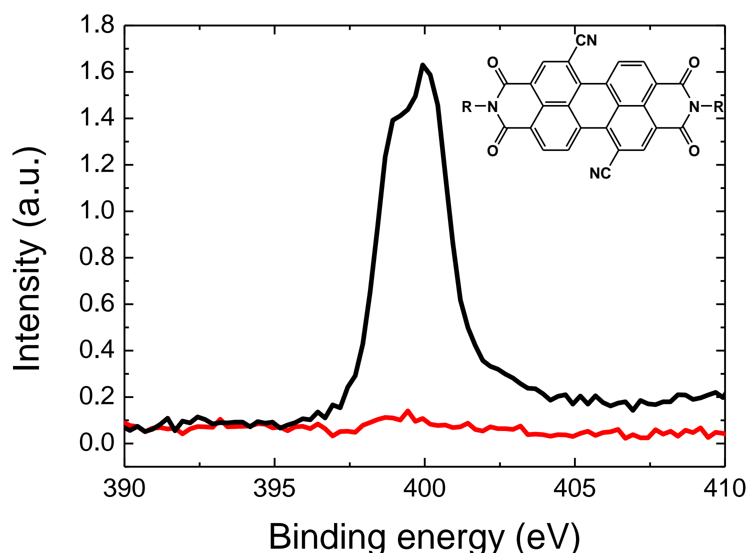

Figure S1: X-ray photoemission spectroscopy before (black) and after (red) perylene exfoliation. After exfoliation the N1s peak is gone, the perylene is completely removed.

Perylene transistors were subjected to a continuous gate bias of 60 V, source and drain electrodes were grounded. Linear transfer characteristics as a function of stress time are presented in Fig. S2a. The transfer curves shift with stress time in the direction of the applied gate bias; in Fig. S2a to the right.

In order to show that the exfoliation procedure can be extended to examine charge transfer across different weakly bound buried interface, the perylene semiconductor is

delaminated at different stages of the stress experiment. Different perylene transistors were stressed for specific periods of time. At the end a transfer curve is measured, the semiconductor is peeled off and the surface potential of the exposed gate dielectric is probed with SKPM with all electrodes grounded. The transfer curves are presented in Fig. S2a with the corresponding surface potentials plotted in Fig. S2b. The non-zero potential originates from the negative interface charges in the gate dielectric. With stress time the surface potential decreases. The magnitude of the surface potential after exfoliation matches to the threshold voltage of the transfer curve before exfoliation, showing that the gate bias stress effect is dominated by charge transfer into the SiO_2 gate dielectric.

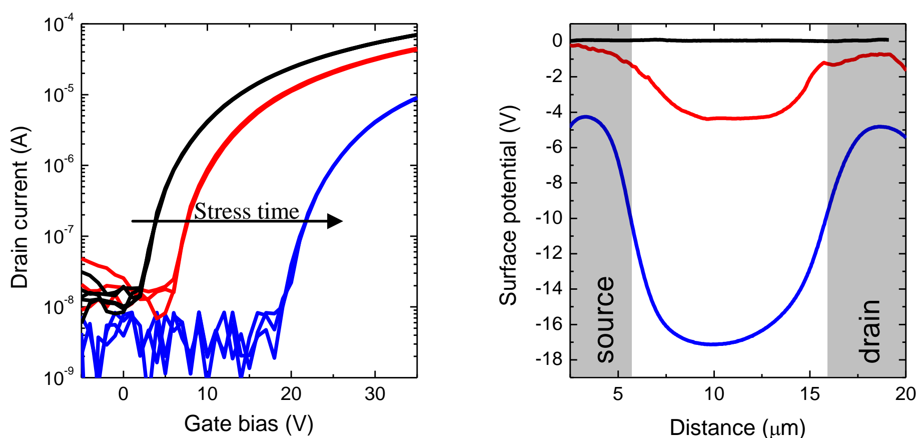

Figure S2. Charge transfer to the gate dielectric. (a) Transfer curves as a function of stress time measured at a drain bias of 5 V. The gate bias during stress was 60 V. The curves shift to positive voltage. (b) Corresponding surface potential profiles after perylene exfoliation. The net surface potential of the negative charges in the dielectric is revealed.