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# Reverse-bias current reduction in low-temperature-annealed silicon *pn* junctions by ultraclean ion-implantation technology

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Reduction in the reverse-bias current in low-temperature-annealed silicon *pn* junctions has been studied. It has been shown that the transition region existing underneath the ion-implantation-generated amorphous layer and the contamination incorporated into this region play a decisive role in determining the reverse current level. In order to minimize the contamination involvement into the transition region, ultraclean ion-implantation technology has been developed. Ion implantation was carried out under a UHV ( $5 \times 10^{-10}$  Torr) condition in order to minimize the recoil implantation of adsorbed contamination at the surface. The contamination due to the high-energy ion-beam sputtering of component parts in the ion implanter has also been suppressed. As a result, a low reverse-bias current level of about  $1.2 \times 10^{-7}$  A/cm<sup>2</sup> has been obtained for arsenic-implanted *n<sup>+</sup>p* junctions annealed at 550 °C, which is more than two orders of magnitude smaller than that previously reported. The stress compensation technology employing combined implantation of phosphorus and arsenic has also been shown to be very effective in reducing the lattice strain and in suppressing the damage generation.

## I. INTRODUCTION

Low-temperature processing is one of the most essential requirements in establishing fabrication processes for future ultralarge-scale integration (ULSI). The reduction in thermal budget after ion implantation is particularly important in forming shallow junctions as well as in realizing high-precision control of dopant profiles in ultimately small dimension devices. Furthermore, if the post-implantation annealing temperature is reduced below the melting point of aluminum (660 °C), a large flexibility in the design of process integration will result, allowing us to make more advanced device structures, such as, for instance, self-aligned aluminum gate MOSFETs (metal-oxide-semiconductor field-effect transistors). Such flexibility will further enhance the circuit performance as well as the integration density.

Another important requirement for such ULSI devices is that the noise component in a signal arising from leakage currents or dark currents must be suppressed to a level that is as small as possible. This is because the amount of signal charge associated with switching or memory functions is being continuously decreased according to the scaling down of device dimensions. However, the problem is that the reverse-bias current in ion-implanted *pn* junctions increases drastically when the annealing temperature is reduced to suppress the thermal diffusion of dopants for forming shallow junctions.<sup>1,2</sup> The reverse-bias current level obtained by 600 °C annealing, for instance, is  $\sim 10^{-5}$  A/cm<sup>2</sup>, which is more than four orders of magnitude larger than that obtained at temperatures above 900 °C.

Rapid thermal annealing (RTA) has been very actively studied in the formation of shallow junctions.<sup>3-5</sup> Lower leak-

age current *pn* junctions were obtained by low-temperature annealing at 550 °C followed by RTA at 1050 °C for 10 s.<sup>4</sup> Using such techniques, it is possible to form shallow junctions with low reverse-bias currents. Although the thermal budget after ion implantation is reduced in terms of the temperature times the processing period, the temperature during RTA typically exceeds 900 °C,<sup>5</sup> which is much higher than the melting point of aluminum and high enough to cause various reactions of metals with other materials. Therefore, RTA techniques are not applicable to devices that require real low-temperature processing.

Then, the purpose of this paper is to establish a real low-temperature-annealing technology for ion-implanted *pn* junctions. For this purpose, we have investigated the mechanism of reverse-bias current increase in low-temperature-annealed *pn* junctions. In the first place, the characteristics of arsenic-implanted *pn* junctions annealed at low temperatures are presented. Then, it will be demonstrated that the reverse-bias current can be reduced by releasing the stress in the ion-implanted layer by an employment of the stress compensation technology.<sup>6,7</sup> The transition region existing underneath the ion-implantation-generated amorphous layer will be discussed in terms of the end-of-range defect generation from this region. It will be shown that the defect generation from the transition region is very sensitive to a trace amount of contamination incorporated into this region. In order to minimize such contamination, we have developed an ultraclean ion-implantation technology.<sup>8,9</sup> As a result, more than two orders of magnitude reduction in reverse-bias current has been achieved for arsenic-implanted *n<sup>+</sup>p* junctions annealed at 550 °C.

In Sec. II the ultrahigh-vacuum ion-implantation sys-

tem used for the experiment is described. The experimental conditions are summarized in Sec. III. In Sec. IV the results and discussion on low-temperature annealing, stress compensation, defect generation from transition region, ultraclean ion implantation, and the discussion on the transition region are presented in Secs. IV A–IV D, respectively. Finally, conclusions are given in Sec. V.

## II. ULTRAHIGH-VACUUM ION-IMPLANTATION SYSTEM

In this section the ultrahigh-vacuum ion-implantation system<sup>8,9</sup> developed for this experiment is described. Figure 1 shows the schematic of the end station system with a wafer-handling mechanism. The first (wafer-loading) chamber and the second (wafer-transport) chamber are evacuated by an oil-free turbomolecular pump with a magnetic rotor supporting mechanism, featuring base pressures of  $10^{-7}$  and  $10^{-8}$  Torr, respectively. The implant chamber in which ions are implanted is equipped with a cryogenic pump, featuring a base pressure of  $10^{-10}$  Torr. These chambers as well as almost the entire system are made of an aluminum alloy and the inner surfaces are TiN coated to minimize degassing.

In order to transport wafers in a high vacuum without generating dust particles, we have employed a newly developed electrostatic-chuck wafer-transport system.<sup>10</sup> Wafers are loaded on the electrostatic holding chucks in the first chamber and transferred to the electrostatic transport chuck mounted at the tip of a frog leg, which conveys wafers from the first chamber to the implant chamber. The electrostatic holding chuck in the implant chamber firmly holds wafers in a high vacuum by electrostatic force, thus establishing a good thermal contact between the wafer and the wafer stage as well as the electrical contact of a wafer to the ground.

In order to realize defect-free heavily doped regions, the concept of stress compensation<sup>6,7</sup> is also important. The stress in heavily doped regions arises due to the difference in the ionic radii between dopants and silicon. Perfect crystal device technology<sup>6</sup> was developed by employing simultaneous diffusion of two kinds of impurities having different ionic radii, one larger and the other smaller than that of

silicon, to release the lattice strain. In order to apply this concept to ion implantation to form heavily doped regions, it is necessary to implant dopants with different ionic radii sequentially. Therefore, our system is designed so that six different ion species (As, P, B, Si, Ar, and H) can be sequentially implanted without breaking the vacuum. Furthermore, in order to minimize the contamination from the ion source, an ultraclean gas delivery<sup>11–13</sup> system has been employed for supplying source gases to the ion source.

## III. EXPERIMENT

*p*-type (100) silicon wafers were used as substrates. Arsenic or phosphorus ions were implanted to these wafers at various doses ( $10^{15}$ – $10^{16}$  cm<sup>-2</sup>) and energies (25–120 keV), either through oxide or to bare silicon surfaces. In the following, implantation was performed basically to bare silicon surfaces unless otherwise stated.

The conventional wet chemical processes were utilized for wafer cleaning: 5-min boiling in H<sub>2</sub>SO<sub>4</sub>/H<sub>2</sub>O<sub>2</sub>, ultrapure water rinsing, and HF/H<sub>2</sub>O (1:50) etching for removing native oxides, followed by ultrapure water rinsing and drying by pure nitrogen gas blow. After drying, a silicon wafer was immediately loaded into the load-lock chamber and then transferred into the UHV implantation chamber using an electrostatic-chuck transport system.

As for the experiment of stress compensation, arsenic and phosphorus ions were consecutively implanted to 4–6 Ω cm, *p*-type silicon wafers with (100) orientation at 105 and 50 keV, respectively. This gives the same projected range ( $R_p$ ) of about 600 Å for both elements. Here, the total dose was kept constant at  $6 \times 10^{15}$  cm<sup>-2</sup>. Implanted layers were thermally annealed in the nitrogen gas ambient at 1000 °C for 30 min and then subjected to deactivation anneal at 700 °C up to 124 h to study the carrier deactivation. In order to evaluate the effect of stress compensation on the integrity of diodes, *n*<sup>+</sup>*p* junctions were fabricated as follows: Window patterns of varying sizes were opened in the 0.7-μm-thick field oxide, which was thermally grown at 1000 °C on a 0.4–0.6 Ω cm, *p*-type (100) silicon wafer. Such low-

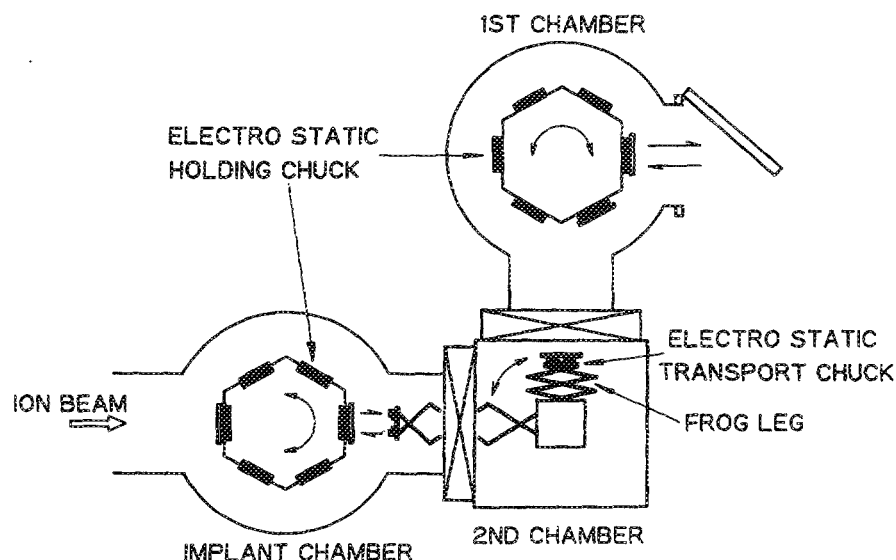


FIG. 1. Schematic of the end-station system of an ultrahigh-vacuum (UHV) ion implanter. Wafers were transported in a high vacuum by a frog leg and an electrostatic wafer chuck.

resistivity substrates were used to suppress the surface inversion effect due to the positive oxide charge without field implantation. After implantation with arsenic and phosphorus, the annealing was performed at 550 °C for 75 min in nitrogen ambient. Contact holes were then opened in the chemical vapor deposition (CVD) oxide of 0.25  $\mu\text{m}$  thickness. Aluminum electrodes were formed with the arsenic-implanted polycrystalline silicon (0.25  $\mu\text{m}$ ) as an intervening barrier layer. The deposition of polycrystalline silicon was carried out employing surface reaction film formation technology<sup>14,15</sup> at below 550 °C for 75 min. Sintering was performed at 400 °C for 20 min in a forming gas ambient. Therefore, the thermal budget after ion implantation was all kept below 550 °C.

For the study of defect generation by cross-sectional transmission electron microscopy, arsenic ions were implanted to 3–8  $\Omega\text{ cm}$ , *p*-type (100) silicon wafers. Typical implant dose and energy were  $1 \times 10^{16}\text{ cm}^{-2}$  and 120 keV, respectively. Implantation was performed either through 100-Å-thick  $\text{SiO}_2$  or into bare silicon surfaces. Implanted samples were thermally annealed in a nitrogen ambient at 1000 °C for 30 min.

In order to investigate the effect of contamination on the integrity of low-temperature-annealed *n*<sup>+</sup>*p* junctions, arsenic implantation was carried out under various background contamination levels. For instance, the base pressure of the ion implant chamber was varied as  $5 \times 10^{-10}$  or  $1 \times 10^{-7}$  Torr. Contamination due to the high-energy ion-beam sputtering of various component parts in the implanter was suppressed by installing a protection apparatus.

The carrier-concentration profiles were obtained by repeating the anodic oxidation and four-point probe measurements. The crystallinity of the ion-implanted layer after annealing was also investigated by reflection electron diffraction analysis.

#### IV. RESULTS AND DISCUSSION

##### A. Low-temperature annealing

Figure 2 demonstrates the carrier-concentration profiles in arsenic-implanted silicon samples that were subjected to annealing for 75 min in a nitrogen ambient at varying temperatures. The horizontal axis shows the depth from the surface, and the vertical axis shows the carrier concentration. The solid line represents the calculated Lindhard-Scharft-Schiott (LSS) impurity profile. As is seen from the figure, the implanted arsenic atoms were activated at high enough concentrations by low-temperature annealing below 700 °C. The maximum carrier concentration of each profile exceeds  $10^{20}\text{ cm}^{-3}$ . Furthermore, no appreciable impurity

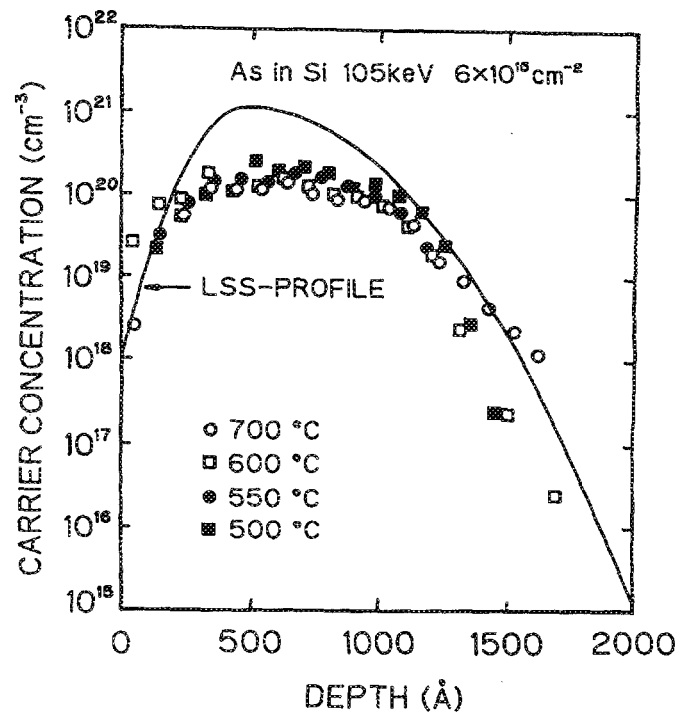


FIG. 2. Measured carrier-concentration profiles in arsenic-implanted silicon subjected to annealing in  $\text{N}_2$  for 75 min at varying temperatures.  $6 \times 10^{15}\text{ cm}^{-2}$  arsenic ions were implanted to silicon at 105 keV. The solid line represents the LSS impurity profile.

diffusion occurs when annealing was done below 600 °C. However, a small amount of diffusion is evidently observed in the sample annealed at 700 °C.

Figure 3 shows reflection electron diffraction patterns obtained from  $6 \times 10^{15}\text{ cm}^{-2}$  arsenic-implanted silicon at 105 keV after annealing for 75 min in nitrogen ambient at varying temperatures. At annealing temperatures greater than 550 °C, the reflection electron diffraction patterns show sharp Kikuchi lines, thus demonstrating that the recrystallization in these samples was completed to the surface. For samples annealed at 500 °C, only a halo pattern is obtained, showing that crystallinity is not restored at the surface, i.e., the solid phase epitaxy was not completed right up to the surface because of the short annealing time of 75 min. A longer annealing time of about 200 min would be required to complete the epitaxy.

Table I summarizes the junction characteristics obtained from  $6 \times 10^{15}\text{ cm}^{-2}$  arsenic-implanted silicon that was subjected to annealing for 75 min in nitrogen ambient at varying temperatures. It is interesting to see that the maximum carrier concentration is increasing with the decrease in

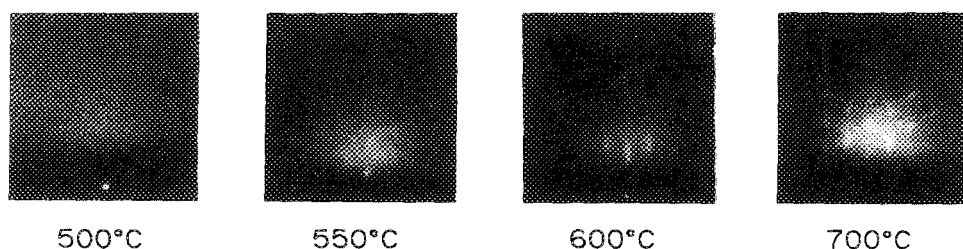


FIG. 3. Reflection electron diffraction patterns from  $6 \times 10^{15}\text{ cm}^{-2}$  arsenic-implanted silicon at 105 keV after annealing for 75 min at varying temperatures.

TABLE I. Characteristics of arsenic-implanted  $n^+p$  junctions annealed at varying temperatures.

Temperature (°C)	Maximum carrier concentration ( $\times 10^{20} \text{ cm}^{-3}$ )	Sheet resistivity ( $\Omega/\square$ )	Junction depth ( $\mu\text{m}$ )
500	2.0	68.0	0.15
550	1.6	70.0	0.15
600	1.5	70.5	0.15
700	1.1	72.0	0.18

the annealing temperature. The sheet resistance is increasing with increasing annealing temperature. It is considered that when the solid phase epitaxy is just completed, relatively high concentration impurity atoms are incorporated into the lattice site and thus electrically activated with a concentration much higher than the thermal equilibrium value. Deactivation appears to have occurred during the annealing period after the completion of regrowth. The deactivation rate depends upon the annealing temperature, and its rate increases at higher temperatures. This accounts for the decrease in the maximum carrier concentration at higher annealing temperatures.

In Fig. 4 the measured reverse-bias current density in arsenic-implanted  $pn$  junctions at a reverse-bias voltage of 5 V is shown as a function of the annealing temperature. Here, the annealing time was 60 min for samples annealed below 900 °C, while at 1000 °C, samples were annealed for 30 min. The reverse-bias current level in the 550 °C annealed  $pn$  junctions formed by using the ultrahigh-vacuum ion-implantation system is  $1.1 \times 10^{-6} \text{ A/cm}^2$ , which is about two orders of magnitude smaller than previously reported data.<sup>1</sup> It

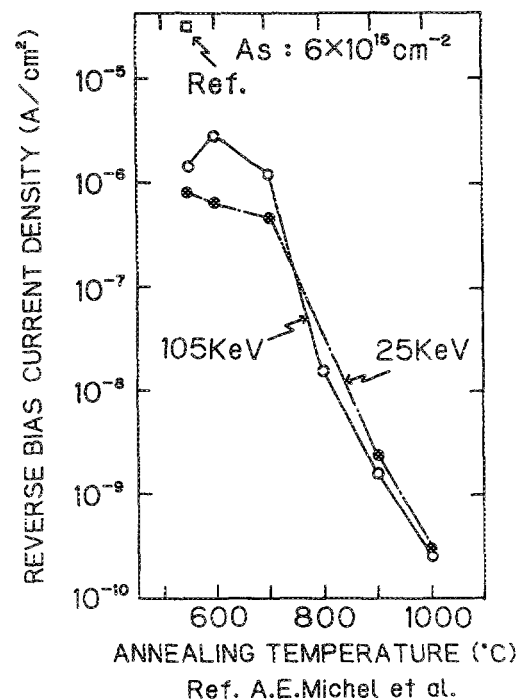


FIG. 4. Reverse-bias current in arsenic-implanted  $n^+p$  junctions measured at 5 V as a function of temperature. The diode size is 1 mm  $\times$  1 mm.

should be noted that the reverse-bias current level in  $pn$  junctions implanted at 25 keV is smaller than that implanted at 105 keV when the annealing temperature is lower than 700 °C. Although the reverse-bias current level in 550 °C annealed samples is reduced as compared to previous data, it is still more than three orders of magnitude larger than that with 1000 °C annealing.

### B. Stress compensation

The effect of stress compensation on the deactivation behavior of dopants is demonstrated in Fig. 5. The abscissa represents the percentage of the phosphorus dose in the total dose of phosphorus and arsenic that is a constant of  $6 \times 10^{15} \text{ cm}^{-2}$ . The ordinate represents the carrier deactivation ratio. Here, the deactivation ratio is defined as the sheet resistivity increase during the deactivation anneal normalized by the pre-deactivation-anneal resistivity by using the following formula:

$$\delta \equiv (1/\rho_1 - 1/\rho_2) / (1/\rho_1) = (\rho_2 - \rho_1) / \rho_2,$$

where  $\rho_1$  is the sheet resistivity of an arsenic-implanted layer after being annealed at 1000 °C for 30 min and  $\rho_2$  is the sheet resistivity after a deactivation anneal performed at 700 °C for 127 h. It is important to note that a local minimum is observed at a phosphorus fraction of about 14%. The occurrence of the local minimum is interpreted in terms of the stress compensation effect.

The residual stress in the regrown layer can be the major driving force for deactivation. In order to reduce the stress in the heavily arsenic-implanted layer arising from a slightly larger ionic radius of arsenic (1.18 Å) (Ref. 16) as compared to that of silicon (1.17 Å),<sup>16</sup> phosphorus atoms having smaller ionic radii (1.10 Å) (Ref. 16) should be simultaneously doped. The ionic radii cited here are those of atoms in tetrahedral covalent bonds. Optimum stress compensation is expected to occur at a phosphorus concentration

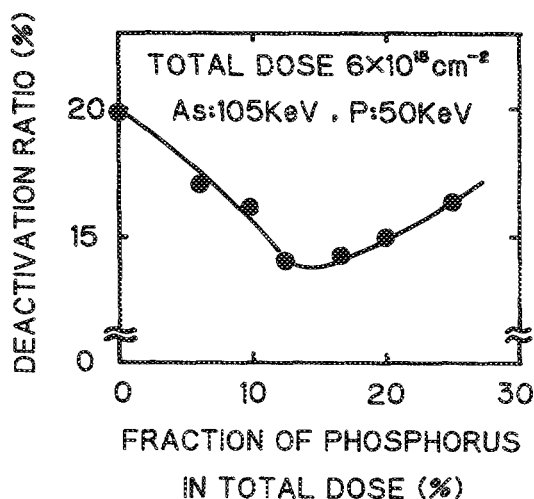


FIG. 5. Carrier deactivation ratio as a function of phosphorus fraction in the total dose. Arsenic and phosphorus ions were consecutively implanted to a total dose of  $6 \times 10^{15} \text{ cm}^{-2}$  with varying dose ratios and annealed at 1000 °C for 30 min. The deactivation ratio is defined as the increase in the sheet resistance during the deactivation anneal of 124 h at 700 °C normalized by the resistance after the deactivation anneal.

where the concentration-weighted average of the arsenic and phosphorus radii becomes equal to that of silicon, which has been calculated to be 12.5% of the phosphorus fraction. This value is nearly equal to the value of 14% at which the local minimum of the deactivation ratio occurs.

In order to examine the effect of stress compensation on the integrity of  $n^+p$  junctions, reverse-bias characteristics were measured. Figure 6 exhibits the measured reverse-bias current at a reverse-bias voltage of 5 V as a function of the phosphorus fraction. The diode size is 1.0 mm  $\times$  1.0 mm and the data distribution within a wafer is also shown by bars indicating the magnitude of standard deviation. It is very interesting to see that the local minimum in the reverse-bias current is observed at a phosphorus fraction of 10%. The minimum reverse-bias current level is about  $6 \times 10^{-7}$  A/cm<sup>2</sup>, which is more than two orders of magnitude smaller than previously reported data.<sup>1</sup> Furthermore, the range of data distribution also becomes smallest at the same phosphorus fraction. The results obtained here suggest that the stress compensation has suppressed the defect generation that determines the magnitude of reverse-bias current level. The phosphorus fractions yielding the local minima in Figs. 5 and 6 are different, and a larger value is obtained in Fig. 5. This is interpreted as follows.

In the experiment of carrier deactivation shown in Fig. 5, 1000 °C annealing was performed on samples after ion implantation, resulting in a substantial diffusion of both phosphorus and arsenic. Since phosphorus diffusivity is much larger than that of arsenic, the ratio of the maximum concentration of phosphorus to that of arsenic decreased. So a higher phosphorus implant dose was needed than expected from simple average calculation. In the case of the experiment shown in Fig. 6, all heat cycles were carried out below 550 °C, and no impurity redistribution by thermal diffusion occurred.

Figure 7 shows the carrier-concentration profiles ob-

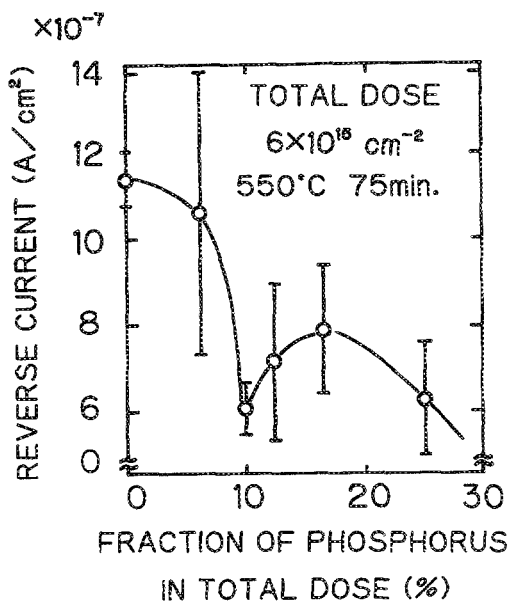


FIG. 6. Reverse-bias current measured at 5 V as a function of phosphorus fraction (0%–30%).

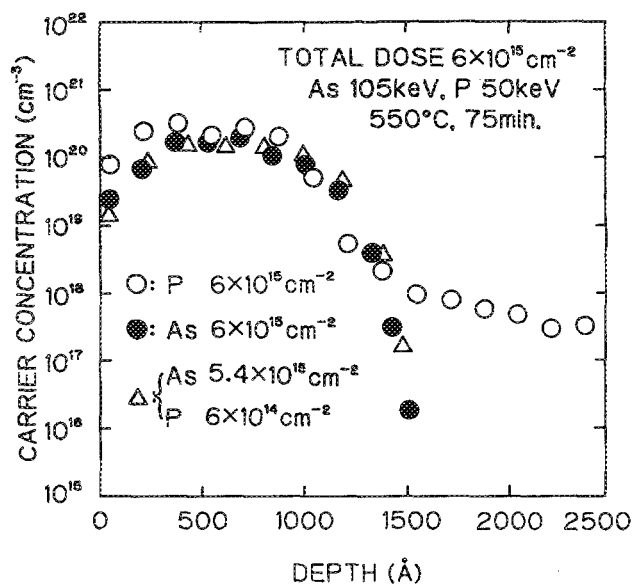


FIG. 7. Measured carrier-concentration profiles for arsenic only, phosphorus only, and arsenic and phosphorus combined implanted samples. Annealing was carried out in N<sub>2</sub> at 550 °C for 75 min.

tained from arsenic and phosphorus combined implantation after annealing in nitrogen at 550 °C for 75 min. No impurity diffusion is observed for arsenic only (●) or 10% phosphorus-implanted samples (Δ), and the junction depth of these samples is about 0.15 μm. However, large diffusion is observed in 100% phosphorus-implanted samples (O), and its junction depth is larger than 0.25 μm although the total impurity dose and the projected range were the same with other samples. Since the phosphorus diffusion in silicon at 550 °C is negligibly small, the substantial diffusion observed here is presumably due to the residual damages existing in the deeper region that would have enhanced the impurity diffusion at such a low temperature. The large difference in the ionic radii of phosphorus and silicon would have generated higher density of residual damages in the 100% phosphorus sample.

Similar enhanced diffusion effect was also pointed out in Fig. 2, where the diffusion of arsenic at 700 °C was evidently observed. Since the diffusivity of arsenic at 700 °C is too small to cause any appreciable diffusion, the observed enhanced diffusion would be due to the residual damage created by arsenic implantation. However, the damage would be much smaller than that caused by phosphorus implantation because the ionic radius of arsenic is much closer to that of silicon than phosphorus. This is why the damage-enhanced diffusion of arsenic was observed only at temperatures above 700 °C, while it was observed at 550 °C for phosphorus.

The phosphorus fraction dependence of the reverse-bias current density is again shown in Fig. 8, where the abscissa scale is expanded to 100%. The samples are the same as in Fig. 6. It is interesting to note the decrease in the reverse current with increasing phosphorus fraction. The reverse-bias current level at a phosphorus fraction of 100% is about  $1 \times 10^{-8}$  A/cm<sup>2</sup>, which is about two orders of magnitude

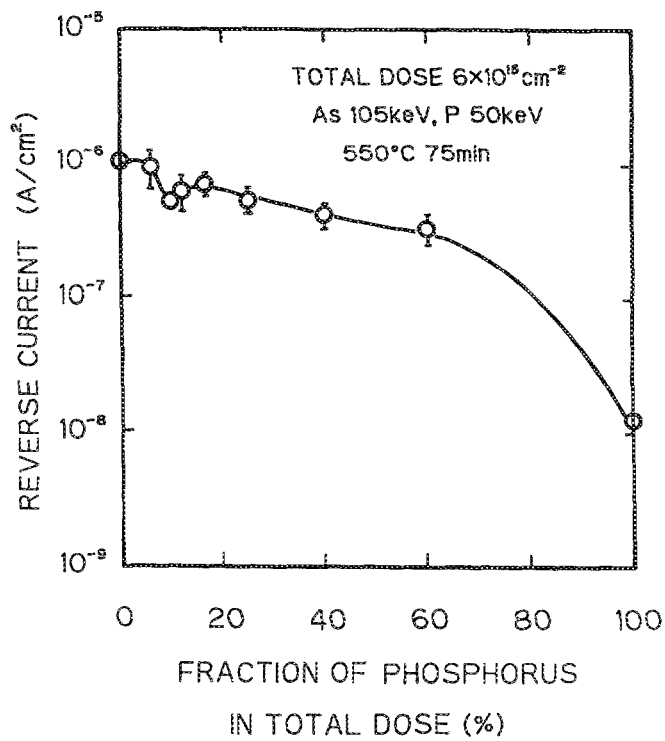


FIG. 8. Reverse-bias current measured at 5 V as a function of phosphorus fraction (0%–100%).

smaller than that of arsenic-only implanted samples. This is explained in the following.

The high density of residual damages due to the phosphorus implantation causes the enhanced diffusion of phosphorus, as discussed in reference to Fig. 7. As a result, these damages are included into the  $n^+$  region, which has expanded by the thermal diffusion of dopants. Since the depletion layer of a reverse-biased  $n^+p$  junction extends only into the lightly doped  $p$  substrate, these defects do not appear in the depletion region and do not contribute to the increase in the generation current, thus reducing the reverse-bias current.

### C. Defect generation from transition region

The stress compensation technology discussed in Sec. IV B contributes to reducing the reverse-bias current by a factor of  $\frac{1}{2}$ . However, the reverse current level is still much higher than that for the 1000 °C anneal. The damage existing in the depletion layer of a reverse-biased  $pn$  junction is the major origin of generation current. Therefore, the study on the damage generation at the ion-implanted layer/substrate interface is most essential to understanding the reason for the large reverse current observed in low-temperature-annealed  $n^+p$  junctions. Therefore, the interface was investigated using cross-sectional transmission electron microscopy.

Figure 9 shows the cross sections of silicon after arsenic is implanted either through a 100-Å oxide or into bare surfaces at 120 keV with a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ . It is observed that a transition region exists between the ion-implantation-generated amorphous layer and the substrate. The thickness of the transition region is about 300 or 500 Å for through-

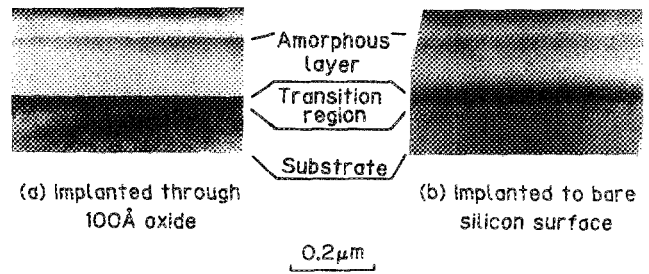


FIG. 9. Cross-sectional TEM micrographs of silicon after arsenic implantation at 120 keV and at a dose of  $1 \times 10^{16} \text{ cm}^{-2}$ : (a) implanted through 100 Å oxide and (b) implanted into bare silicon surface.

oxide-implanted or bare-surface-implanted samples, respectively. The existence of such a transition region indicates that the interface between the implanted region and the substrate is not an abrupt transition from amorphous to single crystal. The transition region would be a highly defective region of silicon. Defects in the transition region would grow to secondary defects during post-implantation anneal and contribute to the increase in the reverse-bias current.

Figure 10 shows the cross section of arsenic-implanted silicon annealed at 1000 °C, also imaged by transmission electron microscopy. It is seen that large defects extend from the transition region into the regrown layer as well as into the substrate. Furthermore, it is very important to note that much higher density defects exist in the through-oxide-implanted sample. In spite of such high density defect generation, the reverse-bias current level of 1000 °C-annealed  $n^+p$  junctions is very small. This is because these defects remain within the  $n^+$  layer, which has been expanded by the thermal diffusion of implanted arsenic. The problem is that such defect generation is much more significant for low-temperature-annealed  $n^+p$  junctions, since the impurity diffusion at low temperatures is negligibly small, and grown defects are included in the depletion region of a reverse-biased  $n^+p$  junction, increasing the reverse-bias current.

The higher defect density found in the through-oxide-implanted sample suggests that knock-on-implanted oxygen atoms could enhance such defect generation. This means that the defect generation would be a combined effect of a highly defective transition region and the contaminant species incorporated into the transition region. Therefore, the elimination of any kind of contamination involvement into the ion-implanted region is of paramount importance to suppress the defect generation and to realize low reverse-current  $n^+p$  junctions. This is the reason we have developed an ultra-

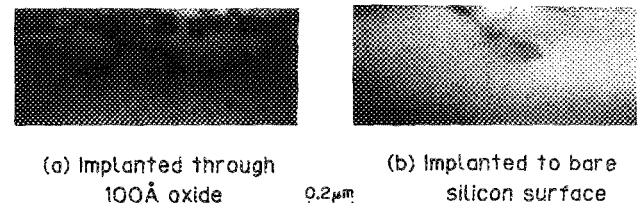


FIG. 10. Cross-sectional TEM micrographs of arsenic-implanted silicon annealed at 1000 °C for 30 min: (a) implanted through 100-Å oxide and (b) implanted into bare silicon surface.

clean ion-implantation technology, which will be discussed in the following.

#### D. Ultraclean ion implantation

Figure 11 shows the dependence of reverse-bias current on the annealing temperature. Arsenic implantation was performed into bare silicon surfaces under two different base pressures, viz.,  $5 \times 10^{-10}$  and  $1 \times 10^{-7}$  Torr. The energy and ion doses were 105 keV and  $6 \times 10^{15} \text{ cm}^{-2}$ , respectively. A definite difference in the reverse-bias current was observed in  $n^+p$  junctions formed under different vacuum conditions. Especially at the temperature range of 800 °C to 900 °C, the reverse-bias current was reduced by about one order of magnitude under the high vacuum condition. However, an apparent difference was not observed for samples annealed below 700 °C.

The reverse-bias current data shown in Fig. 11 were separated into two components, i.e., the peripheral current-density component and the areal current-density component. The annealing temperature dependence of the areal current-density component is shown in Fig. 12, where the data for  $n^+p$  junctions formed at 25 keV under the ultrahigh vacuum condition is also presented. More than one order of magnitude improvement in the reverse-bias current level is seen for

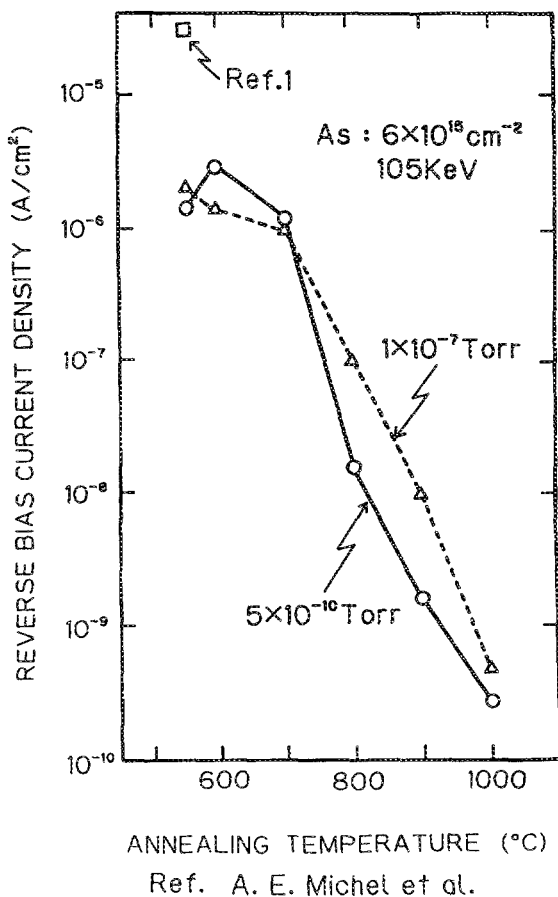


FIG. 11. The effect of background pressure on the magnitude of reverse-bias current (at 5 V) in  $pn$  junctions annealed at varying temperatures. In UHV ( $5 \times 10^{-10}$  Torr) implanted samples, about an order of magnitude reduction in the reverse current is obtained for samples annealed above 800 °C.

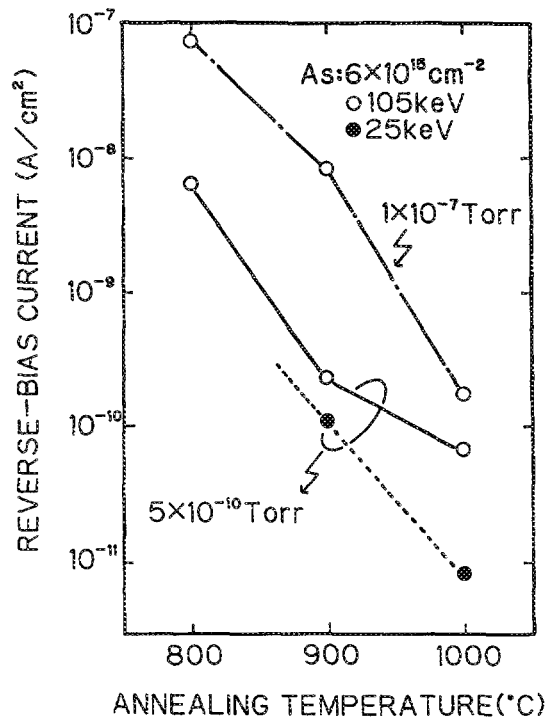


FIG. 12. The areal leakage current component extracted from the data shown in Fig. 11 as a function of annealing temperature. The data for  $n^+p$  junctions formed at 25 keV under the ultrahigh vacuum condition is also included.

samples annealed at 800 °C and 900 °C by UHV implantation. A further reduction in the reverse current is obtained for samples implanted at 25 keV. The reduction in the reverse-bias current observed in samples implanted under UHV conditions is interpreted as follows: The contamination involvement due to the residual gas adsorption such as  $\text{H}_2\text{O}$ ,  $\text{O}_2$ ,  $\text{CO}_2$ , etc., onto the silicon surface and their recoil implantation into the transition layer has been decreased.

The base pressure of  $10^{-7}$  Torr corresponds to the monolayer formation time of about 10 s, that is, about 120 monolayers of residual gas molecules are formed on the wafer surface during the typical implantation time of about 20 min if the sticking coefficient of unity is assumed. When the monolayer thickness of 3 Å is assumed, the effective thickness of the contaminant layer formed on the wafer surface during the entire period of ion implantation would be about 360 Å. These contaminant molecules may have a chance to be recoil implanted into the silicon. Although the assumption of the unity sticking coefficient is not realistic, the effective thickness of 360 Å is not negligible as a source of contamination because serious damages were generated by implantation through 100-Å oxide, as shown in Fig. 10. Under the base pressure of  $5 \times 10^{-10}$  Torr, the effective thickness of a contaminant layer is about 1.8 Å, which would be small enough to cause any serious contamination to the ion-implanted region.

There is another serious contamination source in the ion-implantation system. This is the high-energy ion-beam sputtering of component parts in the ion implanter. We put a number of test pieces of silicon wafer at various locations in



the implanter and analyzed the surface contamination after a period of about one month. SIMS (secondary-ion-mass spectroscopy) and XPS (x-ray photoemission spectroscopy) analyses on these pieces revealed that the components of stainless steel and aluminum were deposited on these silicon pieces, thus verifying that such contamination really exists. By carefully reviewing the geometrical configuration of the ion implanter, we installed a sputtering protection apparatus in the implanter. The apparatus is a silicon wafer with an opening at the center for a beam path. Two pieces of such wafers were installed between the Faraday cup and the wafer holder, preventing the component parts from being sputtered and also a wafer from being contaminated by sputtered metal species. However, it should be noted that the protection is not complete at present, and the sputter contamination has been only partially suppressed. The construction of a more effective protection apparatus is in progress, and the results will be presented in the near future.

The effect of such sputtering protection is demonstrated in Fig. 13, where the reverse-bias current at a reverse-bias voltage of 5 V is shown as a function of annealing temperature. The arsenic implantation was carried out with conditions identical to those in Fig. 12. All samples were implanted under the UHV ( $5 \times 10^{-10}$  Torr) condition and the data are shown for two cases, viz., with or without the sputtering protection apparatus. Further reduction in the reverse current is evident from the figure. It is interesting to see that large improvements in the reverse current level are achieved for samples annealed at low temperatures, i.e., at 600 °C–700 °C. This fact indicates that the suppression of defect generation in the vicinity of the transition region has been achieved.

Decrease in the acceleration energy also contributes to further reducing the reverse current, as shown in Fig. 14. The arsenic implantation was performed under the UHV condition with the sputtering protection apparatus installed. The ion dose was adjusted to yield the identical arsenic peak concentration in both 25- and 105 keV implanted samples. Lower leakage current levels are obtained for samples implanted at 25 keV. We have already seen similar effects in Figs. 4 and 12, where the reverse current was reduced by decreasing the ion-implantation energy. It is expected that the transition-region width decreases with a decrease in the ion energy. A smaller thickness of a transition region would be more favorable in suppressing the defect generation from the transition region. The reduction in the reverse current observed for the 25 keV implantation can be explained by the decrease in the transition-region width. As a result, the reverse-bias current density for *pn* junctions formed at 550 °C is about  $1.2 \times 10^{-7}$  A/cm<sup>2</sup>, which is more than two orders of magnitude smaller than previously reported data.<sup>1</sup>

The relationship between the transition-region thickness and the ion-implantation parameters, such as dose, energy, ion mass, substrate temperature, etc. as well as the effect of the transition-region thickness on damage generation, will be described in detail in a separate article.

For further reducing the reverse-bias current density in *n<sup>+</sup>p* junctions annealed at temperatures as low as 500 °C–600 °C, it is most essential to minimize the transition-region

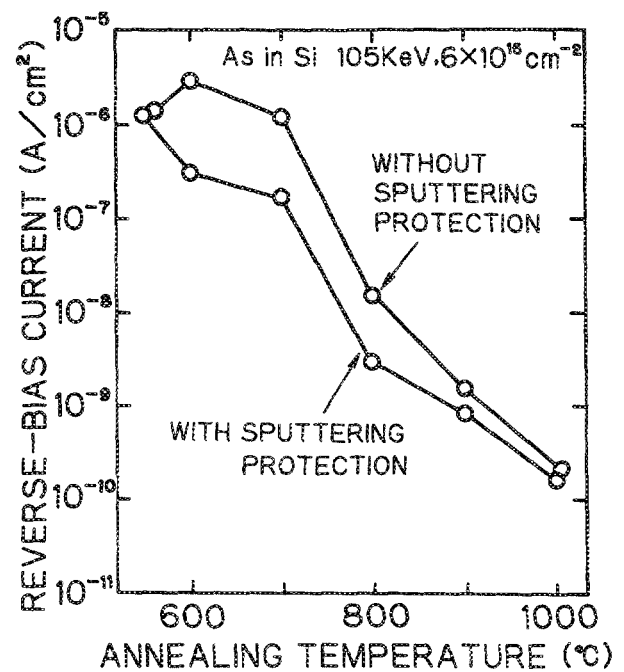


FIG. 13. Annealing temperature dependence of reverse-bias current with or without the sputtering protection apparatus. All implantation was carried out under the UHV condition. Large improvements in the reverse current are achieved for 600 °C–700 °C annealed samples.

thickness in addition to the perfect elimination of sputtering events occurring in the implanter.

## V. CONCLUSIONS

The characteristics of arsenic-implanted *pn* junctions that were annealed at low temperatures have been investigat-

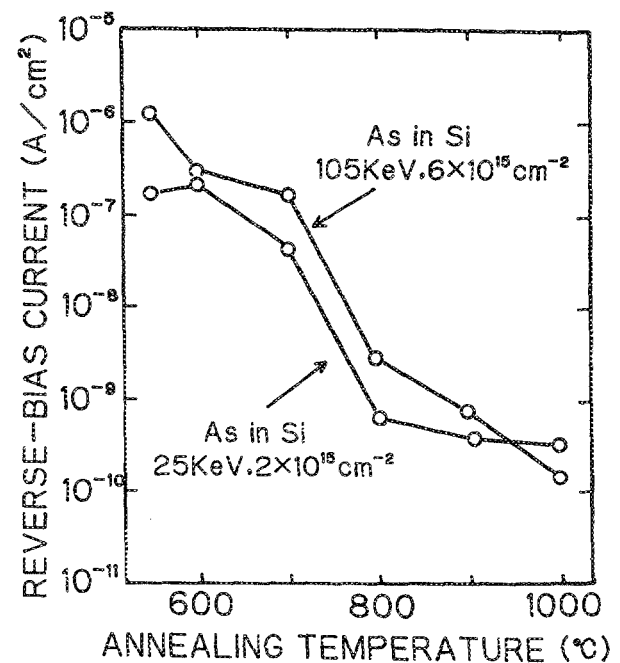


FIG. 14. The effect of reducing acceleration voltage on the reverse-bias current level. The ion dose was adjusted to yield the identical arsenic peak concentration in both samples. Ion implantation was performed under the UHV condition with a sputtering protection apparatus.

ed. Good crystallinity of a regrown layer as well as high carrier concentrations over  $10^{20} \text{ cm}^{-3}$  have been achieved by a post-implantation anneal at temperatures as low as  $550^\circ\text{C}$ . However, the problem was the increased reverse-bias current in low-temperature-annealed  $pn$  junctions that typically exhibited values over three orders of magnitude larger as compared to the  $1000^\circ\text{C}$  annealed junctions. The residual damages existing underneath the ion-implanted layer are exposed in the depletion layer of a reverse-biased junction, contributing to an increase in the generation current. Therefore, the reduction in reverse-bias current in low-temperature-annealed  $pn$  junctions is able to be achieved by eliminating such end-of-range damage. The stress compensation technology employing arsenic-phosphorus combined implantation has been demonstrated to be very effective in reducing the lattice strain and in suppressing the defect generation. We have found through a series of cross-sectional TEM studies that such end-of-range defect generation is determined as a combined effect of a transition region and the contaminant species incorporated into the transition region. Contamination involvement into the transition region has been suppressed by an ultraclean ion-implantation technology. Ion implantation was carried out under a UHV (base pressure of  $5 \times 10^{-10}$  Torr) condition and the recoil implantation of absorbed impurity molecules at the surface has been eliminated. Contamination due to the high-energy ion-beam sputtering of component parts of the ion implanter was also suppressed by installing a sputtering protection apparatus. As a result, the reverse-bias current for arsenic-implanted  $n^+p$  junctions annealed at  $550^\circ\text{C}$  has been reduced to about  $1.2 \times 10^{-7} \text{ A/cm}^2$ , which is more than two orders of magnitude smaller than previously reported data. In order to further reduce the reverse-bias current level, it is essential to reduce the thickness of a transition region by optimizing the ion-implantation conditions. In addition, the perfect elimination of sputtering contamination will be a key to realizing low-reverse-current  $pn$  junctions by low-temperature annealing.

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