IEICE TRANS. ELECTRON., VOL.E82–C, NO.4 APRIL 1999

PAPER

Reversible Energy Recovery Logic Circuits and Its 8-Phase Clocked Power Generator for Ultra-Low-Power Applications

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SUMMARY We proposed Reversible Energy Recovery Logic (RERL) using an 8-phase clocking scheme [1], which is a dual-rail reversible adiabatic logic for ultra-low-energy applications. Because we eliminated non-adiabatic energy loss in RERL by using the concept of reversible logic, RERL has only adiabatic and leakage losses. In this paper we explain its operation and logic design and present its simulation and experimental results. We also present an energy-efficient 8-phase, clocked power generator that uses an off-chip inductor. With simulation results for the full adder, we confirmed that the RERL circuit consumed substantially less energy than other logic circuits at low-speed operation. We evaluated a test chip implemented with a 0.6-μm CMOS technology, which integrated a chain of inverters with a clocked power generator. In the experimental results, the RERL circuit consumed only 4.5% of the dissipated energy of a static CMOS circuit at an optimal operating speed of 40 kHz. In conclusion, RERL is suitable for the applications that do not require high performance but low-energy consumption because its energy consumption can be decreased to the minimum by reducing the operating frequency until adiabatic and leakage losses are equal.

key words: *reversible logic, adiabatic circuit, clocked power generator, RERL (reversible energy recovery logic)*

1. Introduction

In the adiabatic circuits, the signal energy is recycled to reduce energy consumption, and besides leakage current loss there are two types of energy consumption: adiabatic and non-adiabatic losses. In the circuit shown in Fig. 1(a), when a switch is on, the adiabatic loss per a transition of the clocked power ϕ is inversely proportional to its transition time T, which is represented by

$$E_{adiabatic} = \frac{R_{on}C_L}{T} C_L V_{dd}^2, \tag{1}$$

where R_{on} is the on-resistance of the switch and C_L is the load capacitance, assuming that $R_{on}C_L$, the time constant of the circuit, is much smaller than T.

If any voltage difference between the two terminals of a switch exists when it is turned on, non-adiabatic loss occurs. This loss, which is independent of the transition time of the clocked power, is proportional to the square of the voltage difference like the following:

$$E_{non\text{-}adiabatic} = \frac{1}{2}\frac{C_1C_2}{C_1+C_2}(V_1-V_2)^2, \tag{2}$$

where C_1 and C_2 are the capacitances of the two nodes connected to the switch, as illustrated in Fig. 1(b), and V_1 and V_2 are their node voltages just before the switch turns on.

Several adiabatic circuits with non-adiabatic loss were proposed previously in [2]–[4], in which, to determine the energy supplying or recovering path of a node, only the node signal itself and its inputs are used. In these adiabatic circuits, it is not possible to supply or recycle the signal energy of a node perfectly without the "retractile cascades" problem [5]. To recycle the signal energy perfectly, we need to use the diodes with zero turn-on voltage or the MOS transistors with zero threshold voltage with good on-off characteristics, which are not available in reality. Therefore, in such adiabatic circuits, non-adiabatic loss occurs due to their turn-on voltage if such diodes are used, and due to their threshold voltage if such MOS transistors are used. Furthermore, this non-adiabatic loss becomes dominant compared with adiabatic energy loss at lower operating frequencies. Therefore, the adiabatic circuits that have non-adiabatic loss are not suitable for the ultra-low-energy applications.

This non-adiabatic loss can be eliminated by using the concept of reversible logic, which has been employed to several adiabatic logic circuits for ultra-low-energy applications [1], [5]–[7]. To recover the energy of a signal node perfectly, we must use a separate energy-recovering path to avoid the "retractile cascades" problem. To recycle the energy of the input signals in a logic stage, we need to reconstruct the input from its output signals, which requires reversible logic.

Although Merkle's logic in [5] eliminated non-

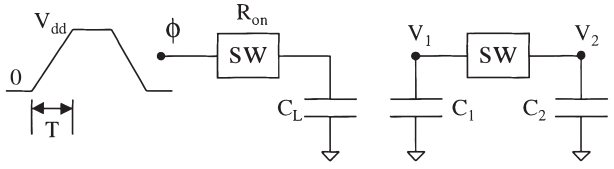

Fig. 1 (a) Adiabatic loss exists if ϕ swings between V_{dd} and GND when the switch is on. (b) Non-adiabatic loss exists if the switch is on when $V_1 \neq V_2$.

Manuscript received September 17, 1998.
Manuscript revised November 11, 1998.

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adiabatic loss completely, it has the "retractile cascades" problem because it did not use the reversible logic. The split-level charge recovery logic (SCRL) [6] employed the reversible logic to solve this problem, but it requires too many clock-rails up to 24 although it is a single-railed logic. The logic of Athas's group [7] resolved the "retractile cascades" problem, but it still has non-adiabatic loss at some internal nodes in each logic stage [1], [8].

We proposed RERL in [1], which is a dual-rail adiabatic logic circuit using a new 8-phase clocking scheme. By using the concept of reversible logic, we eliminated non-adiabatic energy loss in RERL. Therefore, RERL has only adiabatic and leakage losses. In the adiabatic circuit, the energy consumption in the clocked power generator cannot be ignored. Therefore, we propose an energy-efficient 8-phase, clocked power generator that uses only an off-chip inductor. Furthermore, we must evaluate an adiabatic circuit together with its clocked power generator to evaluate it properly. So we implemented an RERL circuit with its clocked power generator and measured its energy consumption.

The purpose of this paper is to describe the logic design of RERL and to present its simulation and experimental results. In Sect. 2, we explain the operation of RERL and its logic design. We also describe the optimal operating speed for the lowest energy dissipation for RERL and its simulation results for energy dissipation. In Sect. 3, we explain an energy-efficient 8-phase, clocked power generator. In Sect. 4, we present experimental results of the test chip that includes a chain of RERL inverters integrated with a clocked power generator, which is followed by the conclusion in Sect. 5.

2. RERL

To eliminate non-adiabatic loss, a switch must be turned on only if there is no voltage difference between its two terminals, which is referred to as zero-voltage switching (ZVS). In RERL, we use the reversible logic to satisfy the ZVS condition. In Sect. 2.1, we describe the operation of an RERL buffer and how the ZVS condition is satisfied, and present the implementation of a reversible full adder as an example. In Sect. 2.2, we compare 2N-2N2P and RERL with the simulation results of a full adder.

2.1 RERL Operation

A basic RERL gate, which is either a buffer or an inverter, is shown in Fig. 2(a) and its reversible pipeline connection is shown in Fig. 2(b). The symbol for an RERL buffer chain is also shown for simplicity in Fig. 2(c): the buffer in Fig. 2(a) corresponds to the shaded parts in Fig. 2(c). The transmission gates T1 and T2 (T3 and T4) implement dual-rail forward (backward) logic functions, which determine the charging

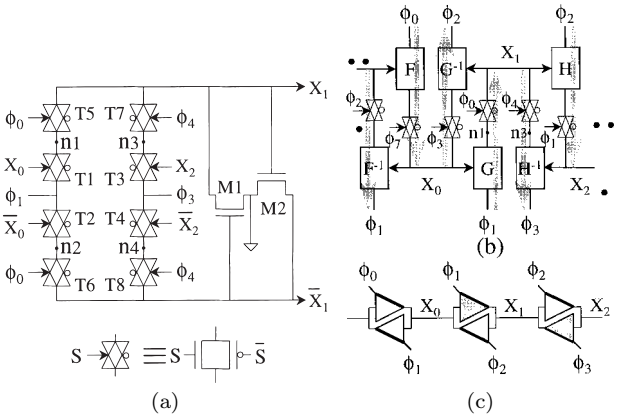


Fig. 2 Reversible energy recovery logic (RERL): (a) a buffer, (b) reversible pipeline connection, and (c) symbol for a buffer chain. A shaded arrow in (b) indicates the direction and path of energy charging or discharging. F, G, and H are forward functions of each logic stage, and F^{-1}, G^{-1} and H^{-1} are their backward functions, respectively. A thick solid line in the buffer symbol of (c) indicates the energy flow. The buffer in (a) corresponds to the shaded parts in (c). Note that the clocks connected to the isolation switches are not shown explicitly in the symbol.

(discharging) paths of the output nodes. The transmission gates T5 and T6 (T7 and T8) are forward (backward) isolation switches, which isolate the charging (discharging) paths.

The clamp transistors M1 and M2 are connected to the output nodes to make the undriven output node stay at ground. Note that unlike to the reversible adiabatic logic proposed in [7], the charging and discharging clocks of a logic stage are separated in the RERL circuit, as shown in Fig. 2, which is required to eliminate non-adiabatic loss [1]. For example, ϕ_1 supplies the energy to node X_1, which is recovered to ϕ_3. The direction and path of the energy flow are illustrated with the shaded arrows in Fig. 2(b).

RERL uses an 8-phase clock, shown in Fig. 3(a). The waveforms of all the nodes in an inverter are shown in Fig. 3(b), as an example, for an input sequence of "110." Here, X_0 is an input signal, X_1 is its pipelined output signal, and X_2 is the output signal of the next stage, whose input is X_1. X_2 is also used as the input to the backward function used to recover the energy of X_1. The sub-index of each signal X indicates its corresponding clock phase, which supplies the energy to the signal. All nodes do not have any abrupt voltage change, which implies that non-adiabatic loss does not occur in RERL. Note that a node of two consecutive logic 1's in RERL such as "11" (for example, X_0 from T = 0 to T = 15) does not keep staying high because a logic "1" is represented as a return-to-zero signal in RERL, as shown in Fig. 3(b).

The operation of an RERL buffer gate is as follows. During the time interval T = 0, the input X_0 goes high and the forward isolation switches T5 and

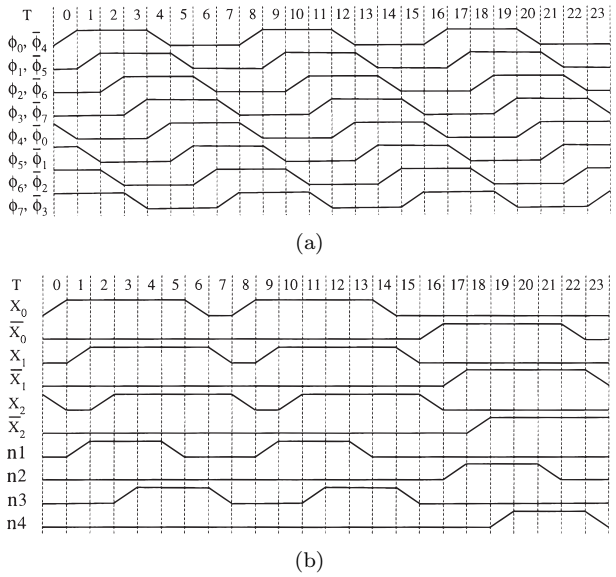


Fig. 3 Waveforms of (a) the 8-phase clock and (b) all the nodes in an RERL buffer.

T6 are turned on. During T = 1, both X_1 and n1 go high via T1 and T5 by the rising ϕ_1 slowly, but both $\overline{X_1}$ and n2 stay at ground because they are driven by the clamp devices and T2 is off. During T = 2, the outputs of the next stage, X_2 and $\overline{X_2}$, go high and stay low, respectively. During T = 3, n3 goes high via T3, and n4 is still at ground because T4 is off. During T = 4, the forward isolation switches T5 and T6 are turned off and the backward ones T7 and T8 are turned on.

During T = 5, the falling ϕ_1 discharges n1 without non-adiabatic loss because T1 is still on due to X_0. During T = 6, the falling ϕ_2 in the previous stage discharges X_0. During T = 7, the falling ϕ_3 discharges both X_1 and n3 because both T3 and T7 are still on due to X_2 and ϕ_4, respectively. During T = 8, the backward isolation switches T7 and T8 are turned off to repeat the 8 steps.

In Fig. 2(a), to explain the role of reversible logic, we assume that the forward and backward logic functions are G and H^{-1}, the output is X_1, and the output of its next stage is X_2 like Fig. 2(b). To make it simple, we describe it as a single-rail. We will explain briefly how RERL satisfies the ZVS condition to eliminate non-adiabatic loss. First, all internal nodes are grounded in the logic gate whose output is X_1 before ϕ_1 goes high. Then, the forward isolation switch T5 can be turned on with rising ϕ_0 without violating the ZVS condition. At the same time, the input to the forward logic function G, can be made valid, which determines the energy-supplying path to the output X_1 with satisfying the ZVS condition because the node X_1 and its energy supply clock ϕ_1 are all grounded. Then, the output X_1 is evaluated when ϕ_1 rises. Next, when ϕ_2 goes high, the output of the next stage is evaluated,

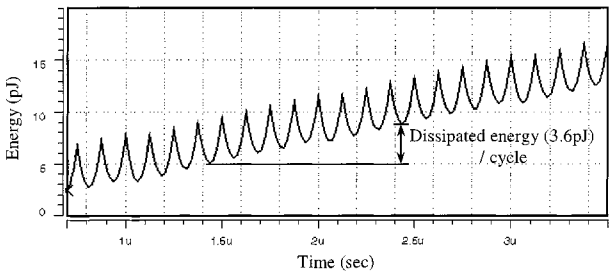


Fig. 4 Energy curve for a 16-stage RERL buffer chain.

which is $X_2 = H(X_1)$ with satisfying the ZVS condition because ϕ_3 and n3 are all grounded. When the energy-recovering clock ϕ_3 is rising, the backward logic function H^{-1} is evaluated, which determines the energy-recovering path from the output. Note that all logic functions are reversible here. Then, n3 has the same value of X_1 because $H^{-1}(X_2) = H^{-1}H(X_1) = X_1$. Therefore, we can turn on the backward isolation switch T7 with satisfying the ZVS condition because the outputs X_1 and n3 are equal. Then you can lower the energy-recovering clock ϕ_3 to recover the energy of the node X_1. Consequently, there is no non-adiabatic charging or discharging loss at any node because the voltage difference between the two terminals of a switch is always zero when it is turned on as shown in Fig. 3(b).

We obtained the energy dissipation curve for a 16-stage buffer chain with SPICE simulations, as shown in Fig. 4. The dissipated energy per cycle is 3.6 pJ when the operating frequency is 1 MHz and the peak voltage of the clocked power is 5 V. Note that the curve repeats periodically energy supply (uphill) and recovery (downhill).

Although the buffer (or inverter) shown in Fig. 2 is basically reversible, most of the Boolean gates are not reversible. Note that mapping from the input to the output must be always one-to-one to be a reversible logic gate. As many Boolean functions require "garbage" information to make them reversible [9], there is some circuit overhead due to reversibility. The output in an RERL full-adder contains "garbage" information for reversibility such as X^* and $C_{in}{}^*$, as shown in Fig. 5, which are delayed copies of the input signals X and C_{in}, respectively. Similarly, we can make any Boolean function a reversible one by simply adding some "garbage" information.

2.2 Energy Dissipation

Because the RERL circuit has only adiabatic and leakage losses, the dissipated energy per cycle in a node is represented by

$$E_{diss} = \frac{2R_{on}C_L}{T}C_L V_{dd}^2 + V_{dd}I_{leak}(N-1)T, \quad (3)$$

where N, the number of phases in a cycle, is eight, as

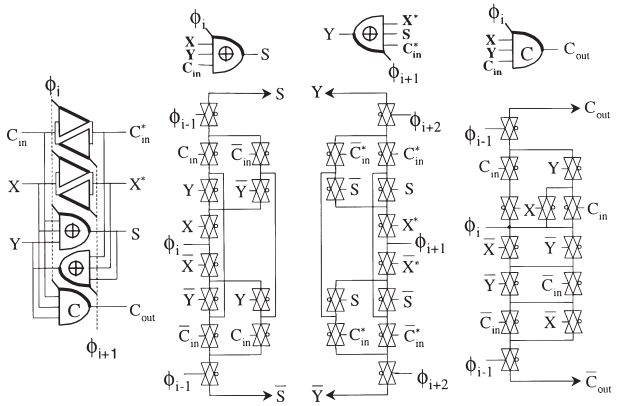


Fig. 5 Schematic of an RERL full adder.

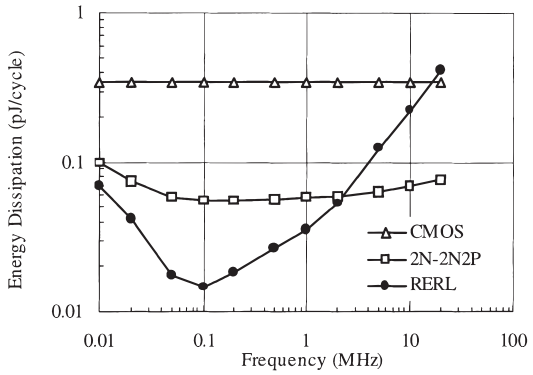


Fig. 6 Energy dissipation vs. operating frequency for a full adder.

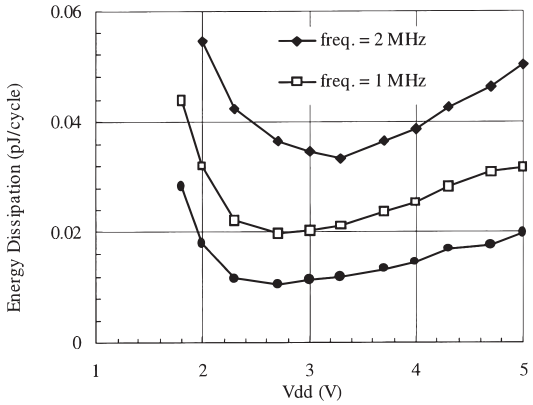


Fig. 7 Energy dissipation in an RERL full adder vs. supply voltage.

shown in Fig. 3(a) and T is the time for a phase, which equals to the transition time of the clocked power. Note that we excluded an idle phase in the second term in Eq. (3) because there is no leakage loss during the idle phase in each cycle. The on-resistance of a transmission gate was derived in [7]. If the operating speed is reduced with increasing T, adiabatic energy loss decreases but leakage current loss increases in Eq. (3). Therefore, there is an optimal operating speed that minimizes the energy dissipation. When the derivative of E_{diss} to T is equal to zero, we obtain

$$T_{opt} = C_L\sqrt{2R_{on}V_{dd}/((N-1)I_{leak})}, \tag{4}$$

$$E_{min} = 2C_LV_{dd}\sqrt{2R_{on}V_{dd}(N-1)I_{leak}}. \tag{5}$$

Therefore, the energy consumption of RERL can be decreased to this minimum E_{min} by reducing the operating frequency, $1/(8T_{opt})$, until adiabatic and leakage losses are equal.

Just like the conventional CMOS circuits, the leakage current in the RERL circuit consists of two types of components: reverse-biased diode leakage at the transistor drains and sub-threshold leakage in the "off" transistors [10]. Note that the sub-threshold current of the transistors is dominant to the reverse-biased diode leakage current in the RERL circuits.

The SPICE simulation results in Fig. 6 compare the energy dissipations of full adders for the static CMOS logic and two adiabatic logic circuits: 2N-2N2P [2] and RERL. In the SPICE simulation, we used the MOSFET models for 0.6-μm CMOS technology, in which the threshold voltages of nMOS and pMOS are 0.7 V and -0.9 V, respectively. We used a size of W/L $= 1.0\,\mu$m$/0.6\,\mu$m for both nMOS and pMOS transistors in all circuits and the supply voltage is 5 V.

The simulation results show that the energy dissipation of an RERL full adder decreases as the operating frequency decreases, while that of the static CMOS is constant. And that of 2N-2N2P does not decrease further during low-speed operation where the non-adiabatic losses become dominant compared to adiabatic losses. The RERL full adder consumed only 4.2% of the energy dissipated in the static CMOS full adder when the operating frequency was 100 kHz. When the operating frequency was slower than 100 kHz, leakage current loss became dominant in RERL. Note that the RERL adder consumed more energy than the 2N-2N2P one in the high-frequency range because the energy consumption in RERL is mostly the adiabatic loss, which is proportional to the operating frequency, while that in 2N-2N2P is non-adiabatic loss, which does not depend on the operating frequency.

In the conventional CMOS circuits the energy dissipation is proportional to the square of the supply voltage. However, adiabatic loss in the adiabatic circuits increases if the peak supply voltage goes below energy-optimal supply voltage, which is about $4V_{th}$ in [7], because of sharp increase of the switch on-resistance. This optimum supply voltage for the minimum energy dissipation is in the range of 2.7 V to 3.3 V in the simulation results shown in Fig. 7.

3. 8-Phase Clocked Power Generator

We can generate the clock waveforms of the 8-phase

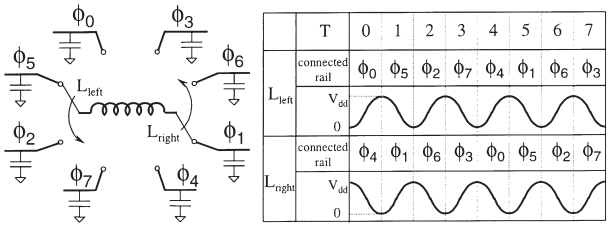


Fig. 8 Switching order that indicates how two terminals of the inductor are connected to two out of eight clock rails.

clocked power as shown in Fig. 3(a) with a small control logic circuit and an off-chip inductor. Figure 8 illustrates how the two terminals of the inductor are connected to two out of eight clock-rails and how the connections are changed, which must be repeated in every 8 steps. This clocked power generator is required to be efficient in energy consumption. Therefore, the connection of two terminal of the inductor must be changed only when the inductor current is zero. That is to say, the change of each clock-rail should be made only when the voltage of each terminal of the inductor is at its highest or lowest value.

Assume that initially, L_{left} is at ground and L_{right} is at V_{dd}. During the time interval T = 0, L_{left} and L_{right} are connected to ϕ_0 and ϕ_4, respectively, and then ϕ_0 swings from ground to V_{dd} and ϕ_4 swings from V_{dd} to ground simultaneously. During T = 1, L_{left} and L_{right} are connected to ϕ_5 and ϕ_1, respectively, and ϕ_0 and ϕ_4 are clamped to V_{dd} and GND, respectively, to make their states truly high or low. Similarly, L_{left} and L_{right} are connected to each clock-rail according to the switching order summarized in Fig. 8 and the unconnected clock-rails are clamped to their own states.

The block diagram of the clocked power generator is shown in Fig. 9. We clock the 3-bit binary counter with an external reference clock, whose frequency must be 8 times that of the clocked power. Each clock-rail driver connects its corresponding clock-rail to one of the two terminals of the inductor either with T9 or with T10. Otherwise, it clamps the rail either to V_{dd} with M3 or to GND with M4. Its control signals that determine the switching order as shown in Fig. 8 can be generated with the output of the 3-b counter.

The waveforms of the control signals for the rail ϕ_0 are illustrated in Fig. 9 and those for other rails can be generated similarly. Although four control signals for each rail driver are required, all eight drivers require only 12 control signals because of their regularity and similarity. Consequently, we implemented the on-chip control-logic circuit with three D-flip-flops for the 3-b binary counter and six NAND gates.

4. Experimental Results and Discussion

A test chip fabricated with a 0.6-μm n-well triple-metal CMOS technology includes a 512-stage RERL inverter

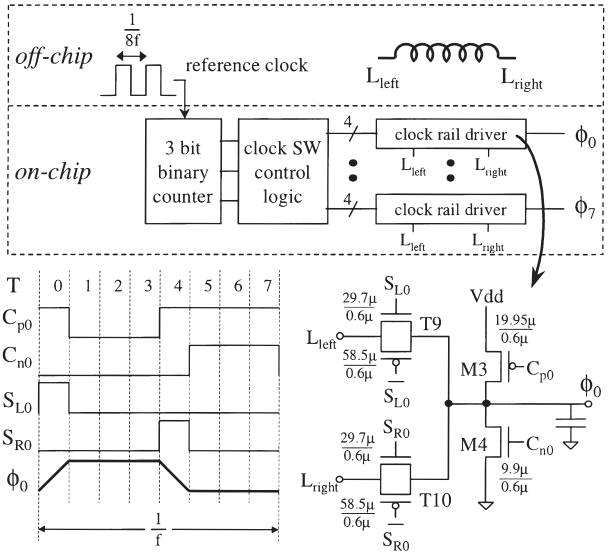


Fig. 9 Block diagram of a clocked power generator and its control signals.

chain and a clocked power generator. The RERL circuit requires no pipeline flip-flops for synchronous operation because of its characteristics of inherent pipelining. However, it requires an 8-phase clocked power. Therefore, we integrated the RERL inverter chain with an 8-phase clocked power generator on the test chip. Energy dissipation in the RERL inverter chain and that in the clocked power generator can be measured separately in the test chip.

To allow fair comparison, a static CMOS 512-stage inverter chain is also included in the test chip. Because we use a pipelined architecture in many designs and because RERL has inherent pipelining, we inserted a flip-flop every eight inverters in the CMOS inverter chain as a pipeline register. Inserting a flip-flop every eight inverters is an arbitrary choice of ours. Therefore, energy dissipation in the static CMOS inverter chain and that in the pipeline flip-flops can also be measured separately to eliminate the effect of this arbitrariness.

We used only the size of W/L=1.8 μm/0.6 μm for both nMOS and pMOS transistors in all circuits, except some devices in the clocked power generator. A photomicrograph of the test chip is shown in Fig. 10. The areas of the RERL inverter chain, the clocked power generator and the static CMOS inverter chain are 1.7×1.4 mm^2, 0.35×0.31 mm^2, and 0.27×0.83 mm^2, respectively. Although the number of the transistors in the RERL inverter chain is 8 times that in the static CMOS inverter chain, the area of the RERL one is about 10.6 times that of the static CMOS one due to the routing overhead.

We measured the waveforms of the clocks generated with the 8-phase, clocked power generator, as shown in Fig. 11. Edges in the waveforms of ϕ_1 and ϕ_2 are obtained by connecting them to the terminals at

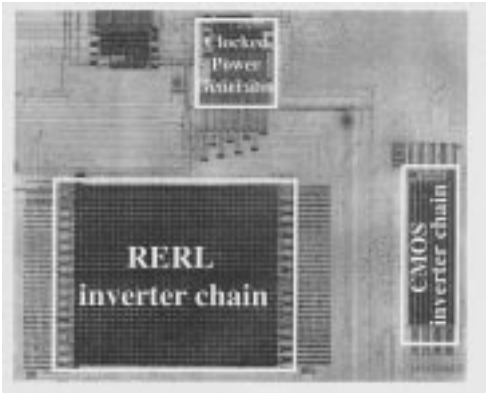


Fig. 10 Photomicrograph of the test chip.

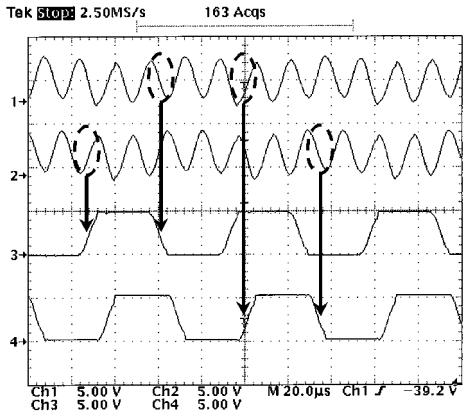
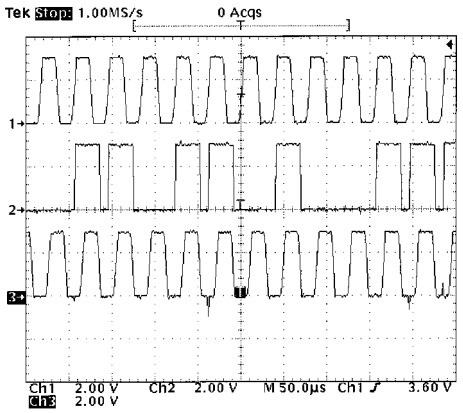
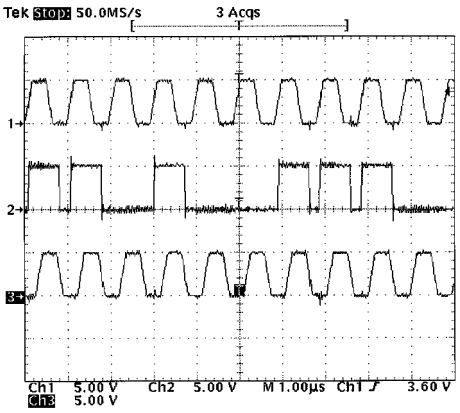


Fig. 11 Measured clock signal waveforms: Ch1: L_{left}, Ch2: L_{right}, Ch3: ϕ_1, Ch4: ϕ_2.



(a) $f = 25.4\,\mathrm{kHz}$, L = 100 mH, $V_{dd} = 3\,\mathrm{V}$, input sequence: 1001001...



(b) $f = 1.05\,\mathrm{MHz}$, L = 50 μH, $V_{dd} = 5\,\mathrm{V}$, input sequence: 0010110...

Fig. 12 Measured RERL waveforms: Ch1: energy-supplying clock ϕ_1, Ch2: buffered output of an RERL inverter, Ch3: energy-recovering clock ϕ_3.

the off-chip inductor in the right time interval, as designated with circles and arrows. We confirmed the correct operation of the clocked power generator up to the frequency of 6 MHz, and its corresponding reference clock is 48 MHz (= 8 × 6 MHz), which was simply bounded by the maximum frequency of the signal generator we have currently. The measured waveforms of the RERL circuits are shown in Fig. 12. Note that the adiabatic waveform corresponding to the "high" is a return-to-zero rectangular pulse, which is measured through a conventional CMOS output driver. Two clocks, ϕ_1 and ϕ_3, supplying and recovering the energy of the output node, respectively, are included in Fig. 12 for reference.

We also measured energy consumption in the test circuits for various operating frequencies and supply voltages, as shown in Figs. 13 and 14. Note that we excluded the energy consumption in the output drivers in both the static CMOS and RERL circuits in measurements because they are just for verification. In Fig. 13, energy dissipation of the RERL 512-stage inverter chain including its clocked power generator is compared with that of the static CMOS 512-stage inverter chain with its pipeline flip-flops. When the supply voltage of the two circuits was 5 V, the energy dissipation of the former was substantially less than the latter in all the range of operating frequencies we measured: the RERL circuit consumed only 4.5% of the dissipated energy of the static CMOS circuit at 40 kHz. If the operating frequency was higher than 40 kHz, the energy consumption of the RERL circuit was proportional to the operating frequency. However, at very low-speed operation slower than 40 kHz, the consumed energy was increased because the leakage current loss becomes dominant compared with the adiabatic energy loss.

We found the optimal supply voltage that minimize the energy-delay product for each of two circuits, 3.0 V for the RERL circuit and 1.8 V (= 2 × −0.9 V| = $2V_{th}$ in [11]) for the static CMOS circuit. We measured the energy dissipation in each circuit for its optimal supply voltage as shown in Fig. 13. In the curve, the operating frequency range where the RERL circuit outperforms the static CMOS circuit in energy dissipation still exists, even though it is reduced.

As shown in Fig. 14, we measured energy dissipa-

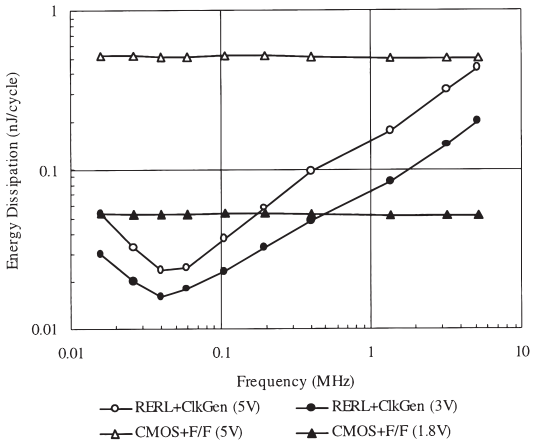


Fig. 13 Energy dissipation vs. operating frequency for the RERL inverter chain with clocked power generator and the static CMOS inverter chain with pipeline flip-flops: measured (1) at V_{dd} = 5 V, and (2) at the supply voltage that minimizes the energy-delay product for each circuit.

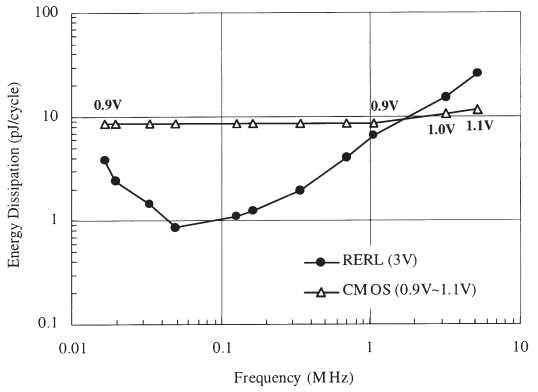


Fig. 14 Energy dissipation vs. operating frequency for the RERL and static CMOS inverter chain at the supply voltage that minimizes energy dissipation for each circuit: V_{dd} = 3.0 V for the RERL, V_{dd} = 0.9 V for the static CMOS logic if not indicated.

tion in each circuit with its supply voltage that minimizes the energy dissipation, which is 3.0 V for the RERL circuit and 0.9 V (= $|V_{tp}|$) for the static CMOS circuit. For the static CMOS circuit, $|V_{tp}|$ which is larger than V_{tn}, is the "theoretical lower limit" for its right operation. Note that this supply voltage in the static CMOS circuit is required to be larger than 0.9 V for proper operation if the operating frequency is higher than 2 MHz. When we measured energy dissipation for the RERL inverter chain, we excluded that in the clocked power generator. Similarly, we also excluded that in pipeline flip-flops for the static CMOS inverter. In this measurement, the RERL inverter chain consumes much less energy than the static CMOS inverter chain at the operating frequency less than 1 MHz. The energy dissipation in the RERL inverter chain is only 10% of that in the static CMOS inverter chain at the operating frequency of 50 kHz.

There are two possible applications of RERL in the future: heat-limiting and energy-limiting applications. We define the heat-limiting applications in which we cannot afford to use an expensive package to cool the circuit better. The intrinsic speed of the device will be increased as well as the integration level of VLSI circuits. Therefore, more VLSI circuits cannot be cooled down properly with a cheap package because the heat generated by their chip is too high. Consequently, we must slow down the VLSI circuits to reduce their heat generation. When the circuits must be slowed down, the reversible adiabatic circuits become more useful. In the energy-limiting applications, RERL has obvious advantage if the applications do not require high-performance. It is because its energy consumption can be decreased to the minimum by reducing the operating frequency until adiabatic and leakage losses are equal.

5. Conclusion

RERL is a dual-rail reversible adiabatic logic that uses an 8-phase clocking scheme. Unlike to the conventional adiabatic circuits, RERL has only adiabatic and leakage losses because we eliminated non-adiabatic energy loss by using the concept of reversible logic. We proposed an energy-efficient 8-phase clocked power generator using an off-chip inductor. With simulations and evaluation of the test chip, we confirmed that the proposed RERL consumes only adiabatic and leakage losses. We integrated a chain of RERL inverters with an 8-phase, clocked power generator in the test chip and we compared it with a static CMOS inverter chain in the same chip to allow fair comparison. We confirmed the proper operation of the clocked power generator in the test chip. The simulation and experimental results showed that the RERL circuit consumed substantially less energy than the static CMOS circuit at low-speed operation. In conclusion, RERL is suitable for the applications that do not require high performance but low-energy consumption such as implanted devices because its energy consumption can be decreased to the minimum by reducing the operating frequency until adiabatic and leakage losses are equal. We are in the process of designing more complex circuits with RERL such as a multiplier and a carry-lookahead adder.

Acknowledgments

This work was supported through the Inter-University Semiconductor Research Center by Korea Research Foundation and also through Seoul National University Nanoelectronics Institute by LG Semicon Company. The test chip was fabricated with the help of LG Semicon Design Contest in 1997. The authors would like to thank the two anonymous reviewers for their useful suggestions and comments.

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