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Supplementary Information

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VAN DER PAUW MEASUREMENTS

Local variation in conductance or threshold voltage due to defects in MoS_2 can be characterized using different van der Pauw configurations shown in Figure S1a. As shown in Figure 4 of the main manuscript, change in R_A/R_C with gate voltage results from different current paths in different measurement configurations, as a particular defect depending on its location will affect one configuration more than the other. To validate the van der Pauw measurements, we also characterized reciprocity i.e. the ratio of $R_C/(R_A + R_B)$, and found it to be equal to 1 as expected and shown in Figure S1b.[1–3]

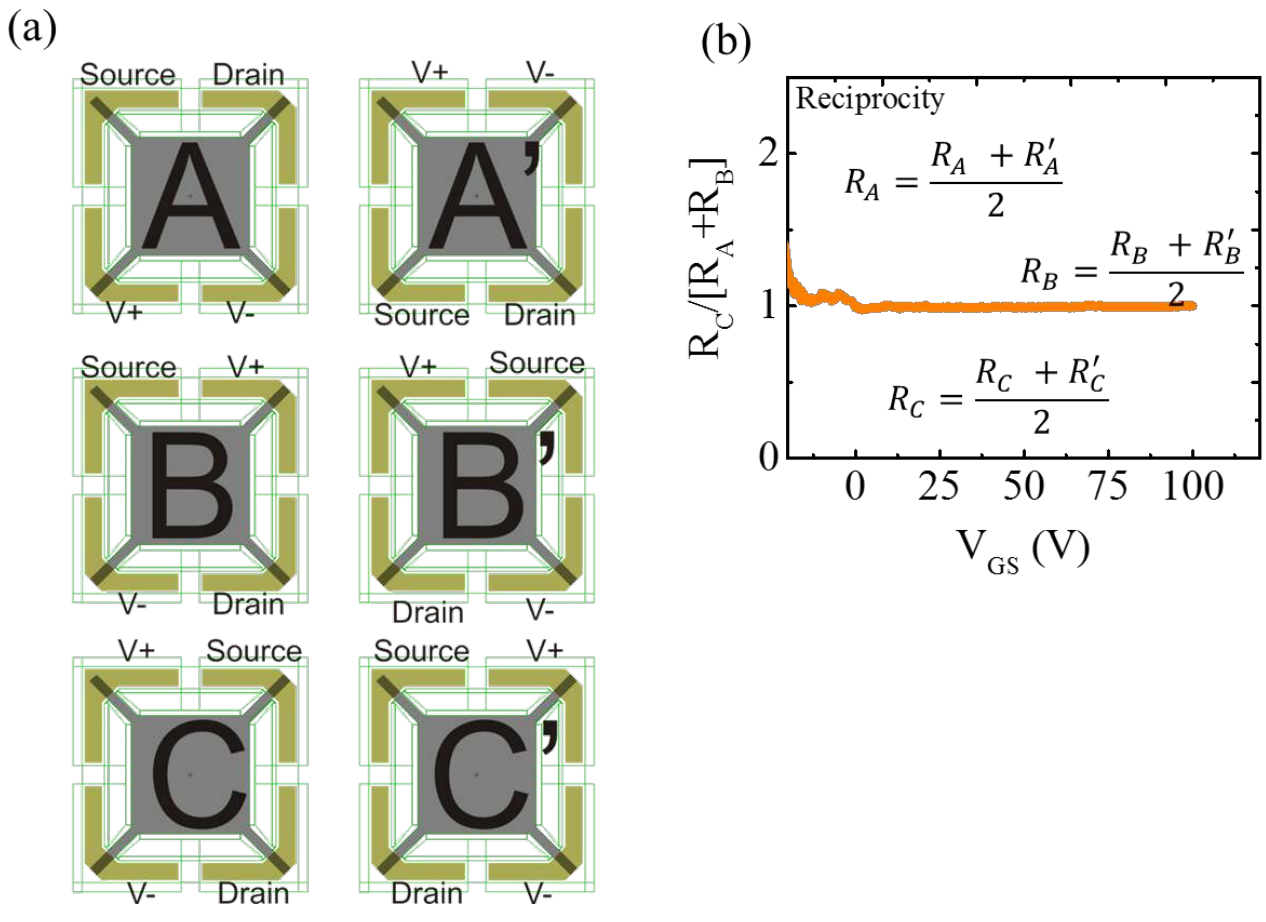

FIG. S1. (a) Different van der Pauw configurations used for electrical measurements. (b) Successful reciprocity check validating the van der Pauw measurements.

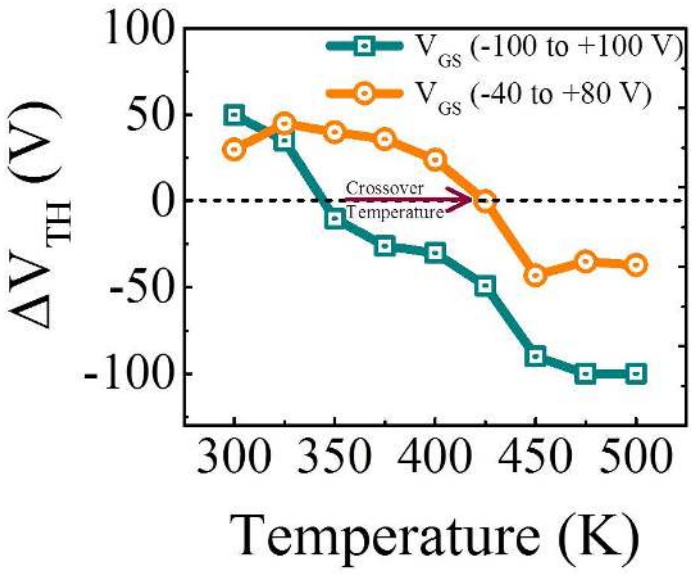

FIG. S2. Variation of crossover temperature (ΔV_{TH} crosses zero) for two different gate voltage ranges.

EFFECT OF GATE VOLTAGE RANGE ON CROSSOVER TEMPERATURE

Hysteresis crossover ($\Delta V_{TH} \sim 0$) at 350 K occurs due to movement of the threshold voltages in forward (FS) and reverse (RS) sweeps towards each other. The crossover temperature at which ΔV_{TH}=0 is seen to be a function of the maximum gate voltage (V_{GS}^{max}) as shown in Figure S2. Hysteresis collapse occurred at higher temperature of 425 K for smaller V_{GS}^{max} (V_{GS} range of -40 to 80 V) as compared to 350 K for V_{GS}^{max} of 100 V (V_{GS} range of $\pm$ 100 V).

COMPARISON OF HYSTERESIS IN SUPPORTED AND SUSPENDED TRANSISTORS

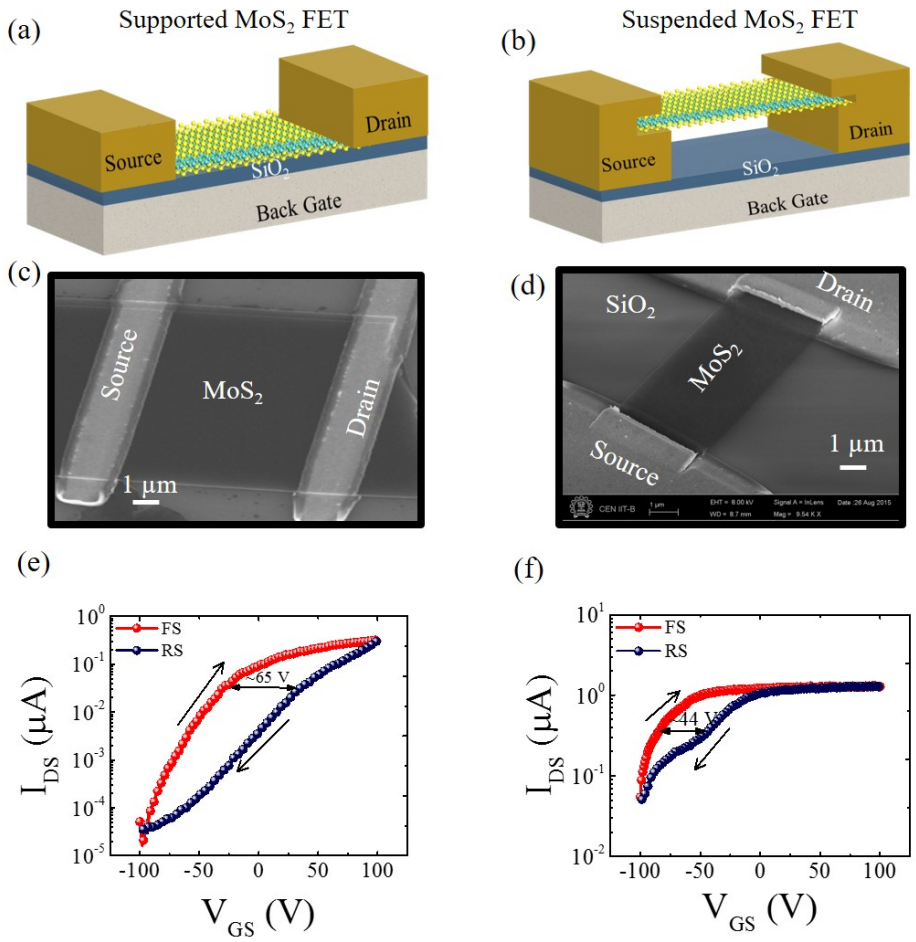

FIG. S3. 3D schematics of FETs with the MoS_2 layer (a) supported on SiO_2, and, (b) suspended ~100 nm above SiO_2. SEM images of (c) supported, and, (d) suspended MoS_2 transistors. Room temperature transfer characteristics ($I_{DS} - V_{GS}$) of (e) supported, and, (f) suspended FETs.

FORWARD AND REVERSE SWEEP TRANSFER CHARACTERISTICS FOR DIFFERENT TEMPERATURES

Figures S4a and b show variable temperature forward and reverse sweep transfer characteristics respectively. In the forward (reverse) sweep, threshold voltage shifts towards the right (left) with increasing temperature. Transconductance vs. gate voltage plots for different temperatures are shown in Figure S5. Figure S5a shows the change in transconductance (g_m) for forward sweep with temperature. A degradation in g_m from 1 μS to 0.5 μS at approximately fixed V_{GS} is observed for increase in temperature from 300 K to 325 K as

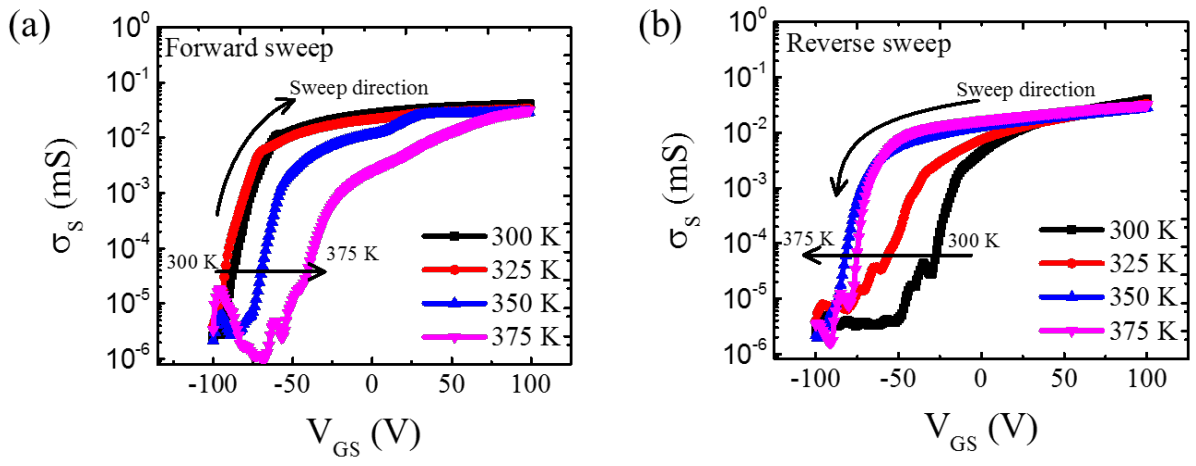

FIG. S4. Transfer characteristics of MoS_2 van der Pauw devices for temperatures varying from 300 to 375 K, for (a) forward sweep (threshold voltage shift to right), and, (b) reverse sweep (threshold voltage shift to left).

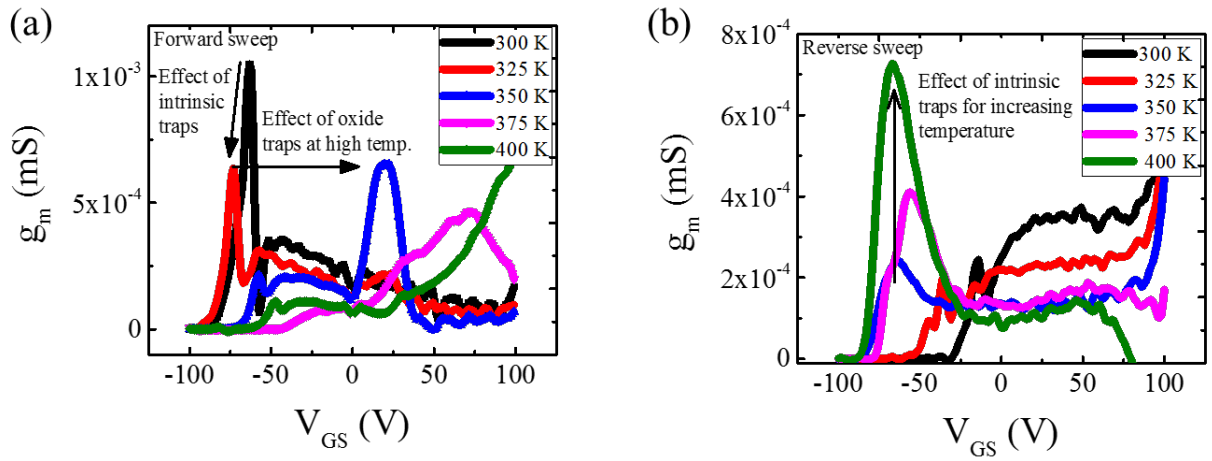

FIG. S5. Transconductance variation with V_{GS} and temperature in (a) forward sweep, and, (b) reverse sweep.

shown in Figure S5a. This lack of a V_{GS} shift in g_m peak indicates that the degradation in g_m is likely due to intrinsic defects/traps till nearly 350 K. However, a further increase in temperature enables the oxide trap mechanism (charge exchange between gate and oxide). As a result, negative charges in the oxide (i.e. due to electron tunneling from p^+ Si gate) shift the g_m peak towards right (higher V_{GS}) in the forward sweep as shown in Figure S5a. There is no shift in the g_m peak for the reverse sweep characteristics shown in Figure S5b since electrons released from the oxide traps at V_{GS} =+100 V (onset of reverse sweep) reduce

the oxide charge.

COMPARISON OF HYSTERESIS IN 2-TERMINAL AND 4-TERMINAL TRANSFER CHARACTERISTICS

To examine the effect of contact resistance on hysteresis and its inversion, we compared the transfer characteristics of two-terminal and 4-terminal (vdP) MoS_2 transistors as shown in Figure S6. Increase in sheet conductance (σ_S) for 4-terminal vdP configuration can be attributed to negligible contact resistance in these measurements. Nearly similar ΔV_{Th} for 2 and 4-terminal devices (Figure S6f) indicates that the effect of contact resistance on hysteresis is small.

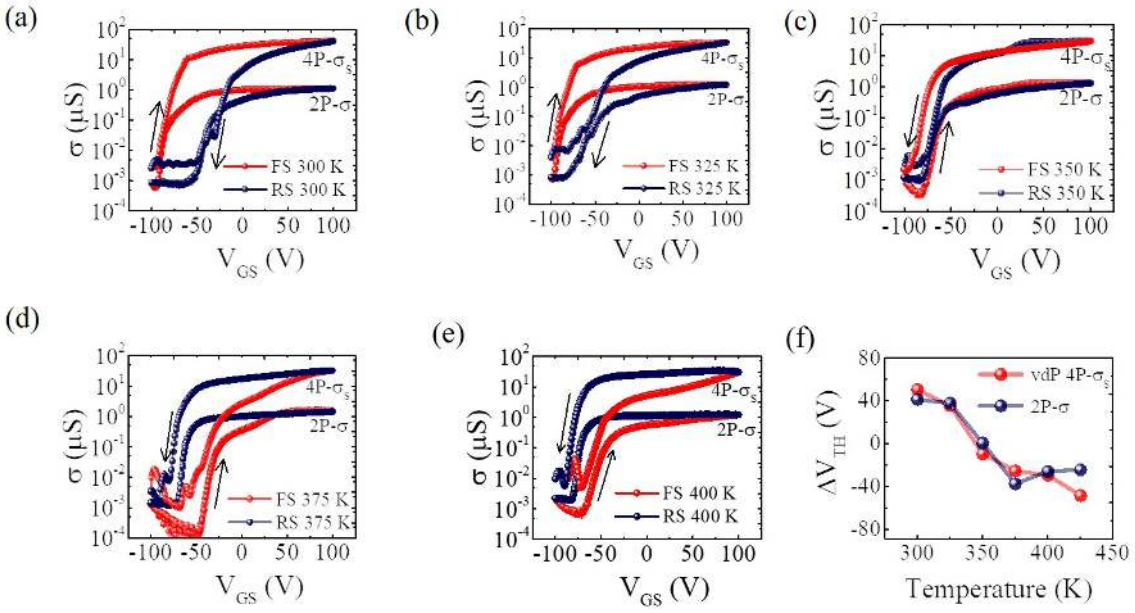

FIG. S6. Two-terminal (2P) and 4-terminal (4P) transfer characteristics of MoS_2 transistor for varying temperature values (300-400 K), (a-e) show clockwise hysteresis at 300 K to anticlockwise hysteresis at 400 K. (f) ΔV_{Th} for 2 and 4-terminal device with temperature. Almost no change in ON current (at +100 V) of both 2− and 4− terminal devices with temperature suggests little effect of temperature on the contact resistance.

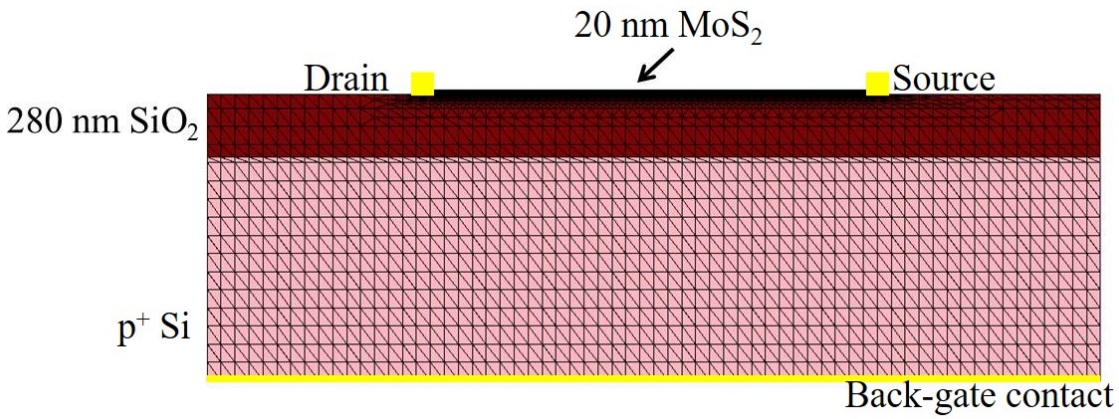

FIG. S7. Device structure used in TCAD simulations.

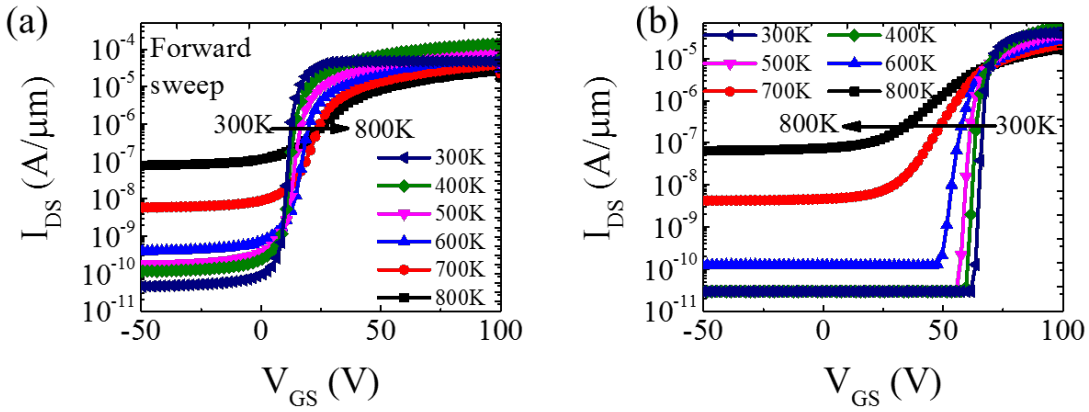

FIG. S8. Simulation results show transfer characteristics with (a) threshold voltage shift to the right with increase in temperature during forward sweep, (b) threshold voltage shift to the left with increase in temperature during reverse sweep.

DEVICE STRUCTURE USED IN SIMULATIONS

The proposed intrinsic and oxide trap models used to explain hysteresis phenomena such as hysteresis crossover and inversion were validated using simulations. Figure S7 shows the device structure used in TCAD simulations. We have used a back-gated FET similar to the fabricated device for hysteresis simulations at different temperatures. Figures S8a and b show the effect of intrinsic traps (2×10^{18} cm^{-3}) on variable temperature transfer characteristics in forward and reverse sweep, respectively. In the forward sweep $I-V$ curves shift towards the right with an increase in temperature as seen in Figure S8a. Whereas in

reverse sweep, $I-V$ curves shift towards the left with increasing temperature as shown in Figure S8b.

Oxide traps used for the simulations are taken to be spread uniformly across the thickness of the oxide for ease of simulation. The net amount of oxide charge can be estimated based on the centroid of the charge distribution. According to the proposed model, the charge centroid will be near the p^+- Si gate and hence the net charge required would be larger than the value used in the simulations.

APPLICATION: MEMORY AND TEMPERATURE SENSOR

We demonstrate two possible applications using thermally assisted hysteresis inversion in MoS_2. Firstly, the hysteresis transfer curve shown in Figure S9a can be exploited for non-volatile memory applications. Figure S9b shows a device working as a memory at 375 K. As the hysteresis is due to charge trapping/detrapping that requires significant change in temperature or bias to change, it is possible to have steady-state charged or discharged states for the intrinsic traps in MoS_2 or oxide traps in SiO_2 which can be used as '0' and '1' states of a memory device. The voltage waveform depicting read and write actions for both '0' and '1' states along with the corresponding conductance waveform are shown in Figure S9b. Reset and write voltages are chosen to be far apart and there is a large distinction in the low conductance read '0' and high conductance read '1' states.

This device can also be used as a temperature sensor. Figure S9c shows $\Delta\sigma_S$ for varying V_{GS} at different temperatures that has been mapped to the operating temperature at V_{GS}=0 V in Figure S9d. Note that $\Delta\sigma$ at 350 K increases for $V_{GS} > 0$ V due to transfer of trapped oxide charges back to the gate. Similar trend is also shown in Figure 2c of the main manuscript, where σ_{FS} increases and crosses σ_{RS} for $V_{GS} > 0$ V. However at higher temperatures (i.e. 375 K and 400 K) σ_{FS} increases but does not cross σ_{RS} due to a large difference between them. Further, hysteresis inversion facilitates a larger working temperature range for these devices compared to previous reports where hysteresis collapses after a particular temperature.

Thermally assisted memory has been demonstrated using anti-clockwise hysteresis at 375 K in the main manuscript. Here we show how hysteresis inversion can be exploited to realize a reduction in read power dissipation for heavy-'0' and heavy-'1' storage applications.

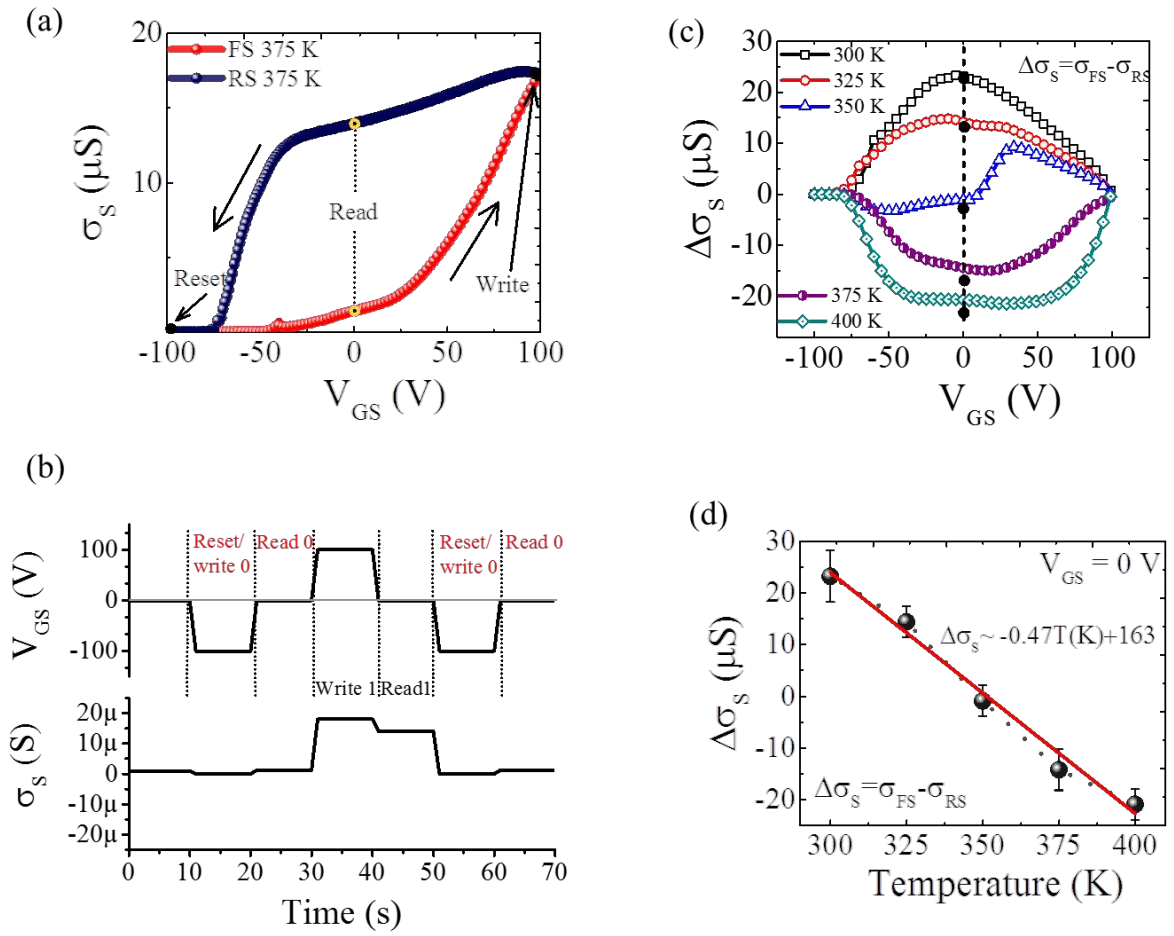

FIG. S9. (a) Hysteresis transfer curve at 375 K for a programmable memory application. (b) The upper plot shows the V_{GS} sequence for read and write actions for both '0' and '1' states, while the lower one shows the resulting variation of the sheet conductance measured in response to the V_{GS} sequence. (c) Sheet conductance difference ($\Delta\sigma_S$) between forward and reverse sweeps for varying V_{GS} and temperatures (300-400 K), (d) $\Delta\sigma_S$ at zero gate voltage for varying temperature that can be used for a look-up table based temperature sensor.

Heavy-'0'/'1' refers to applications where the occurrence of one state is more frequent than the other. Depending on the operating conditions (heavy-'0' or heavy-'1'), one can assign an operating temperature for the device which has lower read conductance for the most occurring state ('0' or '1'). For example, in case of the devices presented in this work, heavy-'0' and heavy-'1' conditions can be operated at 375 K and 300 K respectively as shown in Figure S10 to achieve low read power dissipation.

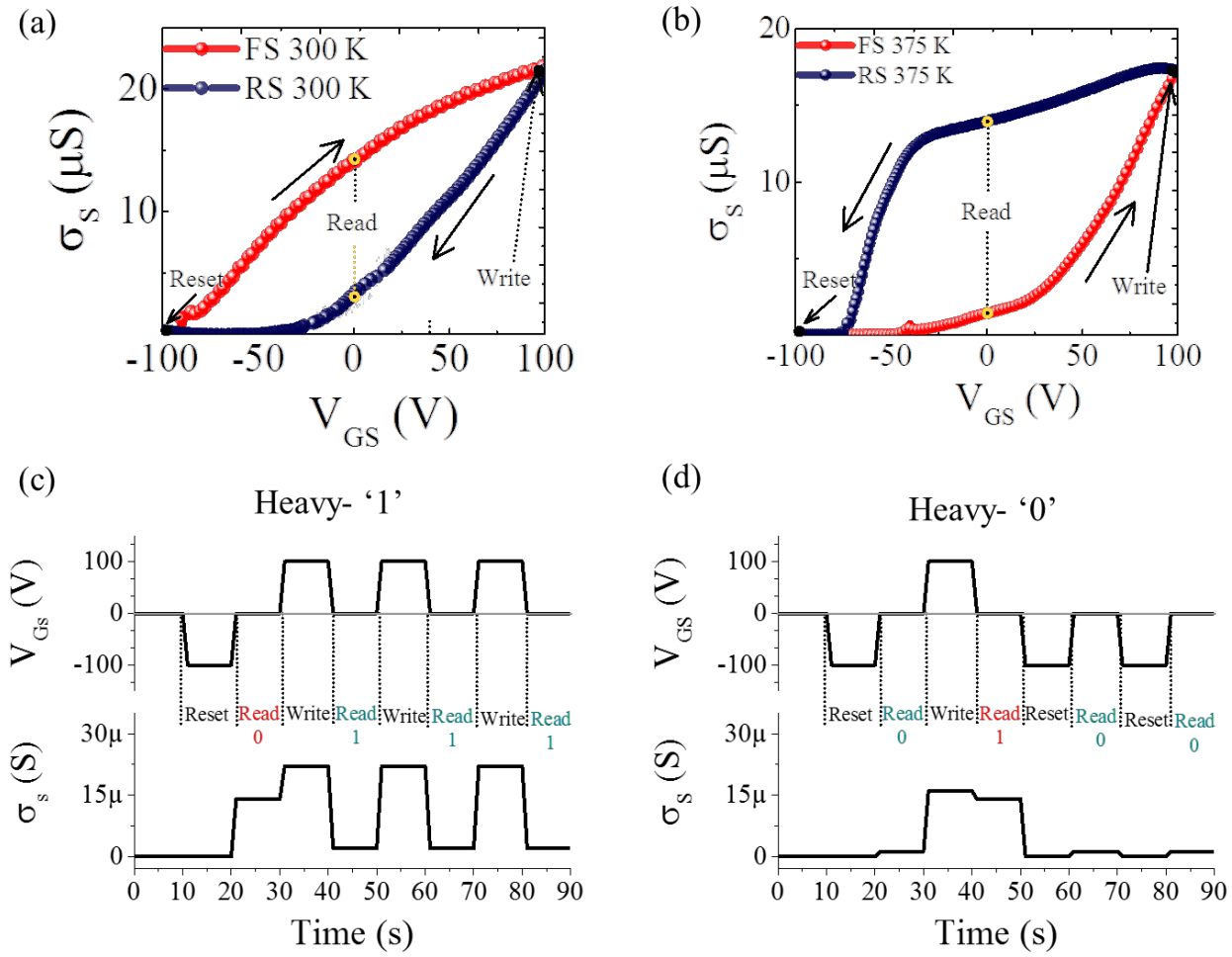

FIG. S10. Thermally assisted reconfigurable memory operation using reversible hysteresis inversion. The $\sigma_s - V_{GS}$ characteristics at (a) 300 K and (b) 375 K used to implement the memory function shown in (c,d). (c,d) The upper plot shows the gate voltage sequence applied to the device while the lower one shows the resulting variation of the sheet conductance measured in response to this sequence for 300 K and 375 K respectively.

REFERENCES

[1]Mackenzie, D. M. A.; Buron, J. D.; Whelan, P. R.; Jessen, B. S.; Silajdzic, A.; Pesquera, A.; Centeno, A.; Zurutuza, A.; Boggild, P.; Petersen, D. H. Fabrication of CVD graphene-based devices via laser ablation for wafer-scale characterization. *2D Materials*, **2**, 045003 (2015).

[2]Pauw, L. V. D. A method of measuring the resistivity and Hall coefficient on lamellae of arbitrary shape. *Philips Tech. Rev.*, **20**, 220–224 (1958).

[3]Mackenzie, D. M. A. et al. Quality Assessment of CVD Graphene: continuity, uniformity

and accuracy of mobility measurements. *Nano Research*, (2017)