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Christopher D. Yerino, Baolai Liang, Diana L. Huffaker, et al.

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REVIEW ARTICLE

Review Article: Molecular beam epitaxy of lattice-matched InAlAs and InGaAs layers on InP (111)A, (111)B, and (110)

Christopher D. Yerino
Department of Electrical Engineering, Yale University, New Haven, Connecticut 06520

Baolai Liang and Diana L. Huffaker
California NanoSystems Institute and Department of Electrical Engineering, University of California, Los Angeles, California 90095

Paul J. Simmonds[a)]
Department of Physics and Micron School of Materials Science and Engineering, Boise State University, Boise, Idaho 83725

Minjoo Larry Lee[b)]
Department of Electrical Engineering, Yale University, New Haven, Connecticut 06520 and Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801

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For more than 50 years, research into III–V compound semiconductors has focused almost exclusively on materials grown on (001)-oriented substrates. In part, this is due to the relative ease with which III–Vs can be grown on (001) surfaces. However, in recent years, a number of key technologies have emerged that could be realized, or vastly improved, by the ability to also grow high-quality III–Vs on (111)- or (110)-oriented substrates These applications include: next-generation field-effect transistors, novel quantum dots, entangled photon emitters, spintronics, topological insulators, and transition metal dichalcogenides. The first purpose of this paper is to present a comprehensive review of the literature concerning growth by molecular beam epitaxy (MBE) of III–Vs on (111) and (110) substrates. The second is to describe our recent experimental findings on the growth, morphology, electrical, and optical properties of layers grown on non-(001) InP wafers. Taking InP(111)A, InP(111)B, and InP(110) substrates in turn, the authors systematically discuss growth of both $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$ on these surfaces. For each material system, the authors identify the main challenges for growth, and the key growth parameter–property relationships, trends, and interdependencies. The authors conclude with a section summarizing the MBE conditions needed to optimize the structural, optical and electrical properties of GaAs, InAlAs and InGaAs grown with (111) and (110) orientations. In most cases, the MBE growth parameters the authors recommend will enable the reader to grow high-quality material on these increasingly important non-(001) surfaces, paving the way for exciting technological advances. © *2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).*
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I. INTRODUCTION

A. Motivation

III–V semiconductor layers grown on (111) and (110) surfaces offer a number of distinctive properties compared to those grown on (001) wafers. Examples include a unique alignment of the internal piezoelectric field, access to different zones of the electronic band-structure, compatibility with novel electronic materials, and different barriers to dislocation nucleation. Despite an initial surge of interest in the 1980s and 1990s, current understanding of growth on these orientations remains much less mature in comparison to growth on (001) surfaces. However, novel device opportunities continue to emerge whose realization depends on the ability to grow high quality (111) and (110) materials. In light of this recent resurgence of interest in (111) and (110) materials, a comprehensive review of the growth of III–V semiconductors with these orientations is long overdue.

The emerging applications that follow critically depend on growth on either the (111) or (110) surface for their success.

1. III–V field-effect transistors

(111)-oriented III–Vs have been proposed as a promising channel material for the scaling of *n*-channel metal-oxide-

[a)]Electronic mail: paulsimmonds@boisestate.edu
[b)]Electronic mail: mllee@illinois.edu

semiconductor field-effect transistors (MOSFETs). III–Vs offer higher electron mobilities (μ_n) than silicon for increased drive current. However, III–V conduction bands typically have a low density-of-states (DOS), which reduces the sheet carrier density and may hinder the drive current in what is termed the "DOS bottleneck."[1] A proposed solution is to create III–V MOSFETs on the (111) surface to access the L-valleys for electron transport.[2] The L-valleys of III–V semiconductors offer both high DOS and high injection velocities. Through the appropriate application of quantum confinement,[3–8] strain,[4–6] and III–V materials with low L-Γ valley separation,[3] conduction in the L-valleys can occur in parallel with the Γ-valley, resulting in large drive currents. In particular, thin layers of GaAs (111) and GaSb (111) are predicted to have superior drive currents compared to Si.[3,4,7,8] One proposed device structure relies on the growth of a tensile strained GaAs quantum well on InP(111),[4,6] a material system that has been successfully grown for novel (111) quantum dots[9,10] (described later in this section). Fabrication of a III–V MOSFET using these strategies has yet to be demonstrated, and its realization relies on the growth of high quality III–Vs on (111) surfaces. Advances in the growth of (111) InGaAs, InAlAs, and GaAs that are discussed in this work will assist with development of new MOSFET designs. The general trends identified may be applicable to other III–Vs useful for MOSFETs such as GaSb.

2. Entangled photon sources

Researchers have recently shown that quantum dots (QDs) grown on (111) surfaces act as ideal sources of entangled photons for quantum information.[11] Pairs of polarization-entangled photons are emitted by the decay of biexcitons.[12,13] However, useful entangled photons can only be prepared if the QDs have negligible excitonic fine-structure splitting (FSS), which is difficult to achieve in QDs on the (001) surface.[14] Low FSS requires high symmetry of the QD electronic states, which can only be reliably produced when the piezoelectric field is normal to the QDs, i.e., on the (111) surface.[15,16] Growth of (111) QDs is a significant challenge, which has been addressed using etch-pit-assisted growth,[11,17] droplet epitaxy,[18–21] and recently tensile-strained self-assembly (described below).[10] All of these (111) QD growth methods result in very low FSS compared to (001) QDs. These techniques require a deep understanding of growth on (111) surfaces, both to grow high quality buffer layers as a template for QD growth, and to understand the complex process of self-assembly on (111) surfaces.

3. Tensile quantum dots

Our groups have recently shown that (110) and (111) surfaces are ideal candidates for a new class of quantum dot (QD) grown under tensile strain. QDs have previously been limited to compressively strained Stranski–Krastanov growth or unstrained droplet epitaxy. This is because QDs grown on (001) surfaces under tensile strain tend to readily nucleate dislocations.[22,23] In addition, QD growth has focused largely on the (001) surface, since previous attempts at compressively strained growth on (111) and (110) surfaces also resulted in highly dislocated material without QD formation.[24–26] Instead, we have shown that combining tensile strain *and* a (110) or (111) surface inhibits dislocation formation in QDs.[27] This principle has enabled us to demonstrate high-quality tensile GaAs/InAlAs and GaP/GaAs nanostructures on both (110) and (111) surfaces.[9,21,28–30] Since tensile strain can strongly reduce semiconductor bandgaps,[9,30] tensile QDs on these surfaces are promising for optoelectronic devices operating at long wavelengths. Moreover, tensile GaAs/InAlAs QDs grown on (111) surfaces are perfectly suited to entangled photon generation due to their high electronic symmetry.[10]

4. Spintronics

(110) materials are of current interest for spintronics, due to the long spin-lifetime observed in (110) quantum wells relative to those on (001).[31,32] This property has enabled a number of advances in spintronics to be made using (110) quantum wells, including gate-control of relaxation time,[33] low-voltage spin manipulation,[34] spin-injected light emitting diodes,[35] and spin-injected lasers.[36] For spintronic applications, smooth interfaces are essential for maximizing spin-lifetimes,[33,37] but III–V materials grown on (110) surfaces are often rough. Improvements in both interface and material quality of (110) III–Vs will thus enhance the performance of spintronic devices. For example, the optimization of high-quality InP-based materials on the (110) surface, as described in this paper, could potentially enable the creation of spintronic devices operating at telecom wavelengths.[38]

5. Topological insulators

(111)-oriented III–Vs have been identified as useful templates for the growth of V_2–VI_3 topological insulators (TIs), including Bi_2Se_3, Bi_2Te_3, and Sb_2Te_3. The hexagonal crystal symmetry of the V_2–VI_3 TIs is better matched to the (111) plane of zinc-blende materials than to the (001) plane. High quality TIs have been grown on both GaAs(111)[39,40] and InP(111)[41–45] substrates. InP(111) has only 0.16% lattice mismatch with Bi_2Se_3. Bi_2Se_3 grown on InP(111) therefore has superior crystalline domain size and defect density to Bi_2Se_3 grown on GaAs(111),[41,46] and both substrates produce better Bi_2Se_3 crystalline quality than growth on Si(111).[44,45] Advances in (111) III–V growth, particularly on InP, are likely to further improve TI quality and allow the integration of TIs with III–V devices.

6. Transition metal dichalcogenides

Growth on (111) III–Vs also offers a promising route for the synthesis of transition metal dichalcogenides (TMDs). TMDs can be grown in 2D monolayer or multilayer forms, and offer a broad range of properties, including semiconductivity,[47,48] metallicity,[49] and superconductivity.[50] Novel electronic and optoelectronic devices have been demonstrated based on TMDs, such as field-effect transistors,[51] phototransistors,[52] and tunable $p-n$ junctions.[53] The

development of TMD devices typically relies on exfoliation,[51] which is challenging to scale to wafer-level synthesis. In contrast, the epitaxial growth of TMD layers on GaAs(111) was reported many years ago, due to the unique termination of (111) surfaces.[54] TMD materials are composed of 2D layers weakly connected by van der Waals bonds. High-quality layers can hence be grown if the substrate only interacts to support the TMD via van der Waals forces.[55] The GaAs(111) surface is ideal for this purpose. Exposure to group-VI atoms, including sulfur, selenium, and tellurium, passivates the specific arrangement of dangling bonds found on (111) surfaces.[55] Renewed interest in TMDs has led to recent molecular beam epitaxy (MBE) growth demonstrations of wafer-scale monolayer $MoSe_2$ on GaAs(111)B (Ref. 56) as well as $MoTe_2/MoSe_2$ superlattices on GaAs(111)B with monolayer precision.[57] Smooth GaAs(111)B buffer layers help facilitate the subsequent TMD growth.[56] By understanding the growth of (111) III–V materials, new opportunities will arise for the integration of III–V and TMD devices.

B. Challenges in III–V growth on (111) and (110) substrates

The above examples highlight the growing demand for high-quality III–Vs on (111) or (110) substrates. However, ideal conditions established for growth of III–Vs on (001) surfaces often produce poor material quality on (111) and (110) orientations. To date, growth on (111) and (110) surfaces has largely focused on GaAs and AlGaAs. Growth of GaAs/AlGaAs (111) and (110) is much more difficult than growth of GaAs/AlGaAs (001), often resulting in large surface roughness, and poor electrical and optical properties. Nevertheless, by carefully exploring growth conditions, smooth surfaces with favorable electrical and optical properties have been demonstrated. However, very little information is available for growing other III–Vs with (111) or (110) orientations, in particular for the technologically useful materials InGaAs or InAlAs grown on InP. This lack of a growth–optimization toolbox means that the electrical, optical, and crystallographic quality that is achievable in (111) and (110) materials is currently insufficient to meet the demands of the novel applications described above.

The atomic force microscope (AFM) images in Figs. 1(a)–1(e) show that surface roughening is the primary challenge for growth of (111) and (110) epilayers. Buffers grown on (111)A, (111)B, and (110) surfaces tend to form a high density of unwanted features. Most prominent among these are "hillocks" [the large 3D islands in Figs. 1(a) and 1(e)],[58–64] and "pits" that arise from step bunching, particularly on offcut substrates [Fig. 1(c)]. To avoid hillock formation, many groups have adopted the use of offcut substrates, which promote step flow growth rather than 3D islanding,[58,65–68] but the optimization of growth conditions is seldom reported, and smooth growth remains challenging.[69–71] Furthermore, much of the early work on (110) and (111) growth was performed prior to widespread availability of commercial AFMs and so morphology studies were often limited to optical microscopy. The effect of growth conditions on atomic-scale morphology therefore remains largely unknown for most materials on non-(001) surfaces.

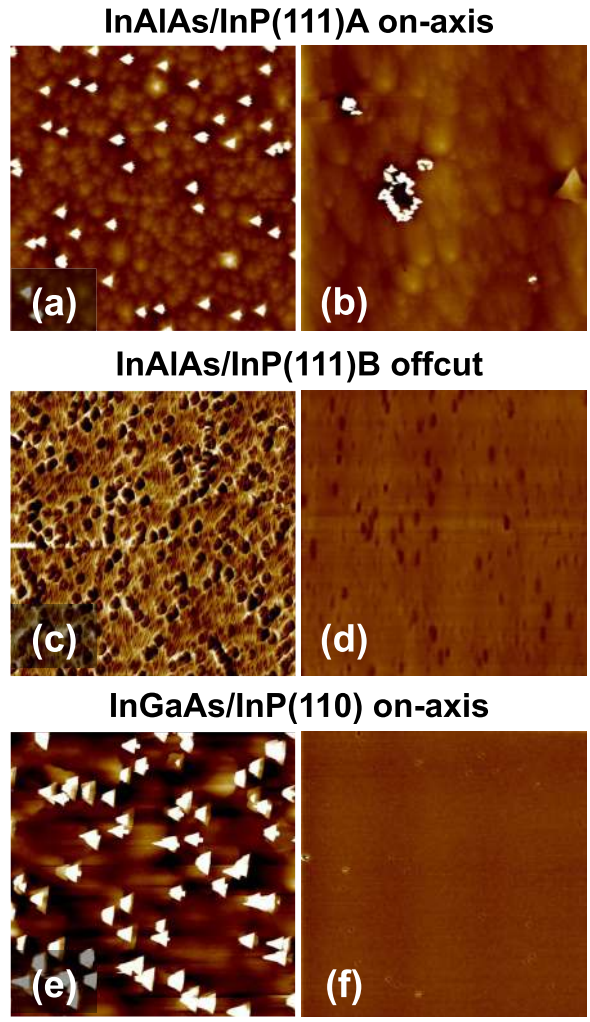

FIG. 1. (Color online) AFM images ($15 \times 15\,\mu m^2$, 15 nm z-scale) showing surface morphology of InAlAs on exact InP(111)A, InAlAs on offcut InP(111)B, and InGaAs on exact InP(110). (a), (c), and (e): Growth under nonoptimized conditions typically leads to rough surface morphologies. (b), (d), and (f): Optimized growth conditions arrived at in this work produce significantly smoother surfaces.

The purpose of this paper is twofold: first, to provide a comprehensive review of the literature surrounding growth on (111) and (110) surfaces; and second to fill in the gaps in the literature with new experimental data. The experimental work we present here focuses on the effect of growth conditions on material properties for InAlAs and InGaAs grown on InP (111)A, (111)B, and (110) with an emphasis on achieving smooth surface morphology. Challenges for homoepitaxy on InP (111)A and (111)B are also discussed. We show that each substrate orientation requires a different growth strategy to optimize material properties, which typically differs greatly from what is used for growth on the (001) face.

The paper is divided into separate sections describing growth on exact InP(111)A (Sec. III), offcut InP(111)B (Sec. IV), and exact InP(110) (Sec. V). Each section begins

with a review of epitaxy for GaAs and other III–Vs on each of these orientations, which informs new growth strategies for InAlAs and InGaAs on InP explored in this work. In Sec. VI we compare and summarize growth across the different surface orientations.

We show that by careful selection of the growth conditions, it is possible to eliminate, or greatly mitigate, morphological defects on each orientation, resulting in atomically smooth surfaces [Figs. 1(b)–1(f)]. We present experimental data showing how the electrical and optical properties of these materials depend on growth conditions. We use trends in surface morphology, electrical and optical properties to identify optimal parameters for the growth of these alloys, and discuss cases where jointly optimizing all of these material properties is challenging. Taken together, this work offers a comprehensive guide to overcoming obstacles to III–V material growth on (110) and (111)-oriented InP substrates.

II. EXPERIMENT

For the new results presented in this work, samples were grown in a VEECO Modular GEN II solid-source MBE, using P_2 and As_4 as the group-V sources. As_4 was selected instead of As_2 for consistency with the body of literature on (111) and (110) III–V growth; many growth studies in the literature predated the widespread availability of the valved arsenic cracker for producing As_2, and hence used the As_4 species. Our fluxes were estimated using a beam flux monitor (BFM) located at the growth position. We calculated V/III flux ratios directly from BFM readings without sensitivity corrections. Growth temperatures T_g were measured by optical pyrometer for $T_g \geq 400\,°C$. For $T_g < 400\,°C$, we measured temperature using a thermocouple located behind the substrate. We estimate that our thermocouple values are ~20–30 °C lower than the true values for $T_g < 400\,°C$.

Wafers used in this study were all semi-insulating and included the following orientations: on-axis InP(110), on-axis InP(111)A, and vicinal InP(111)B offcut 2° toward $\langle 2\underline{11} \rangle$. (110) and (111)A substrates were supplied by AXT, and (111)B substrates were supplied by SWI. All substrate orientations were specified to within ±0.5° by the manufacturers. Substrates were also specified as epiready, and no wet chemical treatment was performed, unless otherwise noted. Cleaved pieces were mounted on 4 in. diameter silicon handle wafers using high-purity molten indium as an adhesive.

The conditions used for growth on (111)A, (111)B, and (110) InP are detailed in the corresponding sections of this paper. InAlAs growths on different InP surface orientations were performed separately. InGaAs samples were grown at a fixed rate of 0.17 μm/h by coloading (110), (111)A, and (111)B InP wafers onto the same backing wafer and testing growth conditions on the three samples simultaneously. *In situ* desorption of the native oxide was performed under P_2 or As_4; our choice of deoxidation species was partially based on the availability of P_2 in our MBE system and does not necessarily reflect a preference for a particular species. Unless otherwise noted, comparisons in this study are only made between samples where the same oxide desorption procedure was used. Single layers of lattice-matched $In_{0.52}Al_{0.48}As$ or $In_{0.53}Ga_{0.47}As$ were directly deposited on the InP substrate to investigate material properties. We confirmed lattice-matching of alloy compositions to the InP with x-ray diffraction (XRD). Hereafter, the terms InAlAs and InGaAs refer to epilayers with alloy compositions lattice-matched to InP.

Surface morphology was characterized using Nomarski microscopy and AFM (Digital Instruments Nanoscope IIIa). Photoluminescence spectroscopy (PL) was performed with a 532 nm pump laser, an InGaAs detector for InGaAs samples, and a Si detector for InAlAs samples. Hall effect measurements were performed on InGaAs samples using the van der Pauw method to determine background electron density, n_0, and electron mobility, μ_n. We used indium solder to create electrical contacts for Hall measurements. To ensure Ohmic behavior, we gently annealed the contacts with the soldering iron until the indium wet the surface. Hall measurement was not possible for most InAlAs samples, due to the rapid formation of insulating oxides in air and resulting high contact resistances. Transmission electron microscopy was performed in either cross-section (X-TEM) or plan-view (PV-TEM) using a FEI Osiris operating at 200 kV.

III. GROWTH ON InP (111)A

A. Review of growth on (111)A surfaces

Previous reports of III–V epitaxy on (111)A surfaces focused almost exclusively on GaAs, with very little work describing growth trends for other materials. As discussed above, the primary challenge for growth on (111)A is the formation of a high density of hillocks under a wide range of growth conditions.[58,59,72] The hillocks are threefold symmetric and take the form of either a pyramid triplet with three mounds that are bounded by {010}-related facets, or a single triangular pyramid bounded by {110}-related facets.[73]

Hillock formation is eliminated using a substrate offcut by ≥5° toward (100),[58,65] but it is also possible to grow smooth GaAs on on-axis (111)A substrates under certain growth conditions. Earlier reports showed decreasing hillock size and increasing hillock density with low T_g and high V/III ratio, enabling hillock removal by shrinking them to zero size.[58,59] In addition, Sato *et al.* found that the presence of hillocks was related to arsenic-limited growth regimes.[59] Their group showed from reflection high-energy electron diffraction (RHEED) intensity oscillations that the GaAs(111)A growth rate was arsenic-limited rather than gallium-limited at high T_g and low V/III,[74] and this behavior was attributed to a low arsenic sticking coefficient for the (111)A surface. The arsenic-limited regime was shown to be closely correlated to hillock formation, suggesting that hillocks are related to excess Ga on the surface.[59] During growth on (111)A substrates, researchers have observed surface defects arising from growth on both (100)- and (110)-related facets.[73] We hypothesize that if they offer higher arsenic sticking coefficients than (111)A, it is possible that preferential growth on these facets could lead to hillock

formation. Substrate cleaning and control of ambient arsenic levels prior to growth have also been suggested as techniques to promote smooth epitaxy.[73]

The surface morphology of GaAs(111)A has been surveyed extensively by Nomarski and scanning electron microscopy, but little has been published regarding its morphology at the atomic-level. According to RHEED, GaAs(111)A exhibits a (2×2) reconstruction before, during, and after growth, across virtually all T_g values.[72] The (2×2) reconstruction has been studied by scanning tunneling microscopy (STM), and arises from periodic gallium vacancies on the GaAs(111)A surface.[75] These Ga-vacancies are expected to appear under the Ga-rich conditions common to GaAs(111)A growth, based on *ab initio* theoretical calculations.[76] However, the effect of growth conditions on the atomic terrace morphologies of InP(111)A and its lattice-matched InGaAs and InAlAs buffers remain largely unexplored. Sections III B–III E address this gap in the literature.

B. InP(111)A homoepitaxy

We performed preliminary work on InP(111)A homoepitaxy, to determine if growing InP buffers on InP(111)A substrates before heteroepitaxy would lead to smoother surfaces. In fact, both InAlAs and InGaAs grown on bare InP(111)A substrates were smoother than when grown on InP(111)A homoepitaxial buffers (see Secs. III C and III D). Substrate deoxidation and InP growth were both performed using P_2, followed by InP growth at 0.26 μm/h. Similar to GaAs(111)A homoepitaxy, InP(111)A [as well as InGaAs(111)A and InAlAs(111)A discussed in Secs. III C–III E] exhibits a (2×2) streaky RHEED pattern during growth.[72,75]

The effect of native oxide desorption temperature and T_g on InP homoepitaxy is shown in Fig. 2. Both sample surfaces in Fig. 2 were covered with triangular faceted features that are gradually sloped on one side and vertically sloped on the two adjoining sides. The vertical slopes produced pronounced discontinuities across the growth surface, which appear as narrow trenches at the foot of the faceted structures. Lower T_g and desorb temperatures caused the hillocks to increase in density and decrease in size. Under such conditions, the trench-features subsided and smoother regions appeared between the hillocks.

We attempted to use V/III ratio to lower the hillock density, but no effect was observed in the range V/III = 40–80. Substrates etched in H_2SO_4:H_2O_2:H_2O followed by a bromine-methanol etch produced very similar growth morphologies to untreated epiready substrates (not shown), confirming that the hillocks are not induced by substrate preparation. As discussed in Secs. III C–III E for InAlAs and InGaAs growth on InP(111)A, very high and very low T_g appear most promising for smooth growth. Such strategies may also yield smooth InP homoepitaxy, but further work is needed to demonstrate atomically smooth InP(111)A homoepitaxy on exact substrates.

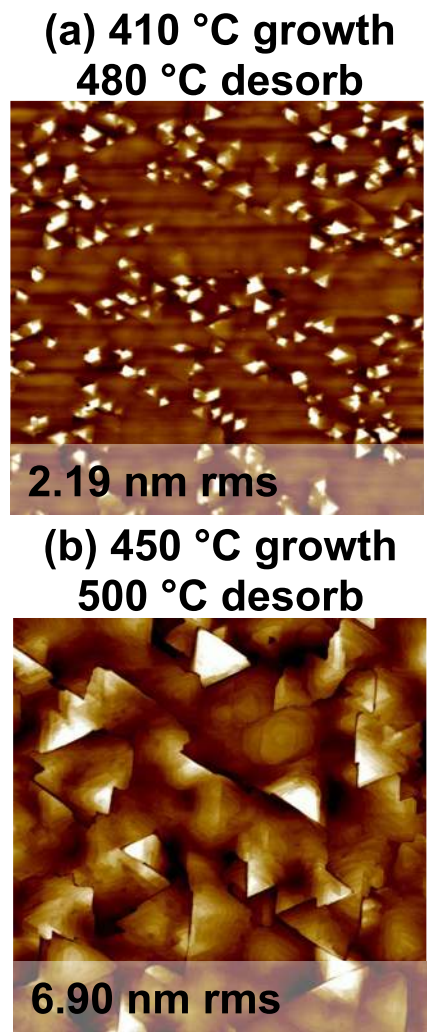

FIG. 2. (Color online) AFM images ($5 \times 5\,\mu m^2$, 30 nm z-scale) showing morphology of InP(111)A for different T_g and deoxidation temperatures. Rms roughness values averaged over 225 μm^2 include roughening due to hillocks.

C. InAlAs on InP(111)A

1. InAlAs(111)A: Surface morphology

In this section, we present new results on surface morphology optimization of InAlAs grown directly on exact InP(111)A substrates without an InP buffer. Pyramidal hillocks are the primary challenge for InAlAs and InGaAs growth on InP(111)A [Fig. 1(a)]. The reduction or elimination of hillocks for InAlAs and InGaAs on exact InP(111)A was found to be more difficult than growth on offcut InP(111)B (Sec. IV) or exact InP(110) (Sec. V). The triangular hillocks were typically ~500 nm wide and ~50 nm tall with densities ranging from the mid-$10^6\,cm^{-2}$ to the mid-$10^7\,cm^{-2}$. In addition, the smoother region between the hillocks consisted of atomic "wedding cakes," where monolayers of concentric 2D islands appeared, rather than step flow growth. Such wedding cakes form when adatoms nucleate new 2D islands on top of existing ones, rather than attaching to the sides of other islands; similar wedding cake features form during MBE growth of certain other III–V materials including GaSb(001).[77] We characterized the

roughness attributable to the wedding cakes by measuring rms roughness values in regions free of hillocks (unless otherwise noted). InP(111)A oxide desorption was performed under either As_4 or P_2, followed by growth of 100–200 nm of InAlAs.

First, we show the effect of As_4 versus P_2 overpressure during InP native oxide desorption (Fig. 3) where a beam equivalent pressure of 1.1×10^{-5} Torr was used for both species. When InAlAs was grown under the same, near-optimal T_g and V/III conditions, the P_2 desorb produced ~40% fewer hillocks on the surface than the As_4 desorb. Surface roughness between the hillocks also improved by switching from As_4 to P_2 (Fig. 3). The AFM images show that using P_2 during the oxide desorption produces a triangular step-flow morphology, which better reflects the (111) crystal symmetry than the almost-circular wedding cakes observed when As_4 is used. Desorbing the native InP oxide under arsenic produces monolayers of compressive $InAs_{1-x}P_x$ on the surface, due to anion exchange,[78] which may explain the changes in morphology observed here. P_2 is thus recommended as the ideal species under which to desorb the InP native oxide.

As Figs. 4(c) and 4(e) show, growth rate had a pronounced effect on InAlAs(111)A morphology. Increasing the growth rate from 0.17 to 0.5 μm/h raised the hillock density by >3×. Adatom diffusion length is reduced at higher atomic flux, increasing the rate of island nucleation.[79] The lower adatom diffusion time at high growth rate allows 3D islands to form closer together, leading to a higher density of hillocks.

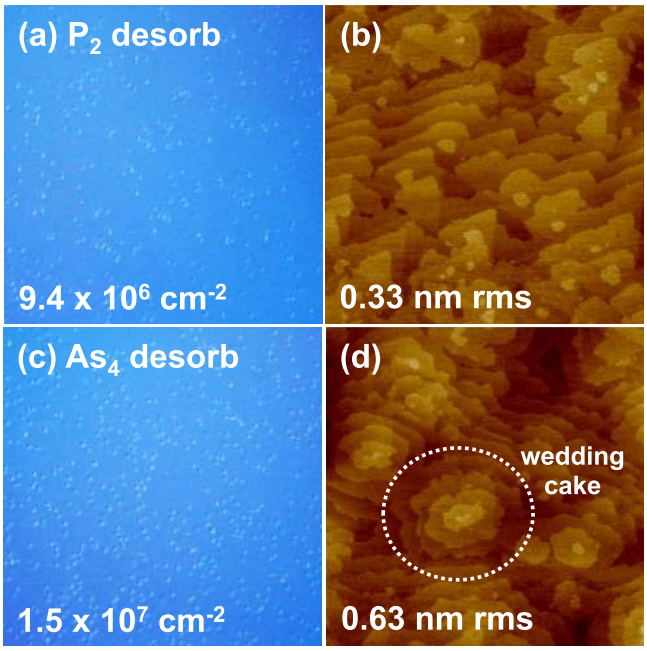

FIG. 3. (Color online) Effect of oxide desorption overpressure species on subsequent InAlAs(111)A morphology. (a) and (b): Substrates deoxidized in P_2. (c) and (d): Substrates deoxidized in As_4. (a) and (c): $50 \times 50\,\mu m^2$ Nomarski images, annotated with hillock densities. (b) and (d): $1 \times 1\,\mu m^2$ AFM images (3 nm z-scale). Rms roughness values averaged over $25\,\mu m^2$ between hillocks.

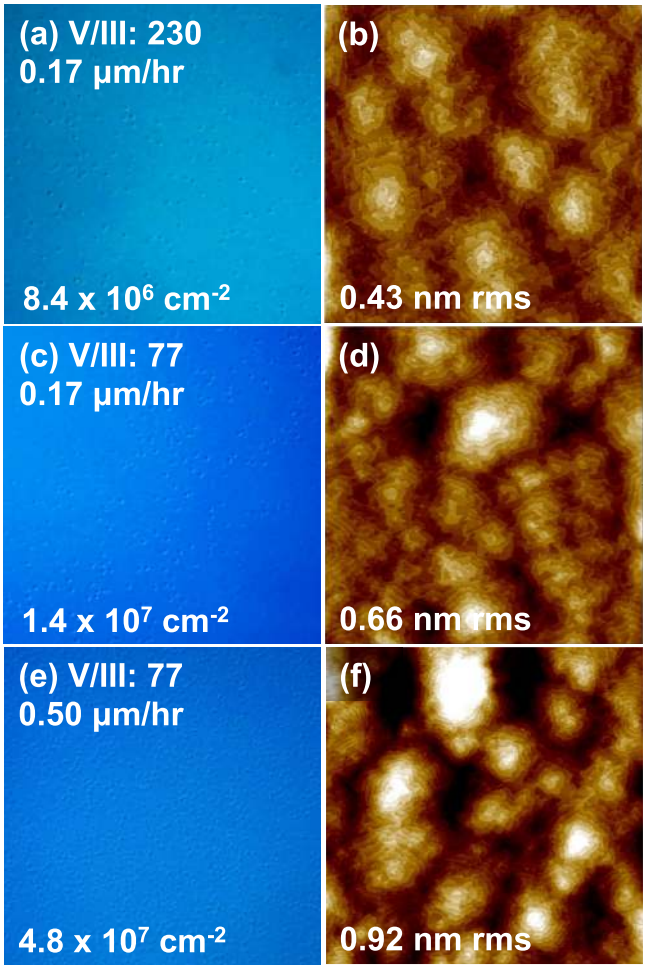

FIG. 4. (Color online) Comparison of growth rate and V/III ratio effects on InAlAs(111)A morphology for $T_g = 500\,°C$ (substrates deoxidized in As_4). Images in same row are taken from same sample. (a), (c), and (e): $50 \times 50\,\mu m^2$ Nomarski images, annotated with hillock densities. (b), (d), and (f): $2 \times 2\,\mu m^2$ AFM images (3 nm z-scale), annotated with rms roughness. Rms roughness values averaged over $25\,\mu m^2$ between hillocks.

In addition, comparison of Figs. 4(d) and 4(f) shows that a slower growth rate lowered wedding cake height, reducing rms roughness from 0.92 to 0.66 nm over a $5 \times 5\,\mu m^2$ area. Since island nucleation rates increase with adatom arrival rate, the use of higher atomic fluxes can encourage the nucleation of new 2D layers atop existing ones to promote taller wedding cakes.[79] Due to the improved atomic morphology and lower hillock density at lower growth rate, all subsequent InAlAs(111)A growths were performed at 0.17 μm/h.

Comparison of Figs. 4(a) and 4(c) also shows the effect of V/III ratio on the InAlAs(111)A morphology. Nomarski microscopy shows that increasing the V/III ratio from 77 to 230 reduced the hillock density by 40%. This similarity with GaAs(111)A growth suggests that the hillocks on InAlAs(111)A are related to limited arsenic-availability caused by a reduced arsenic sticking coefficient.[74]

The effect of reducing T_g on hillock density is shown in Fig. 5. Hillock density increased from $5.6 \times 10^6\,cm^{-2}$ at 480 °C to $8.0 \times 10^6\,cm^{-2}$ at 437 °C, while hillock size decreased rapidly, such that the volume of material in the

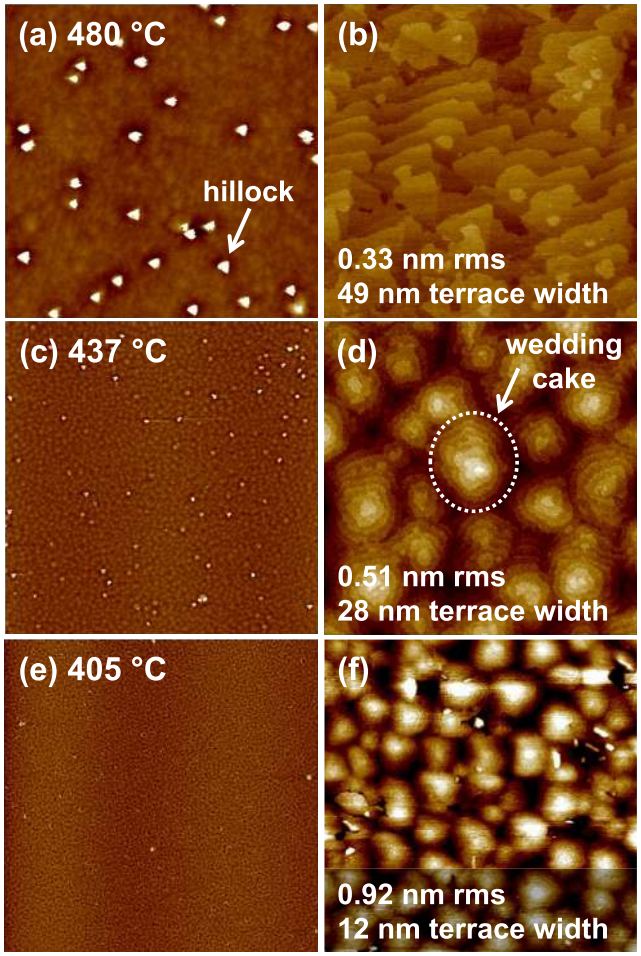

FIG. 5. (Color online) Effect of T_g on InAlAs(111)A morphology for samples grown at V/III = 230, 0.17 μm/h (substrates deoxidized in P_2.) Images in same row are taken from same sample. (a), (c), and (e): $15 \times 15\,\mu m^2$ AFM images (15 nm z-scale). (b), (d), and (f): $1 \times 1\,\mu m^2$ AFM images (3 nm z-scale), annotated with roughness and average widths. Rms roughness values averaged over 25 μm^2 between hillocks.

hillocks also decreases. At 405 °C, the hillocks were eliminated almost entirely. While the removal of hillocks encourages the use of low T_g, the atomic scale roughness shows the opposite trend. As T_g decreased, the terrace widths on the wedding cakes shrank from 49 to 12 nm on average, and the wedding cakes grew in height; rms roughness increased concomitantly from 0.33 to 0.92 nm. The relationship between T_g and wedding cake size indicates that the nucleation rate of 2D islands is lower at higher T_g due to faster detachment of adatoms from island protonuclei.[29,80–82]

New surface defects appeared in the InAlAs grown at 405 °C, including pits, hillock clusters, and irregularly shaped trenches. Close inspection of Fig. 5(f) reveals hillocks much smaller than previously observed, which form in clusters of three, arranged with threefold symmetry. The symmetric arrangement of these hillocks resembles the larger, threefold symmetric hillocks more commonly observed at high T_g, suggesting that they have the same origin. The total density of threefold symmetric defects, including larger hillocks and small hillock-clusters, was $1.0 \times 10^7\,cm^{-2}$ at 480 °C, $3.8 \times 10^7\,cm^{-2}$ at 437 °C, and $2.3 \times 10^8\,cm^{-2}$ at 405 °C. The higher density of these features with decreasing T_g shows that formation of the surface defects is regulated by adatom diffusion length. We attribute this effect to indium adatoms, given previous observations of enormous migration lengths up to ~25 μm on III–V surfaces.[83] This in turn allows the hillocks to form closer together as they compete for adatoms. Note that V/III = 230 is used for all samples in Fig. 5. The increasing distance between hillocks at higher temperature indicates that the diffusion length is still on the order of microns, even under high As-flux.

X-TEM and PV-TEM of InAlAs/InP(111)A show very few extended defects in the optimized InAlAs(111)A buffers. Figure 6(a) shows TEM images from the smoothest InAlAs(111)A samples obtained in this study [i.e., Fig. 5(a)]. Defects are only noticeable in the hillocks [Fig. 6(b)], which contain a high density of planar defects and dislocations. Thus, the hillock defects are likely to be electrically and optically detrimental: reduction in hillock density is expected to improve the overall material quality. The sample in Figs. 6(a) and 6(b) also includes a layer of InGaAs between the InAlAs and InP, the growth of which is discussed in Sec. III E. We conclude that apart from the hillocks, both InAlAs and InGaAs grow with minimal defect nucleation.

Finally, we investigated the effect of pregrowth InP substrate etching, to determine whether the hillocks are influenced by substrate preparation, as suggested by Ref. 73. An untreated epiready InP(111)A wafer was coloaded with InP pieces etched in H_2SO_4:H_2O_2:H_2O (5:1:1) followed by bromine: methanol (1:80). The wet chemical treatment reduced the hillock density from 9.4×10^6 to $5.0 \times 10^6\,cm^{-2}$,

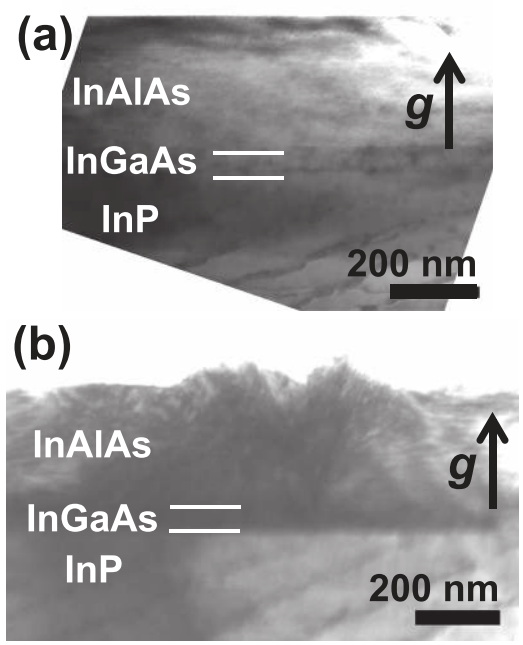

FIG. 6. Bright field X-TEM of 300 nm InAlAs/50 nm InGaAs layers grown on InP(111)A. (a) Most of the sample area is free from dislocations. (b) Hillocks in the epilayer contain high densities of dislocations and planar defects. $\boldsymbol{g} = 222$ and a ⟨110⟩ imaging zone was used.

implying that surface preparation is partially responsible for hillocks.[73]

2. InAlAs(111)A: Photoluminescence

PL from the InAlAs(111)A is influenced by T_g (Fig. 7) but is relatively insensitive to other variables. The PL spectra in Fig. 7 show the InP substrate emission at 1.34 eV, next to the InAlAs emission at 1.45 eV. As T_g was increased from 405 to 480 °C, the entire spectrum increased in intensity by 35%. The shape of the two spectra are identical, suggesting that the higher PL intensity may partially result from stronger light extraction in the 480 °C sample, due to the formation of larger hillocks. PL is largely insensitive to growth rate and V/III ratio, with nearly identical PL intensities observed across the parameters used in this study (not shown).

3. InAlAs(111)A: Summary

In summary, the hillocks prevalent during growth of InAlAs(111)A can be significantly mitigated using high T_g, very high V/III ratio, and low growth rate, but, unlike the case of GaAs(111)A,[59] it was not possible to completely eliminate them. Low T_g removed the large hillocks but only at the expense of smaller-scale surface defects and higher atomic roughness due to wedding cakes. TEM confirms that hillocks contain a high density of extended defects, so further work is needed to eliminate them. The photoluminescence of InAlAs(111)A was relatively insensitive to growth conditions, with marginal change in the intensity attributed to light extraction due to surface roughening. We favor the use of high T_g since this produces low hillock densities with smoother surfaces in-between. Provided the hillocks are low enough in density, there will be sufficiently large areas of smooth, high-quality, defect-free InAlAs in between them to suit many applications.

Overall, our recommended growth conditions for InAlAs(111)A are high T_g (≥480 °C), very high V/III ratio (∼230), and low growth rate (0.17 μm/h).

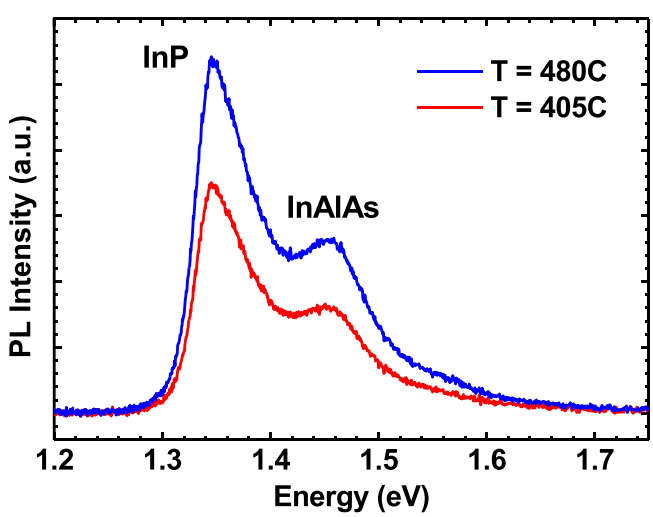

FIG. 7. (Color online) Effect of T_g on 300 K PL of InAlAs grown on InP(111)A.

D. InGaAs on InP(111)A

1. InGaAs(111)A: Surface morphology

As shown in Fig. 6, hillocks are the primary source of extended defects in both InGaAs and InAlAs, so it is highly desirable to minimize their density. In terms of controlling hillock formation and wedding cake roughness, InGaAs(111)A obeyed broadly similar growth trends to InAlAs(111)A. We grew 200 nm InGaAs layers on InP(111)A following the oxide desorb at 485 °C under 1.1×10^{-5} Torr As_4. Based on the InAlAs(111)A growth experiments in Sec. III C, we adopted a growth rate of 0.17 μm/h for InGaAs(111)A. However, we found InGaAs(111)A to be much less sensitive to growth rate than InAlAs (not shown), and we believe the following results are equally applicable at higher growth rates.

The effect of V/III ratio on InGaAs(111)A morphology is shown in Fig. 8 for samples grown at $T_g = 485$ °C. The InGaAs(111)A surface is roughened by large hillocks and very tall wedding cakes when a moderate V/III ratio of 25 was used [Figs. 8(e) and 8(f)]. A V/III ratio of ∼75 or higher

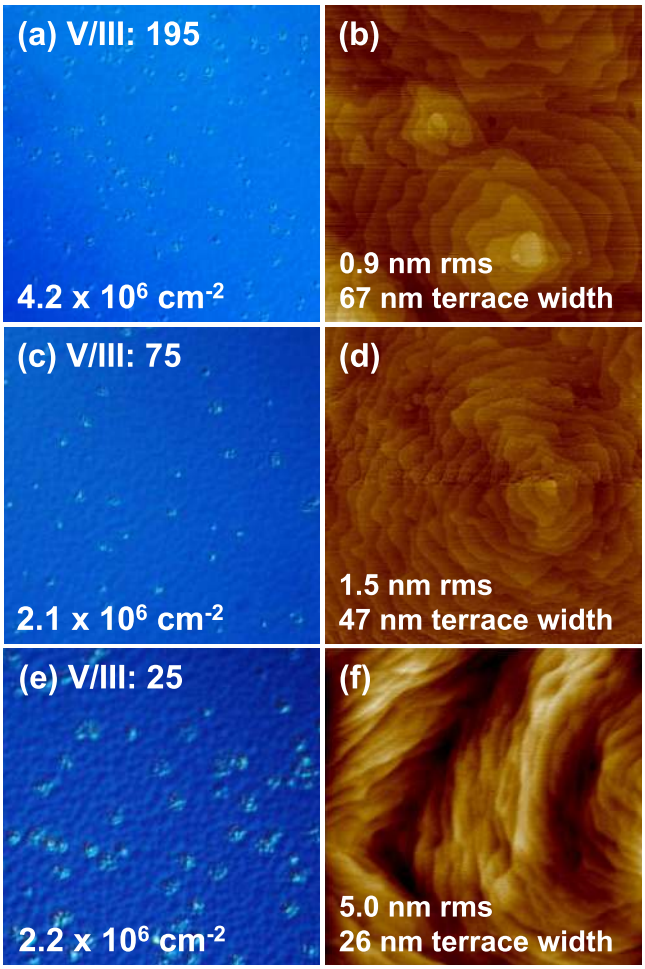

FIG. 8. (Color online) Effect of V/III ratio on InGaAs(111)A morphology for $T_g = 485$ °C. Images in same row are taken from same sample. (a), (c), and (e): $50 \times 50\ \mu m^2$ Nomarski images, annotated with hillock densities. (b), (d), and (f): $1 \times 1\ \mu m^2$ AFM images (5 nm z-scale), annotated with rms roughness and average terrace width. Rms roughness values averaged over 25 μm^2 between hillocks.

was needed to reduce hillock size [Figs. 8(a) and 8(c)] and planarize the InGaAs surface in between [Figs. 8(b) and 8(d)]. Similar to InAlAs(111)A, the InGaAs(111)A morphology at higher V/III ratio was predominantly flat with triangular hillocks scattered about the surface. However, for InGaAs growth, the hillock density was several times lower than for InAlAs growth, typically in the low to mid-$10^6\,\mathrm{cm}^{-2}$. On some samples, clusters of hillocks were observed in addition to isolated hillocks; we report hillock densities as the number of contiguous hillock clusters per unit area.

Increasing the V/III ratio from 75 to 195 doubled the hillock density, which is opposite to the trend for InAlAs(111)A and GaAs(111)A.[58,59] For InGaAs(111)A, the arsenic-limited model[29] used to explain GaAs(111)A hillocks no longer appears to be applicable. Instead, the trend for InGaAs(111)A suggests that hillock density scales with adatom diffusion length within this V/III range. The higher V/III ratio lowers the diffusion length, allowing hillocks to form closer together while competing for adatoms.

As we increased V/III ratio, atomic wedding cakes decreased in height and increased in atomic step spacing (i.e., terrace width). This effect was more pronounced than the effect of V/III ratio on InAlAs(111)A growth. V/III ratio optimization of InGaAs(111)A differs from InAlAs(111)A in that a tradeoff must be made between atomic-scale wedding cakes and larger-scale hillocks. For minimum hillock density, V/III ~75 is recommended. However, for applications where access to atomically flat surfaces is more important (e.g., QD studies), a high V/III ~195 should be used to increase the terrace widths.[10]

The effect of T_g on InGaAs(111)A morphology from 350 to 485 °C is shown in Fig. 9 at a fixed V/III of 75. As seen in Fig. 5 for InAlAs(111)A and Fig. 2 for InP(111)A, reducing T_g decreased the size and increased the density of hillocks. The hillock density increased by 3 orders of magnitude as T_g was reduced from 485 to 350 °C, confirming that hillock density scales inversely with adatom diffusion length for InGaAs(111)A. However, in contrast to InAlAs(111)A growth, low T_g could not be used to completely eliminate hillock formation. The higher adatom mobility of Ga compared to Al may make it easier for Ga adatoms to reach hillock incorporation sites, even at low T_g.

Atomic scale wedding cake formation in InGaAs(111)A was suppressed as T_g increased, lowering the rms roughness (Fig. 9). This reduction is consistent with our observations for InAlAs(111)A in Sec. III C and suggests that a reduction in the 2D nucleation rate promotes smooth growth in both cases. Increasing both T_g to 510 °C and V/III ratio to 195 yielded terraces as wide as 100 nm, with hillock densities as low as $2\times10^6\,\mathrm{cm}^{-2}$ (Fig. 12). Increasing T_g further did not yield additional surface smoothing, and the size and density of hillocks became larger for T_g near the InGaAs decomposition temperature of ~550 °C.

2. InGaAs(111)A: Electrical properties

All InGaAs(111)A samples were unintentionally *n*-type, as commonly observed for InGaAs/InP(001).[84] The

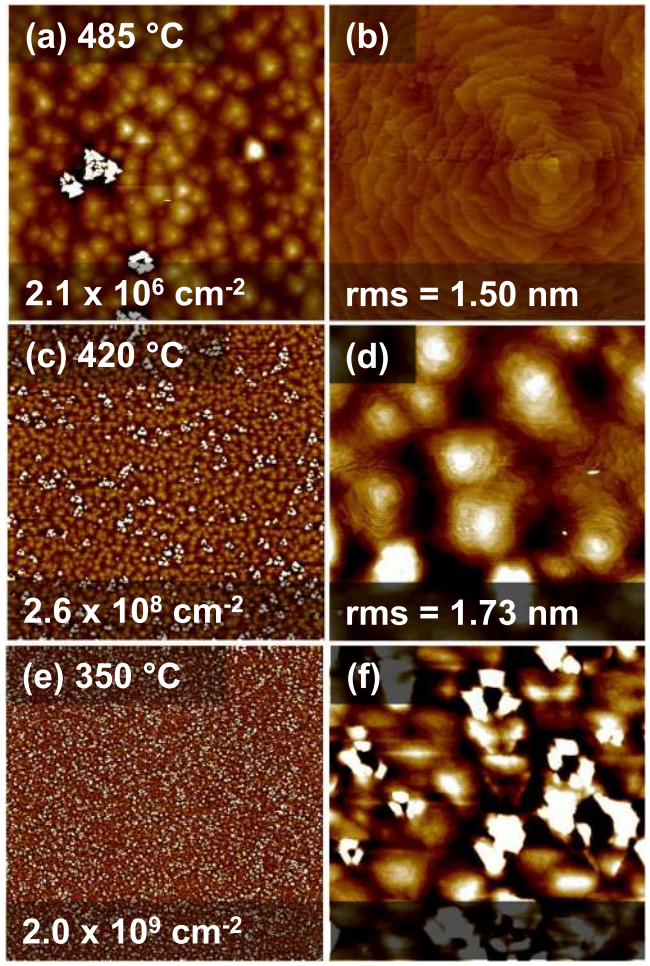

FIG. 9. (Color online) Effect of T_g on InGaAs(111)A morphology for samples grown at V/III = 75. Images in same row are taken from same sample. (a), (c), and (e): $15\times15\,\mu\mathrm{m}^2$ AFM images (15 nm z-scale). (b), (d), and (f): $1\times1\,\mu\mathrm{m}^2$ AFM images (5 nm z-scale). Rms roughness values averaged over $25\,\mu\mathrm{m}^2$ between hillocks, with exception of 350 °C sample, in which hillocks were too close to separate.

electrical properties of the InGaAs samples at 300 K were strongly dependent on V/III ratio [Figs. 10(a) and 10(b)]. For growths performed at $T_g = 485$ °C, V/III was optimized at ~75 to reach the lowest n_0 of $3.8\times10^{14}\,\mathrm{cm}^{-3}$ and the highest μ_n of $5300\,\mathrm{cm}^2/\mathrm{V\,s}$. n_0 increased and μ_n decreased substantially if V/III was increased to 195 or decreased to 25. In addition to higher background electron density, the sample grown under low V/III conditions also contained larger hillocks (see Fig. 8). Strong defect scattering due to the high hillock density likely contributes to the reduction in μ_n at low V/III. For the samples grown with high V/III, we speculate that arsenic-related defects may play a role in the higher n_0. This issue is also encountered in the case of InGaAs(110), which is grown at low T_g and high V/III (Sec. V D).

T_g also controls the electronic properties of InGaAs(111)A, albeit to a slightly lesser extent than V/III ratio [Figs. 10(c) and 10(d)]. For samples grown at V/III = 75, increasing T_g from 420 to 485 °C increased μ_n from 3900 to $5300\,\mathrm{cm}^2/\mathrm{V\,s}$ at 300 K; we note that the dependence on T_g observed at V/III = 75 is similar to that at V/III = 225. The value of n_0 is

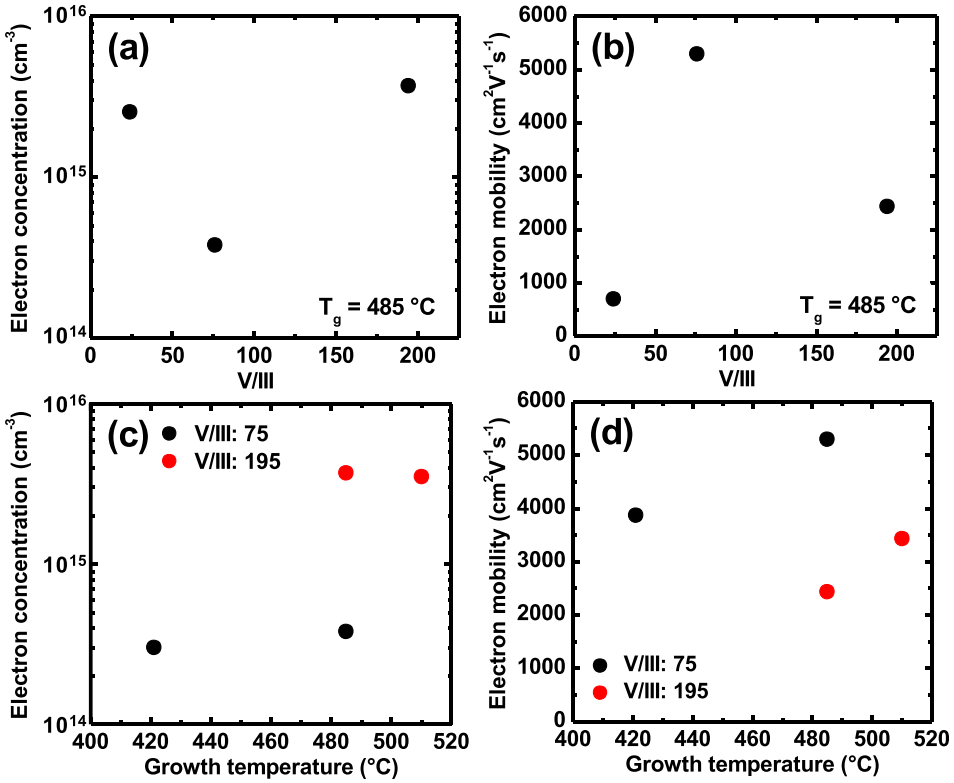

FIG. 10. (Color online) Effect of V/III ratio on (a) n_0 and (b) μ_n of InGaAs(111)A samples grown at 485 °C. Effect of T_g on (c) n_0 and (d) μ_n of InGaAs(111)A samples grown at V/III of 75 and 195. Hall measurements done at 300 K.

almost independent of T_g, and so the concurrent improvement in μ_n at high T_g cannot be attributed to a reduction in ionized impurities. Instead, the defects associated with hillocks likely dominate carrier transport since hillock density is strongly temperature sensitive. μ_n of the InGaAs(111)A samples is much lower than InGaAs(001) for which $\mu_n \approx 11500\,\mathrm{cm^2/V\,s}$ in this electron density range,[84] indicating significant room for improvement.

3. InGaAs(111)A: Photoluminescence

A monotonic improvement in PL intensity and FWHM linewidth was observed with increasing T_g for a given V/III ratio [Figs. 11(a) and 11(b)], likely due to the lower density of defective hillocks at high T_g. Figure 11(c) shows that the InGaAs PL intensity increased and linewidth decreased with higher V/III ratio; the improvement in PL from V/III = 25–75 is correlated with a large improvement in surface morphology. However, hillock density increased at V/III = 195, which does not explain the accompanying increase in PL intensity. Instead, a 10× increase in n_0 occurred at this V/III ratio [Fig. 10(a)], which would increase the radiative recombination rate. While V/III = 195 yielded the best PL, the highest Hall μ_n values were found for V/III = 75. This further suggests that the improvement of PL intensity at higher V/III may not be related to crystalline quality.

4. InGaAs(111)A: Summary

In summary, the optimization of InGaAs on InP(111)A requires high $T_g \geq 485$ °C and high V/III ratio to minimize surface roughness on the atomic scale and to alleviate hillocks. While hillock density is minimized at V/III ~ 75, roughness from atomic-scale features is minimized at V/III ~ 225. Optimization of electrical and optical properties largely overlaps with the conditions that minimize hillock density, allowing these properties to be jointly optimized.

Overall, our recommended growth conditions for InGaAs(111)A are: high T_g (≥485 °C) and V/III ratio ~75–225.

E. InAlAs on InGaAs/InP(111)A

In Secs. III C–III D, we showed that InAlAs and InGaAs(111)A exhibit similar growth trends, but that InGaAs(111)A exhibited a smoother surface both in terms of hillock density and wedding cake roughness. For applications that require smooth InAlAs(111)A, we demonstrate that InAlAs grown on top of an InGaAs(111)A buffer largely inherits the atomic-level smoothness of the InGaAs. After desorbing the native oxide under As_4, we grew 100 nm InAlAs on 50 nm InGaAs. InAlAs and InGaAs were grown at 510 °C using V/III ratios of 230 and 195, respectively.

InAlAs grown on an InGaAs(111)A buffer exhibits a tenfold reduction in hillock density compared to InAlAs grown directly on InP(111)A [2.1×10^6 and $1.5 \times 10^7\,\mathrm{cm^{-2}}$, respectively, Figs. 12(a) and 12(c)]. However, the InAlAs/InGaAs hillock density was still higher than that of the bare InGaAs layer [$8.8 \times 10^5\,\mathrm{cm^{-2}}$, Fig. 12(b)]. Under these growth conditions, both InGaAs(111)A and InAlAs(111)A have similar rms roughness away from the hillocks. Also, the average

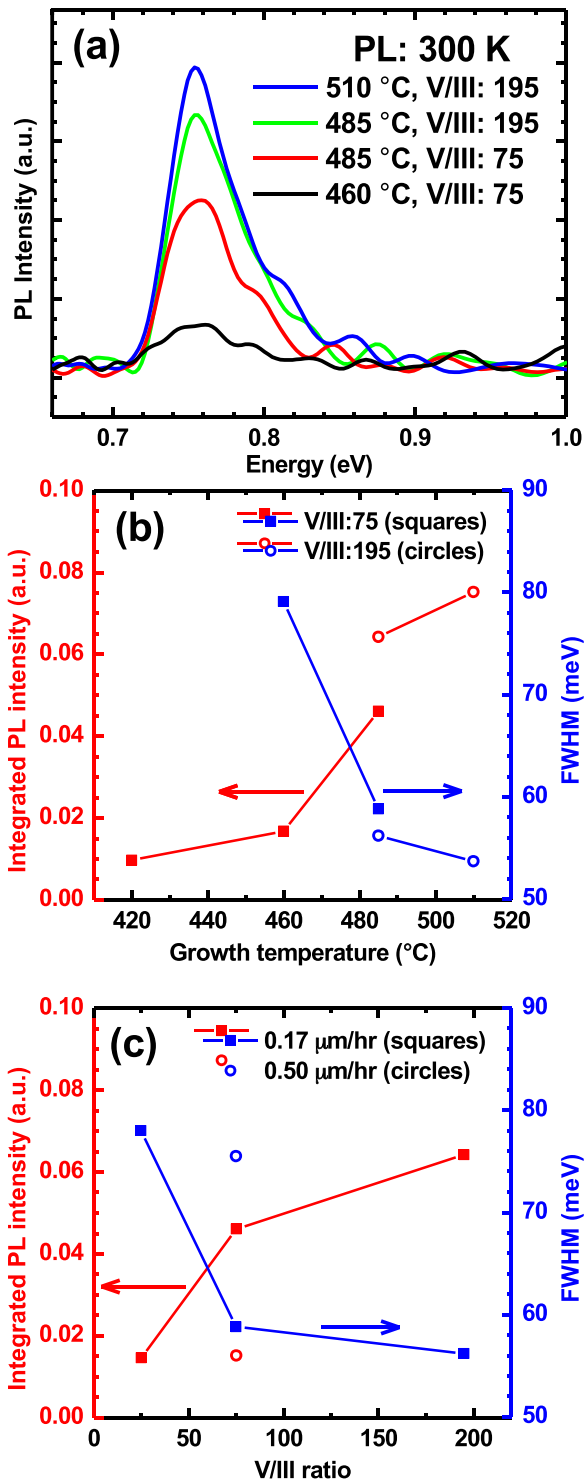

FIG. 11. (Color online) PL at 300 K for InGaAs(111)A grown under different conditions. (a) PL spectra showing effect of T_g and V/III ratio. Fourier transform filtering was applied to smooth spectra. Effect of (b) T_g and (c) V/III ratio on integrated PL intensity (left-hand vertical axes) and FWHM (right-hand vertical axes).

terrace width for InAlAs grown on InGaAs was 95 nm, very close to the 100 nm measured on the optimal InGaAs samples, and double the terrace width for optimal InAlAs grown directly on InP(111)A. Despite the tendency for InAlAs to form a high density of hillocks and tall wedding cakes, the step-edges and hillocks of the InGaAs provide favorable incorporation sites for adatoms during InAlAs growth. We have already demonstrated the effectiveness of this approach by growing high-quality InAlAs barriers for tensile strained GaAs(111)A quantum dots.[10]

IV. GROWTH ON InP (111)B

A. Review of growth on (111)B surfaces

Previous III–V epitaxy work on (111)B surfaces has focused primarily on GaAs(111)B, although good progress has also been made with InP(111)B homoepitaxy. The primary growth challenge for GaAs(111)B exact substrates is the formation of wide triangular hillocks, which were found to be nearly unavoidable.[60,85–87] These wide, short hillocks tend to cover the surface, in contrast to the taller, narrower hillocks for growth on (111)A surfaces (see Sec. III), degrading both the optical and electrical quality.[88] For GaAs(111)B, surface morphology was correlated with RHEED observations, where the low temperature (2×2) reconstruction was always associated with hillock formation. It is possible to obtain smooth GaAs(111)B when growth is performed at higher temperature where the $(\sqrt{19}\times\sqrt{19})$ surface reconstruction is stable, but only a very narrow growth window exists.[86] GaAs(111)B growth on the (1×1) reconstruction (stable at high T_g and low V/III ratio) is also known to result in smooth surfaces.[69] However, growth of smooth indium-containing materials such as InGaAs(111)B, under these same reconstructions, is difficult due to the high desorption rate of indium above $T_g = 530\,°C$.[85,86]

Due to these challenges, the use of offcut substrates became the primary solution to achieve smooth GaAs(111)B growth.[66,67,85] Yang *et al.* identified that the hillocks formed on GaAs(111)B were composed of three vicinal (111) "facets" inclined ~2° from the singular plane.[85] They proposed that these vicinal facets were more energetically stable than the singular (111) plane and thereby demonstrated that tilting the surface toward these planes by 1°–3° in the $\langle 2\underline{11}\rangle$ directions promoted smooth growth. Offcut substrates consequently resolved the problem of narrow growth windows. Growth in the $(\sqrt{19}\times\sqrt{19})$ and (1×1) regimes both resulted in smooth GaAs(111)B, even at low T_g, where $In_xGa_{1-x}As$/GaAs(111)B (e.g., $x<0.15$) could be grown with a unity sticking coefficient for indium.[69,85]

While resolving the hillock problem, growth of GaAs(111)B on offcut substrates is still susceptible to roughening by step-bunching on the atomic scale. Under many conditions, growth on offcut surfaces forms large atomic steps typically several nanometers tall, referred to as "macrosteps."[69–71] These macrosteps are composed of parallel alternations between exact (111) facets and vicinal (111) surfaces.[69,70] Proposed reasons for the step bunching include an energetically stable vicinal (111) face as well as arsenic desorption, which is a factor during high temperature growth;[69] high V/III ratios and moderate growth temperatures can prevent step bunching.[69,71]

Smooth homoepitaxy of InP(111)B also requires a substrate offcut. A study of growth by metalorganic vapor phase epitaxy showed that faceted InP morphologies were

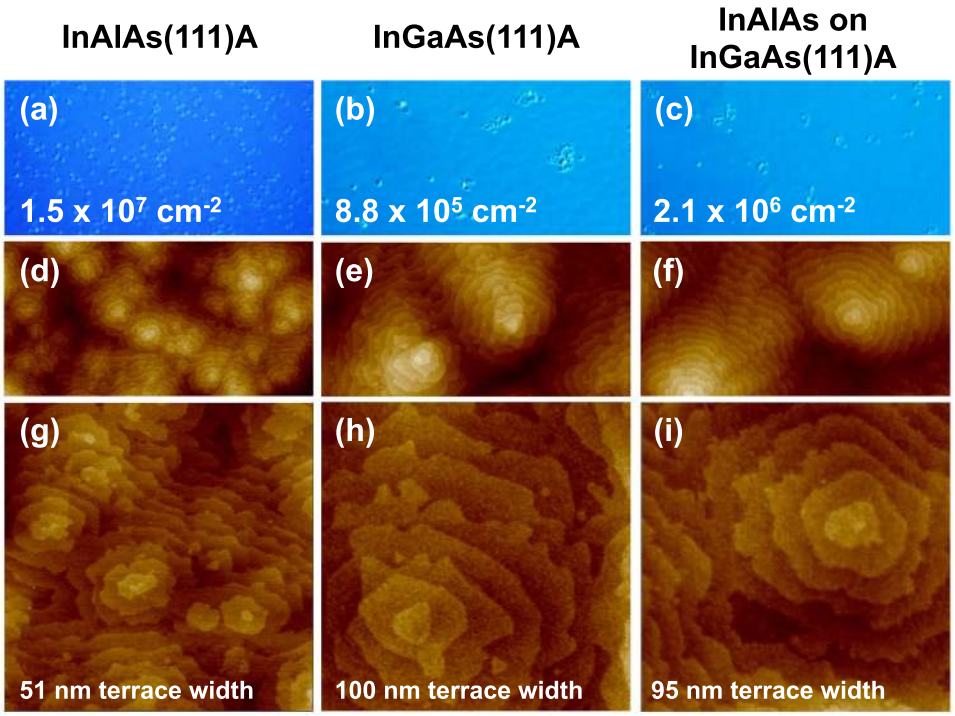

FIG. 12. (Color online) Comparison of InAlAs (200 nm), InGaAs (200 nm), and InAlAs/InGaAs (100 nm/50 nm) surface morphologies. Images in same column taken from same sample. For the InAlAs/InGaAs sample, InAlAs inherits the morphology of InGaAs at all length scales. (a)–(c): 50 μm wide Nomarski images, annotated with hillock densities. (d)–(f): 3 μm wide AFM images (5 nm z-scale). (g)–(i): 1×1 μm^2 AFM images (5 nm z-scale), annotated with average terrace width. Rms roughness value averaged over 25 μm^2 between hillocks.

unavoidable on exact substrates[61] and that smoother surfaces were possible using an offcut toward $\langle 2\underline{11} \rangle$ than an offcut toward $\langle 01\underline{1} \rangle$.[61] Growth optimization of InP was also reported by Hou and Tu for gas-source MBE for a 0.5° offcut toward $\langle 2\underline{11} \rangle$;[89] note that this group and some others refer to the $\langle 2\underline{11} \rangle$ offcut direction as the nearest $\langle 011 \rangle$, which are equivalent tilt directions.[90] They found that high T_g just below the InP decomposition temperature and low V/III ~ 1 produced featureless surfaces by Nomarski, while elongated surface defects emerged if higher V/III ratios were used.[89]

Very few reports discuss InAlAs and InGaAs growth on InP(111)B, though smooth surfaces have been obtained.[91,92] A 1° offcut toward $\langle 2\underline{11} \rangle$ was found to produce featureless surfaces by Nomarski with favorable bulk and two-dimensional electron gas mobilities, while a faceted surface was observed for growth on exact substrates.[91] However, neither atomic-level surface characterization nor systematic study of growth conditions on electrical or optical properties for InAlAs and InGaAs have been reported. Similar to GaAs(111)B, we have found that pronounced step bunching occurs under a wide range of conditions, further necessitating careful growth optimization.

B. InP(111)B homoepitaxy

1. InP(111)B: Surface morphology

For our experiments, we begin with InP(111)B homoepitaxy, which, unlike the (111)A surfaces, provided a useful initial buffer for subsequent ternary growth. Based on the review of (111)B growth in Sec. IV A, we exclusively used InP(111)B substrates with a 2° offcut toward $\langle 2\underline{11} \rangle$ to prevent faceting for all work in Sec. IV.

The InP(111)B deoxidation temperature must be carefully controlled to prevent substrate decomposition. We used 5×10^{-6} Torr of P_2 overpressure to desorb the native oxide prior to InP growth at 0.26 μm/h. At a high deoxidation temperature of 515 °C, indium droplets appeared in Nomarski due to InP decomposition [Fig. 13(a)]; this decomposition was not evident using *in situ* RHEED monitoring, which showed a bright, streaky (1×1) pattern throughout. Similar defects were noted by Hou and Tu resulting from decomposition at high temperature.[89] Lowering the deoxidation temperature to 495 °C prevented droplet formation [Fig. 13(b)].

Further optimization of InP growth was not required beyond the conditions reported by Hou and Tu,[89] and we demonstrated smooth InP(111)B growth at 475 °C with a low V/III of 6.4. The AFM image in Fig. 13(c) shows that after removing the native oxide at 495 °C, these growth parameters result in a very smooth surface with rms roughness of 0.23 nm across a 225 μm^2 area. The striated appearance of the AFM image resulted from closely spaced atomic steps due to the substrate offcut, and no step-bunching was observed.

Despite the absence of lattice mismatch in InP homoepitaxy, X-TEM of InP(111)B under optimum growth conditions showed a high density of dislocations at the initial growth interface (Fig. 14); a layer of InAlAs was grown on top of the InP buffer for study in Sec. IV C. We note that InP(111)B wafers are not widely available, so the dislocations may reflect the quality of the manufacturer's substrate surface preparation. Cleaning and etching of the substrate is

FIG. 13. (Color online) Effect of oxide desorption temperature on morphology of 100 nm InP on InP(111)B. (a) and (b) Nomarski images showing formation of indium droplets when deoxidation temperature is too high. Scale bars are 50 μm. (c) AFM image ($10 \times 10\,\mu m^2$, 3 nm z-scale) of smooth InP(111)B homoepitaxy using 495 °C desorb condition (Inset: $1 \times 1\,\mu m^2$ AFM image, 3 nm z-scale). Rms roughness is 0.23 nm averaged over 225 μm^2.

recommended to improve the microstructural quality for future work on InP(111)B. In addition, fine-tuning of the deoxidation procedure may further reduce formation of extended defects.

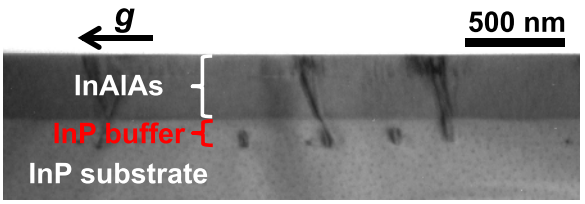

FIG. 14. (Color online) Bright field X-TEM of 100 nm homoepitaxial InP(111)B buffer with 300 nm InAlAs on top. Defects nucleate from InP/InP interface. $\boldsymbol{g} = 224$ and a [1$\underline{1}$0] imaging zone was used.

2. InP(111)B: Electrical properties

We performed Hall measurements on the InP(111)B buffers to assess their electrical properties, finding all samples to be unintentionally *n*-type. A sample grown under higher T_g and deoxidation temperatures of 515 °C was too resistive for measurement. These conditions exacerbate InP decomposition, producing poor electrical properties. Lowering T_g reduced the resistivity significantly, even with decomposition still present from the 515 °C deoxidation. Growth at 490 °C and V/III = 3.2 showed n_0 of $9.8 \times 10^{14}\,cm^{-3}$ and μ_n of $1650\,cm^2/V\,s$. Lowering T_g to 475 °C and increasing the V/III to 6.4 lowered n_0 to $5.3 \times 10^{14}\,cm^{-3}$ and increased μ_n to $2500\,cm^2/V\,s$, consistent with better material quality in a weaker decomposition regime. However, lowering the desorption temperature from 515 to 495 °C impaired the electrical properties, producing a high n_0 of $1.9 \times 10^{17}\,cm^{-3}$ and a low μ_n of $850\,cm^2/V\,s$, despite the prevention of surface decomposition. In contrast, InP(001) has a $\mu_n = 4000\,cm^2/V\,s$ for $n_0 = 1 \times 10^{15}\,cm^{-3}$,[93] suggesting that further work is needed to lower the dislocation density and reduce scattering in the InP(111)B epilayers.

A possible explanation is that the low deoxidation temperature does not fully remove the surface oxide and contaminants from the as-received wafer. Researchers have shown that the temperature window within which the native oxide can be successfully removed from InP(001) spans less than 10 °C.[94] Within this narrow range, the position at which the Fermi level is pinned is extremely sensitive to deoxidation temperature. Fine-tuning of the InP deoxidation temperature and anneal time is therefore critical to optimize electrical properties while avoiding substrate decomposition.

3. InP(111)B: Photoluminescence

PL results from the InP(111)B buffer layers, measured at 300 K, are shown in Fig. 15. PL spectra for the bare, semi-insulating InP(111)B substrates are also provided as a baseline for intensity comparison, and in general, the homoepitaxial layers are expected to have higher integrated intensity due to the unintentional *n*-type doping. T_g has a pronounced effect on the PL intensity, such that the PL intensity reduces by a factor of 8 as T_g was lowered from 515 to 475 °C [Fig. 15(a)]. All samples in Fig. 15 showed some degree of InP decomposition except for the 495 °C sample in Fig. 15(c). The stronger decomposition at the highest T_g likely increases

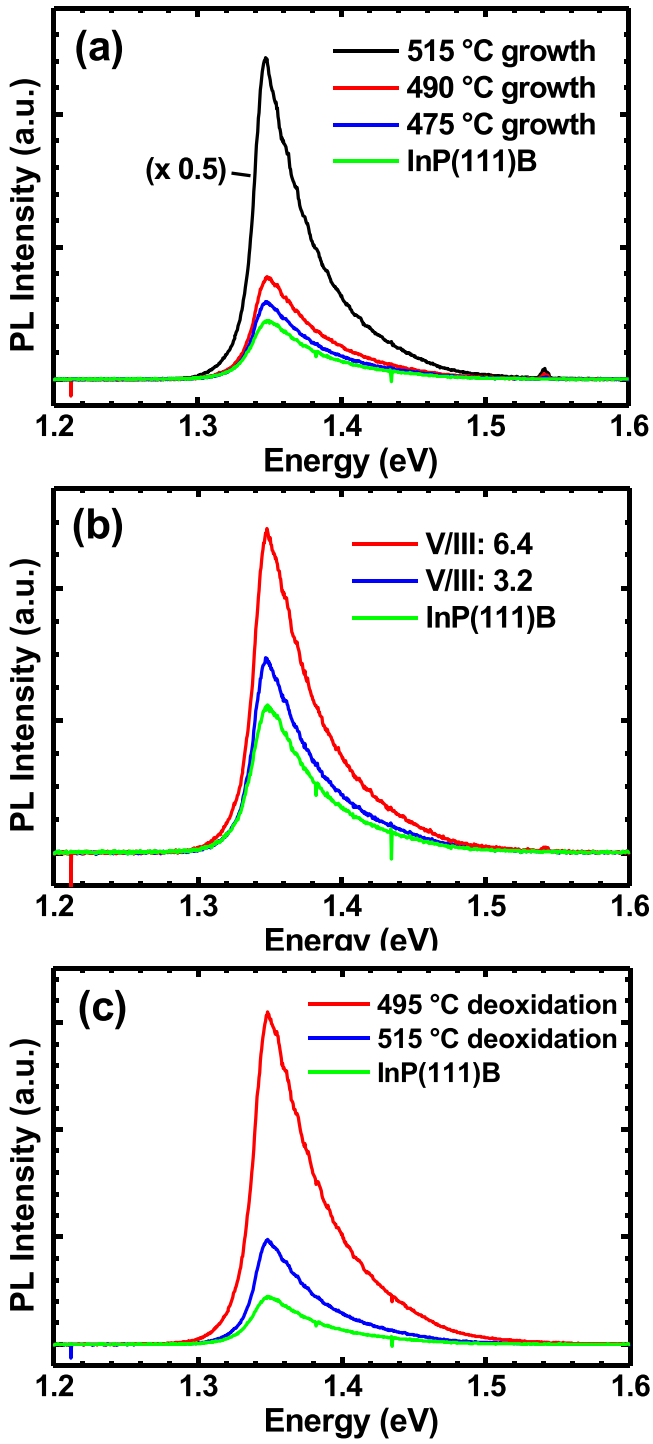

FIG. 15. (Color online) PL at 300 K comparing InP(111)B buffers grown under different conditions and bare semi-insulating InP(111)B substrate (green traces). (a) Effect of T_g using V/III = 3.2 and 515 °C deoxidation. Spectrum for sample grown at 515 °C scaled by 0.5× for comparison. (b) Effect of V/III ratio with $T_g = 475$ and 515 °C deoxidation. (c) Effect of deoxidation temperature with $T_g = 475$ °C and V/III = 6.4.

the PL intensity due to higher n_0 and increased light extraction due to surface roughening. Figure 15(b) shows that PL intensity increased significantly at higher V/III ratio. Finally, the effect of lower deoxidation temperature is shown in Fig. 15(c). The 495 °C deoxidation condition is the only sample

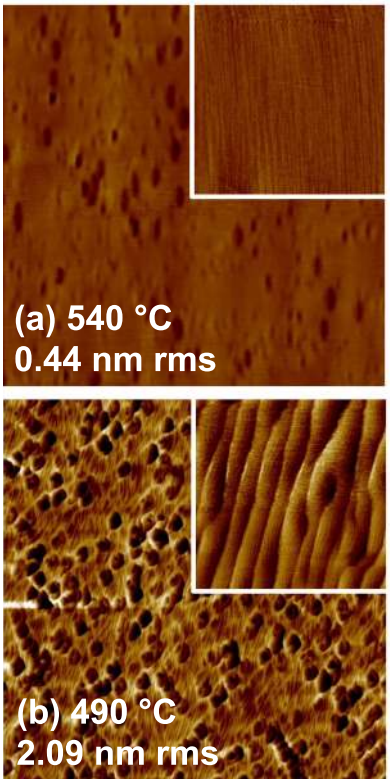

FIG. 16. (Color online) AFM images ($15 \times 15\,\mu m^2$, 10 nm z-scale) of InAlAs(111)B, showing effect of T_g at V/III = 12 (Insets: $1 \times 1\,\mu m^2$ AFM images, 5 nm z-scale). Rms roughness values averaged over 225 μm^2.

without decomposition. However, the much stronger PL intensity appears to be largely correlated to the much higher n_0 observed during Hall measurement. Growth conditions had little effect on the emission linewidth. In all cases, the

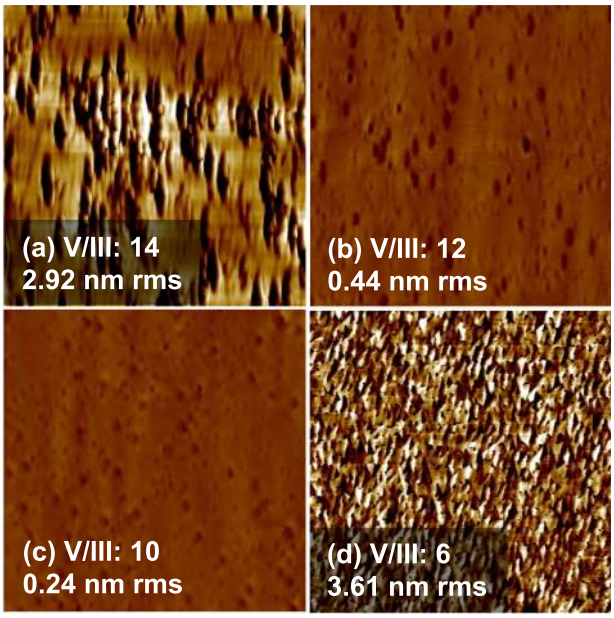

FIG. 17. (Color online) AFM images ($15 \times 15\,\mu m^2$, 10 nm z-scale) of InAlAs grown on InP(111)B showing effect of V/III ratio at $T_g = 540$ °C. Rms roughness values averaged over 225 μm^2.

epitaxial InP films produced higher PL intensity and slightly narrower linewidth than the InP(111)B substrate.

4. InP(111)B: Summary

We have produced smooth InP growth on offcut InP(111)B substrates using a T_g of 475 °C and a low V/III of 6.4. A low deoxidation temperature of 495 °C is important to prevent substrate decomposition. Low n_0 and reasonable μ_n values can be obtained near these conditions. However, further adjustment of the deoxidation temperature as well as improved substrate preparation is needed to remove defects indicated by Hall measurement and TEM.

C. InAlAs on InP(111)B

1. InAlAs(111)B: Surface morphology

Here, we present our optimization of MBE conditions for the growth of InAlAs on InP(111)B to achieve low surface roughness, and good optical and electrical properties. Since growth is performed on offcut substrates, the primary obstacle to smooth growth is step bunching rather than hillock formation, as discussed in Sec. IV A.

We removed the InP native oxide at 495 °C before growing InAlAs on the InP(111)B surface. For some samples, a 100 nm InP buffer was grown prior to the InAlAs, but the presence of the InP buffer was found to have no effect on InAlAs growth trends. In either case, the InP is initially capped with 5 nm InAlAs grown at 480 °C to protect the InP from decomposition during higher temperature growth. Without this 5 nm InAlAs cap, growth of InAlAs above 480 °C resulted in rough surfaces. Next, 200–500 nm of InAlAs was deposited at 0.5 μm/h to study the effect of T_g and V/III ratio on surface morphology. Across all growth conditions studied, RHEED monitoring showed a (1×1) streaky pattern for both InP and InAlAs surfaces, similar to GaAs(111)B under certain growth conditions.[95,96]

Almost all InAlAs(111)B samples grown in this study appeared smooth when viewed with Nomarski (not shown). However, at the atomic scale it is clear that T_g strongly influences surface morphology (Fig. 16). Growth at $T_g = 540$ °C yielded a smooth surface with a prevalence of monolayer-high steps [Fig. 16(a) inset], implying a step-flow growth mode. Reducing T_g to 490 °C resulted in the appearance of tall step bunches on the surface [Fig. 16(b) inset]. Pits formed where many step edges bunched together at a particular location (i.e., step pinning), and the depth of the pits decreased with increasing T_g.

It is not possible to investigate whether InAlAs(111)B surfaces improve further at even higher T_g. Five hundred and forty degree Celsius is the hottest we can grow smooth InAlAs before thermal decomposition occurs and indium droplets appear. In addition, due to the high desorption rate of indium at 540 °C,[97] the InAlAs composition is sensitive to small temperature variations during growth. Thus the $In_xAl_{1-x}As$ composition in this study was found to vary among samples from x = 0.514–0.532, as measured by x-ray diffraction and PL.

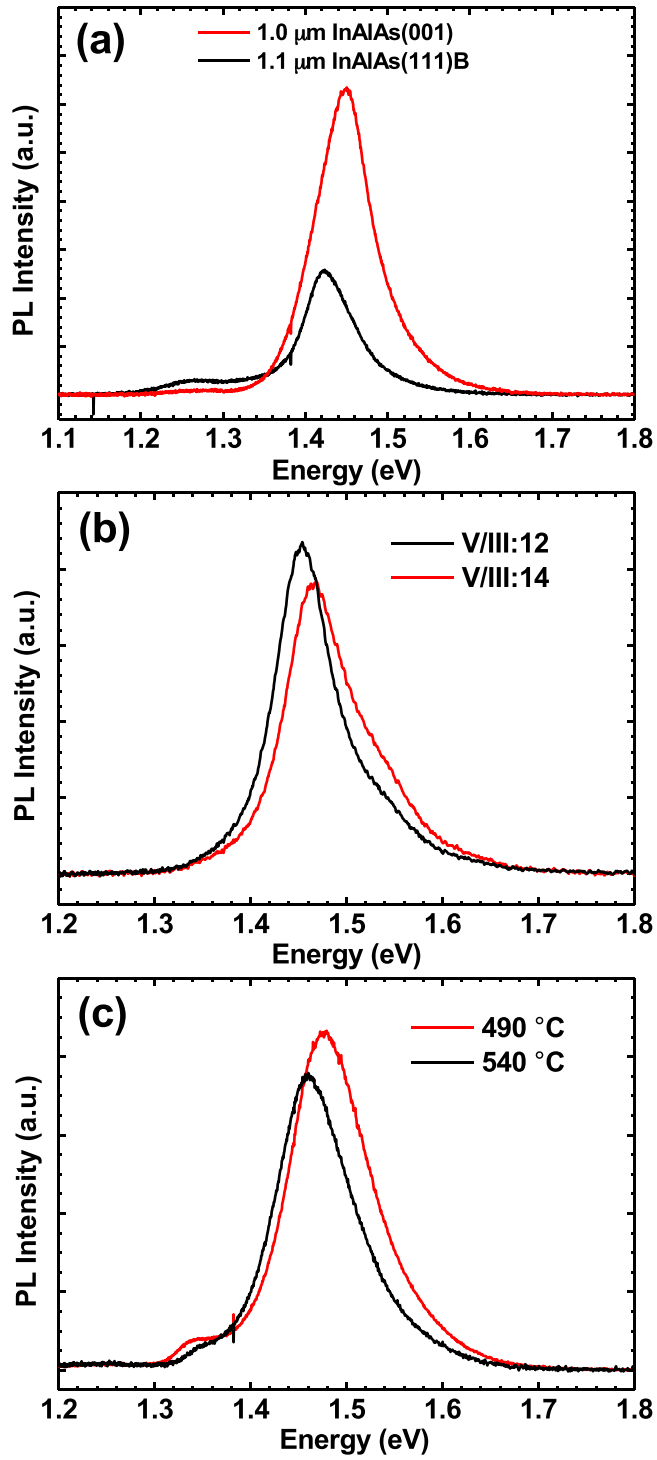

FIG. 18. (Color online) PL at 300 K for InAlAs. (a) Comparison between InAlAs grown on InP(001) and InP(111)B. (111)B sample contains a buried 3 ML GaAs layer for tensile nanostructure study, causing broad emission at ~1.26 eV, as discussed elsewhere (Ref. 32). (b) Effect of V/III ratio on InAlAs(111)B PL. (c) Effect of T_g on InAlAs(111)B PL. InP emission at 1.34 eV is also present in (b), since a 100 nm InP buffer was grown beneath the InAlAs in this case.

InAlAs(111)B surface morphology is also very sensitive to V/III ratio. Figure 17 shows AFM images of InAlAs grown at $T_g = 540$ °C with varying V/III. A clear optimum in the InAlAs roughness lies at V/III = 10–12, corresponding to rms roughnesses of 0.24–0.44 nm. At a higher V/III of 14,

step bunches became larger and deeper, while at a lower V/III of 6, small facets and pits covered the surface and the RHEED became faint.

As a result of this buffer optimization, we were able to obtain surfaces with atomic-scale smoothness at 540 °C and V/III ~ 10 [Fig. 17(c)]. Small indentations in the sample surface were still visible by AFM due to a slight tendency toward step-bunching, but these features contribute very little to the overall roughness. The $1 \times 1\ \mu m^2$ inset to Fig. 16(a) (grown at 540 °C, V/III = 12) shows closely spaced, parallel monolayer steps running perpendicular to the [2$\underline{1}$1] offcut direction (i.e., parallel to [0$\underline{1}$1]). These monolayer steps are spaced 11 nm apart, consistent with the 2° substrate offcut.

TEM of the optimized InAlAs(111)B buffers shows that the lattice-matched InAlAs did not produce new defects when grown atop an InP epilayer (Fig. 14). When InAlAs was grown directly on the InP substrate (not shown), a similar density of dislocations was observed as that of the InP/InP(111)B homoepitaxial interface in Fig. 14, supporting our hypothesis that the dislocations originate from nonideal substrate preparation, rather than the growth conditions.

2. InAlAs(111)B: Electrical properties

We performed Hall measurements to compare InAlAs(111)B samples grown at 490 and 540 °C. The InAlAs(111)B surface was found to produce Ohmic contacts after etching the native oxide, whereas contacts to InAlAs on (001), (110), and (111)A surfaces could not be obtained, due to rapid oxidation. Of the four orientations, only the InAlAs(111)B surface is aluminum-free. We speculate that the arsenic-terminated InAlAs(111)B surface hinders oxidation of the buried aluminum, enabling Ohmic contact to these samples. In addition to smoother surface morphology, higher T_g was found to improve the electrical properties. The InAlAs(111)B samples had μ_n values (n_0 values) of $1100\ cm^2/V\,s$ ($1.3 \times 10^{16}\ cm^{-3}$) and $3600\ cm^2/V\,s$ ($4.0 \times 10^{15}\ cm^{-3}$), for T_g of 490 and 540 °C, respectively. Unexpectedly, the sample with $\mu_n = 3600\ cm^2/V\,s$ suggests that InAlAs(111)B could have higher μ_n than InAlAs(001); for InAlAs(001), Ref. 98 reports $\mu_n = 1350\ cm^2/V\,s$ for $n_0 = 3.7 \times 10^{15}\ cm^{-3}$.

3. InAlAs(111)B: Photoluminescence

Optimized InAlAs(111)B exhibited strong 300 K PL, with ~40% the PL intensity of InAlAs(001) grown in the same MBE system [Fig. 18(a)]. The weaker PL of InAlAs(111)B compared to (001) is likely due to the high density of extended defects that form at the initial growth interface, which we attribute to the substrate preparation.

The PL intensity and linewidth of InAlAs(111)B was relatively insensitive to the growth conditions investigated [Figs. 18(b) and 18(c)]. Even though increasing the V/III ratio from 12 to 14 significantly roughened the surface, the PL intensity decreased only slightly. Lower T_g, which was observed to produce large step bunches, also did not deteriorate the PL intensity. However, PL linewidth did correlate with surface morphology, with broader linewidths measured

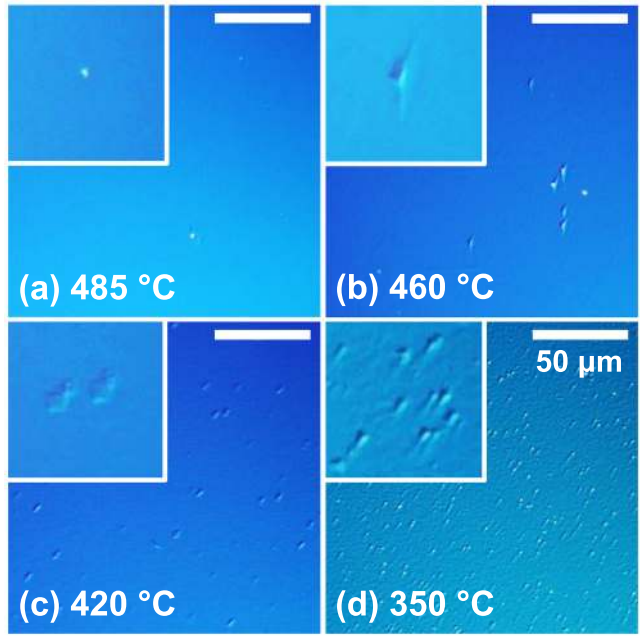

FIG. 19. (Color online) (a)–(d) Nomarski images showing effect of T_g on InGaAs(111)B morphology at V/III = 75. Insets: higher magnification images of surface features, with $20 \times 20\ \mu m^2$ area.

for the rougher samples grown with higher V/III of ~14 and lower T_g of 490 °C. The surface roughening may play a role in compositional inhomogeneity for InAlAs due to nonuniform adatom incorporation along the surface. As noted earlier in this section, small variations in T_g slightly modulated the InAlAs composition, and hence the PL peak position varied from 1.42 to 1.47 eV.

4. InAlAs(111)B: Summary

InAlAs(111)B can be jointly optimized for surface roughness, optical, and electrical properties, and we have shown atomically smooth InAlAs(111)B surfaces with PL and electrical quality comparable to InAlAs(001). Elsewhere, we have shown that InAlAs(111)B grown under these conditions makes a suitable buffer and barrier material for high quality tensile GaAs(111)B quantum dashes with strong PL.[9]

Overall, our recommended growth conditions for InAlAs(111)B are high T_g of 540 °C and a narrow window of V/III ratio of 10–12.

D. InGaAs on InP(111)B

1. InGaAs(111)B: Surface morphology

We investigated growth of InGaAs(111)B by depositing 200 nm on offcut InP(111)B substrates at 0.17 μm/h, consistent with other InGaAs samples in this study. As for InAlAs(111)B growth, InGaAs(111)B maintains a (1×1) streaky RHEED pattern for all tested conditions.

Both T_g and V/III ratio had similar effects on the morphology of offcut InGaAs(111)B as offcut InAlAs(111)B. From Nomarski images (Fig. 19), an overall improvement in surface roughness with increasing T_g was observed. At the low T_g of 350 °C, a high density of kite-shaped features

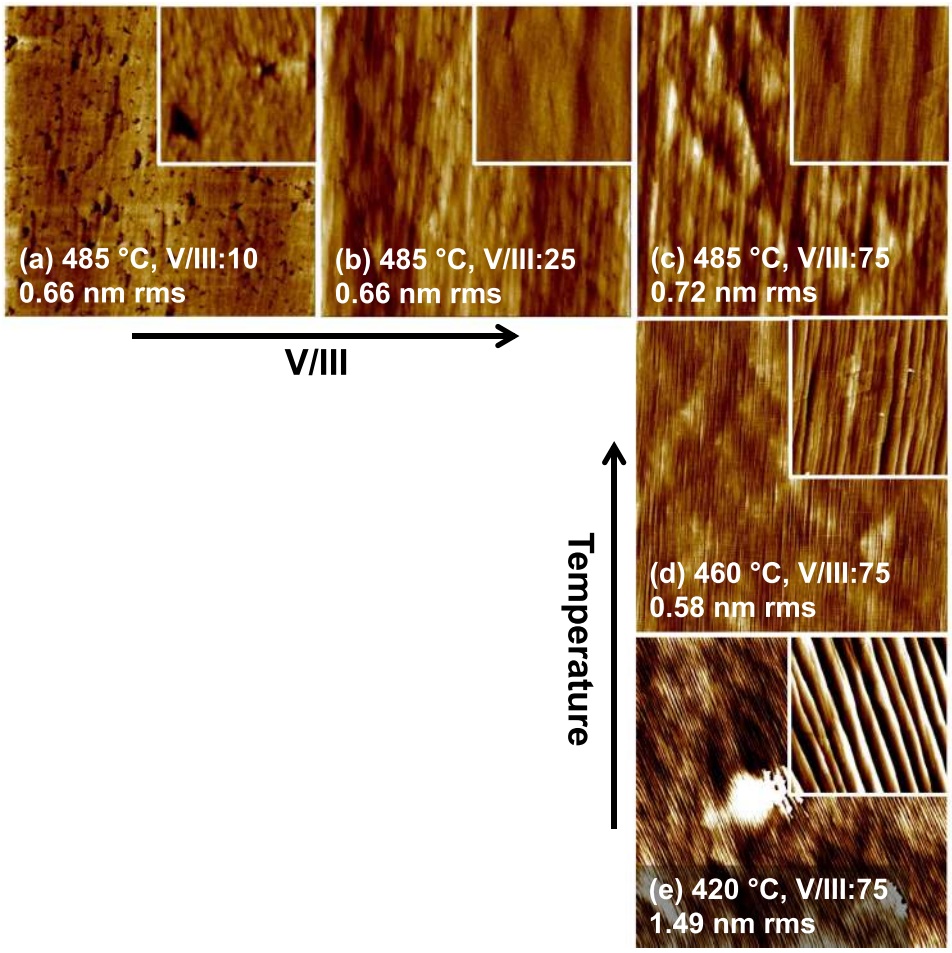

FIG. 20. (Color online) AFM images ($15 \times 15\ \mu m^2$, 5 nm z-scale) of InGaAs grown on offcut InP(111)B, showing effect of T_g and V/III ratio on morphology (Insets: $1 \times 1\ \mu m^2$ AFM images, 3 nm z-scale). Rms roughness values averaged over $225\ \mu m^2$.

appear, and with increasing T_g, these features changed shape and decreased in density, disappearing almost entirely by 485 °C. A low density of faint features remained on the surface at $T_g = 485$ °C, resembling oval-defects that often form during the growth of buffers on (001) surfaces.

AFM imaging shows that higher T_g also suppressed step bunching for InGaAs [Figs. 20(c) and 20(e)], just as it did for InAlAs(111)B. At $T_g \leq 460$ °C, pronounced macrosteps formed due to the merging of adjacent offcut steps into taller steps. In contrast to InAlAs(111)B, the InGaAs macrosteps were straight instead of wavy, and pit-shaped step-bunches were not observed. The macrosteps roughened the atomic surface significantly, and the rms roughness increased from 0.58 nm at 485 °C to 1.49 nm at 400 °C as step bunches became more pronounced. However, the surface was also roughened by elongated triangular features as T_g was increased to 485 °C. These features may indicate the onset of faceting, as previously reported in (111)B growth.[60,85–87]

Optimization of the V/III ratio is also important for smooth InGaAs(111)B growth, again similar to offcut InAlAs(111)B. As we decreased V/III from 75 to 10 at $T_g = 485$ °C [Figs. 20(a)–20(c)], the triangular features became less pronounced, and then disappeared. However, a high density of pits emerged at V/III = 10, which was also observed for InAlAs(111)B grown at lower V/III. The optimal growth condition for surface smoothness lies between V/III = 10–25, a slightly larger window than we observed for InAlAs. In Nomarski, all samples were nearly featureless at 485 °C, independent of V/III ratio.

2. InGaAs(111)B: Electrical properties

Nominally undoped InGaAs(111)B exhibited an n-type carrier background. Depending on growth conditions, we measured n_0 values ranging from 2×10^{16} to $1 \times 10^{17}\ cm^{-3}$, with $\mu_n = 1300$–$4000\ cm^2/V\ s$. V/III ratio had a strong effect on electrical properties, where increasing V/III raised μ_n and lowered n_0 [Figs. 21(a) and 21(b)]. The inverse relationship between μ_n and n_0 suggests that ionized impurity scattering is one of the factors limiting μ_n. The relationship between V/III ratio and electrical properties is not monotonic, but instead μ_n (n_0) is lowest (highest) at V/III = 25 and improves at both higher and lower V/III. However, atomic hills or pits appear at high or low V/III ratios [Figs. 20(a)–20(c)], indicating a small tradeoff between morphology and electrical properties during V/III optimization.

T_g is an equally important variable with μ_n (n_0) increasing (reducing) with temperature [Figs. 21(c) and 21(d)]. Once

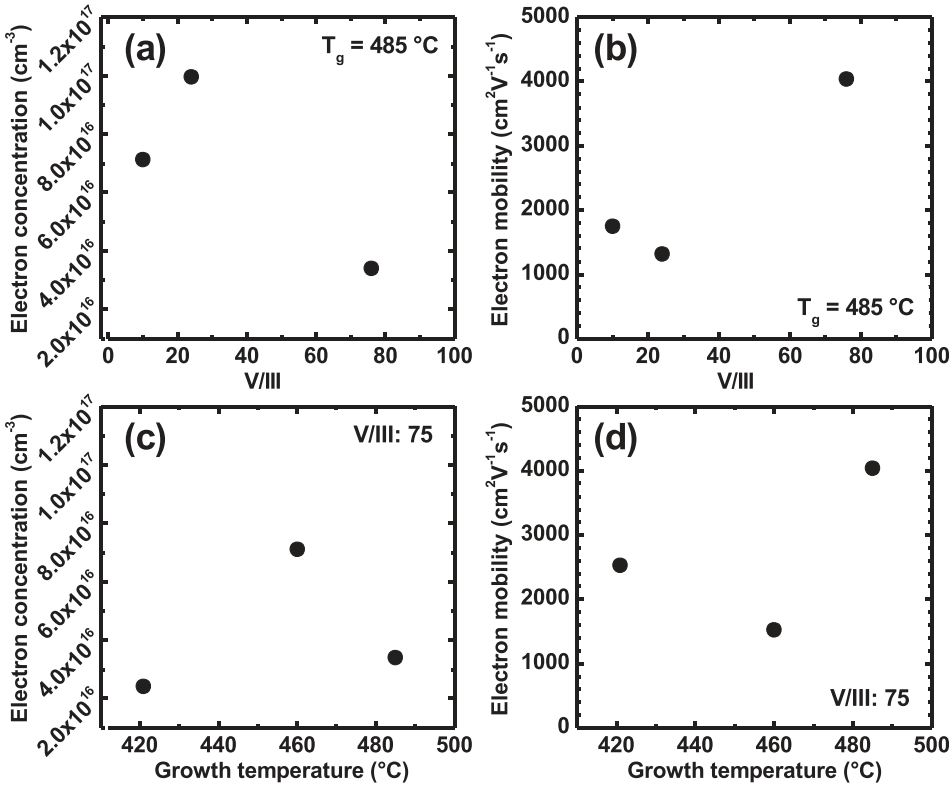

FIG. 21. Effect of V/III ratio on (a) n_0 and (b) μ_n of InGaAs(111)B samples grown at 485 °C. Effect of T_g on (c) n_0 and (d) μ_n of InGaAs(111)B samples grown at V/III = 75. Hall measurements done at 300 K.

again, conditions that produced low n_0 also yielded high μ_n, confirming the role of ionized impurity scattering. Similar to the V/III trend, the improvement was not monotonic, but some degradation was observed for a moderate T_g of 460 °C. As before, the electrical quality was correlated with higher surface roughness, for reasons not currently understood. Overall improvement in μ_n at high T_g was also found by Yeo *et al.*, who reported Si-doped InGaAs(111)B with μ_n as high as 5100 cm^2/V s for T_g of 550 °C.[91] We note that these values are still below the 8000–10 000 cm^2/V s observed for InGaAs(001) in this electron density range,[84] indicating significant scattering. This increased carrier scattering in InGaAs and InP growth on (111)B is likely linked to the high dislocation densities originating from the initial growth interface (Fig. 14).

3. InGaAs(111)B: Photoluminescence

The effect of T_g on the InGaAs(111)B PL is shown in Fig. 22(a). For all InGaAs(111)B samples observed, linewidths decreased under conditions where PL intensity increased. PL intensity [Fig. 22(b)] and linewidth [Fig. 22(c)] are optimized at $T_g \sim 460$ °C and V/III ~ 25, respectively, growth conditions that correspond to samples with lowest surface roughness. An increase in linewidth with surface roughness suggests that rougher surfaces have spatially nonuniform incorporation of indium and gallium adatoms. In some quaternary alloys, small adjustments in the surface orientation can significantly change the alloy composition,[99,100] which can lead to compositional nonuniformity for rough surfaces. Comparing the PL in Fig. 22 to the Hall data in Fig. 21, PL intensity and n_0 are closely correlated. This indicates that the higher PL intensity at 460 °C is largely due to a faster radiative recombination due to higher n_0 and is less strongly related to material quality.

A similar assessment applies to the PL trend with V/III ratio where again, the optimum PL corresponded to the V/III condition that yielded the smoothest surface. At V/III = 25, both surface pits and faceting were avoided, which may lead to narrower linewidths due to better compositional uniformity.[99,100] PL intensity and n_0 were closely correlated across V/III ratios (Figs. 21 and 22). As we increased V/III from 25 to 75, PL intensity decreased due to reduced n_0, even though material quality appears to be higher, based on higher μ_n (Fig. 21).

4. InGaAs(111)B: Summary

In this section we have shown that the optimization of offcut InGaAs(111)B morphology follows a similar trend to that of offcut InAlAs(111)B. For InGaAs, moderate T_g of $\sim$460 °C and V/III ratio of $\sim$25 are needed to minimize surface roughness. A minimum rms roughness of 0.66 nm was obtained in InGaAs, which is somewhat higher than the 0.24 nm rms roughness achieved in InAlAs. The μ_n of InGaAs(111)B has not reached the level of InGaAs(001) growth, but further improvements should be possible based on the observed trends. To optimize electrical transport properties, we recommend high T_g ($\geq$485 °C) and V/III ratios ($\sim$75). InGaAs PL intensity varies primarily due to n_0, while

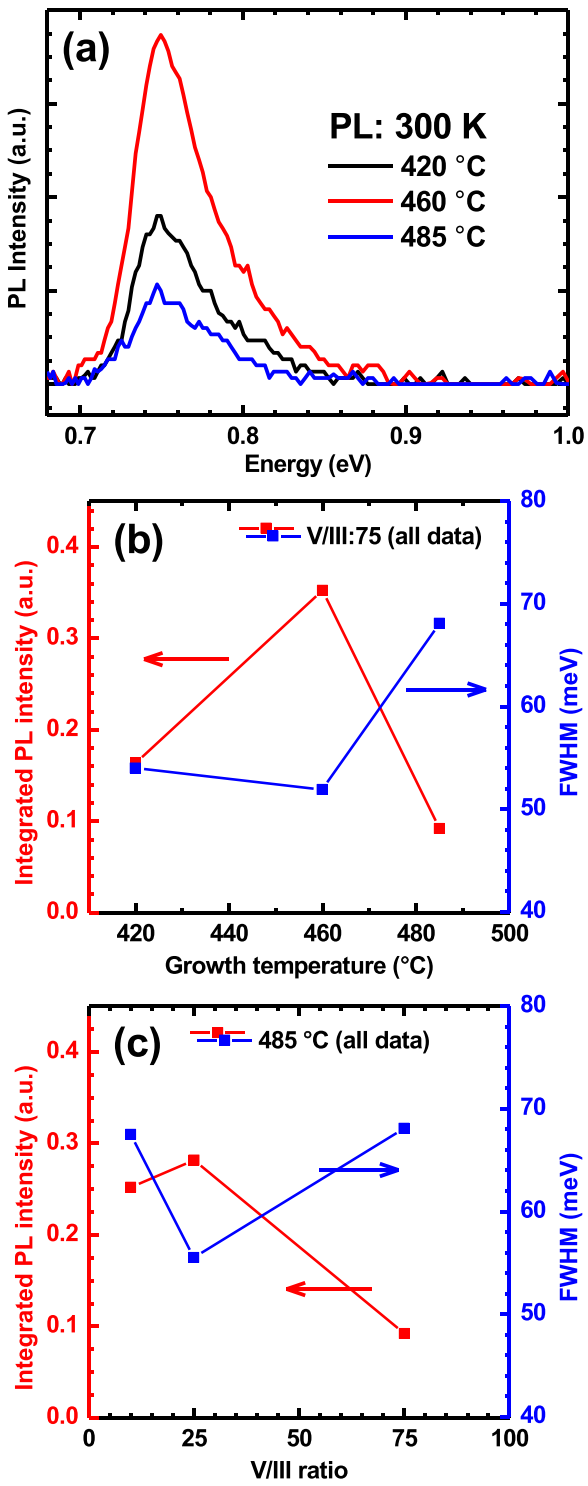

FIG. 22. (Color online) PL at 300 K for InGaAs(111)B grown under different conditions. (a) PL spectra showing effect of T_g. Effect of (b) T_g and (c) V/III ratio on integrated PL intensity (left-hand vertical axes) and FWHM (right-hand vertical axes).

the PL linewidth appears to correlate with surface smoothness. As a result, an acceptable compromise between the smoothness of InGaAs(111)B and its electrical and optical properties can be made, even though individually each property is optimized at different areas of the parameter space.

Overall, our recommended growth conditions for InGaAs(111)B are $T_g = 485\,°C$ and V/III ratio = 75.

V. GROWTH ON InP (110)

A. Review of growth on (110) surfaces

Previous work on (110) growth has primarily focused on GaAs homoepitaxy, although some studies exist for InGaAs, InAlAs, and other III–Vs. Early studies found that rough surfaces with elongated, faceted hillocks were formed under a wide range of T_g, V/III ratios, and growth rates.[62,63] At the low V/III ratios typical for (001) growth, metal droplets formed on the (110) surface, indicating a low sticking coefficient for arsenic.[63] Consistent with the poor morphology, carrier mobilities were very low and PL emission was dominated by defect levels.[62,63]

Analysis of the hillocks created during on-axis GaAs(001) growth showed that they are elongated along [001] with a prominent (11$\bar{1}$)A facet.[101] The problem of hillocks was thus resolved by using an offcut 6° toward the (11$\bar{1}$)A facet.[68] Subsequently, the same offcut technique has been used to achieve smooth InGaAs, InAlAs, InGaAsP, and InP on InP(110).[38,64,102,103]

For growth on exact (110) surfaces, Zhou *et al.* reported that by using relatively low growth rate, high V/III ratio, and low T_g of 470–500 °C, they could create AlGaAs/GaAs(110) heterostructures with sufficiently good interface quality to form a high μ_n 2D electron gas (2DEG).[104] Pfeiffer *et al.* subsequently confirmed that similar growth conditions produced smooth surfaces, and demonstrated a 2DEG with very high μ_n via growth on a cleaved (110) wafer edge.[105,106] Wassermeier *et al.* later investigated GaAs(110) growth trends by AFM, and eliminated hillocks using elevated V/III ratio and reduced growth rate to produce atomically smooth surfaces with step-flow growth.[107]

In contrast, InGaAs and InAlAs growth on exact InP(110) have received little study. Brown *et al.* found that smooth InGaAs and InAlAs could only be formed using an extremely low temperature of 300 °C and a high V/III of 80.[64] Yasuda *et al.* confirmed this trend for InAlAs(110), showing the formation of large, triangular hillocks above this temperature.[38] In this section, we present a brief study of InAlAs(110), followed by a detailed growth parameter study of InGaAs(110).

B. InP(110) homoepitaxy

The development of homoepitaxial, on-axis InP(110) buffers may promote the growth of smooth InAlAs(110) and InGaAs(110) epilayers. InP(110) could not be experimentally investigated by our group however, due to equipment problems. Previous work on InP(110) growth on exact substrates shows a highly faceted surface,[102,103] consistent with the growth of other (110) III–Vs (Sec. V A). Bhat *et al.* showed by MOCVD that specular surfaces nearly free of defects can be obtained for a 3° offcut toward (111)A or (111)B, and they suggest that further improvement is possible with a higher offcut.[102] Mitsuhara *et al.* confirmed this result for chemical beam epitaxy growth, and found gradual improvement in the surface morphology with offcut angle up to 6°.[103] Smooth growth of GaAs(110) as well as InGaAs(110) and InAlAs(110) can be achieved using very

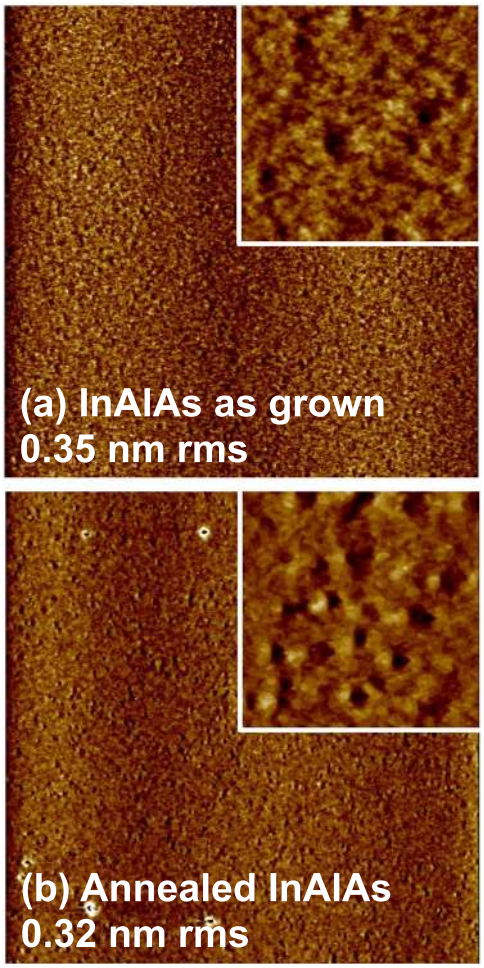

FIG. 23. (Color online) AFM images ($10 \times 10\ \mu m^2$, 3 nm z-scale) of InAlAs on InP(110) (Insets: $1 \times 1\ \mu m^2$ AFM images, 3 nm z-scale). For both (a) and (b), InAlAs was grown at 280 °C with V/III = 80. Sample in (b) was annealed for 15 min at 500 °C after growth. Rms roughness value averaged over 225 μm^2 .

low T_g and high V/III ratios (Secs. V A, V C, and V D), and a similar strategy may be applicable to the growth of InP(110) buffers in future work.

C. InAlAs on InP(110)

1. InAlAs(110): Surface morphology

Following the work of Brown *et al.*, we utilized a low T_g of 280 °C and high V/III ratio of 80 to achieve smooth InAlAs

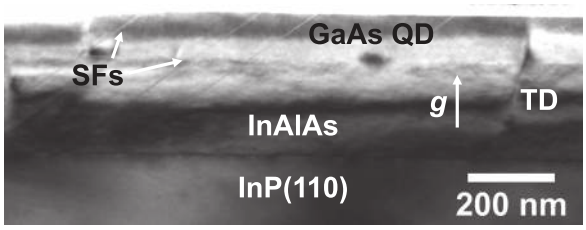

FIG. 24. Bright field X-TEM of InAlAs grown on InP(110). GaAs QDs embedded 100 nm from the InAlAs surface are described elsewhere (Ref. 30). Stacking faults nucleate at the InAlAs/InP interface. A threading dislocation (TD) is also visible on the right side of the image. Horizontal contrast bands are from bending of the sample. $g = 220$ and a ⟨110⟩ imaging zone was used.

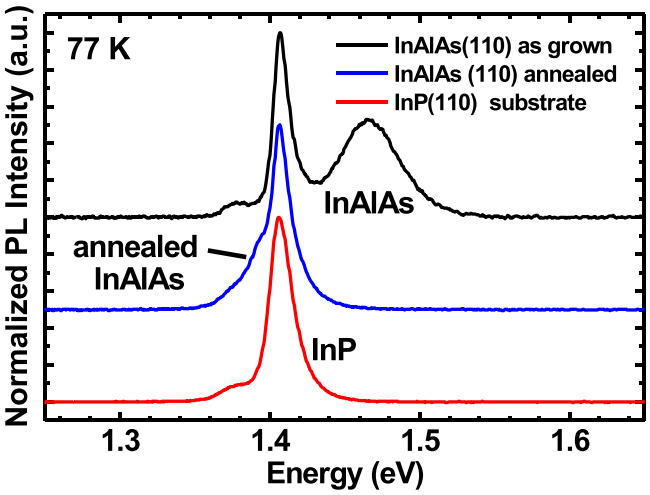

FIG. 25. (Color online) PL at 77 K for InAlAs/InP(110) samples. PL spectra are normalized to the height of the InP peak, and offset vertically for clarity.

growth on InP(110) substrates.[64] Following desorption of the native oxide from the InP substrate at 500 °C under As_4, we deposited 200 nm of InAlAs at 0.5 μm/h. During each InAlAs growth, a streaky (1×1) RHEED pattern was observed. This compares well with the (1×1) pattern reported for pristine GaAs(110) surfaces (before growth) where surface atoms are displaced, yet retain the (1×1) periodicity.[108–110] Other reconstructions for growth of III–Vs on (110) surfaces have not been reported to our knowledge.

Nomarski images confirmed that the InAlAs(110) surface was smooth and featureless (not shown), while AFM images showed a smooth surface with 0.35 nm rms over a $15 \times 15\ \mu m^2$ area (Fig. 23). The absence of faceted hillocks is consistent with previous reports that high V/III and low T_g promote a smooth (110) surface.[64,104,106] The atomic surface morphology was disordered, and defined neither by step-flow growth nor clear indications of 2D islanding. In addition, small pits were visible in the $1 \times 1\ \mu m^2$ image [Fig. 23(a) inset] that are 1.0–1.5 nm deep. We attribute this morphology to the use of a low T_g that prevents adatoms from diffusing to their lowest energy sites and forming clear terraces. We attempted to smooth the InAlAs(110) further using annealing at 500 °C under As_4, based on a report by Yoshita *et al.*,[111] but rms roughness was unchanged [Fig. 23(b)].

While the use of low T_g produces an atomically smooth surface, the microstructure suffers from a high density of stacking faults (SFs) that emerge from the InAlAs/InP growth interface (Fig. 24). A high SF density was also observed for InAlAs(110) in Ref. 38 under similar conditions. We have confirmed by XRD that the InAlAs composition is nearly lattice-matched to InP, so the SF nucleation is not induced by the lattice mismatch. To prevent SF formation, we suggest that the process by which InAlAs growth is initiated could be optimized.

2. InAlAs(110): Photoluminescence

PL for the annealed and nonannealed InAlAs(110) samples at 77 K is shown in Fig. 25. The nonannealed sample

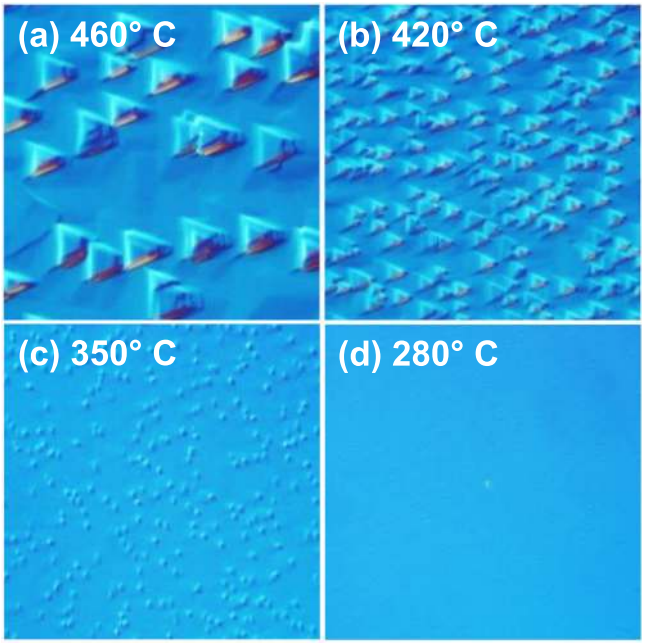

FIG. 26. (Color online) (a)–(d) Nomarski images ($50 \times 50\,\mu m^2$) of InGaAs on InP(110) showing effect of T_g on morphology at V/III = 75. Hillocks are present on all samples, but have low contrast at 280 °C due to their small size.

has an emission peak at 1.47 eV, with a FWHM of 48 meV. PL from the annealed sample was red-shifted to ~1.39 eV (overlapping the InP peak). The group-III composition from XRD was found to be 51.2% indium in both samples, so the expected bandgap at 77 K is 1.54 eV. The 1.47 eV peak for low-T_g InAlAs is consistent with the report by Brown *et al.*, who attributed the reduction in emission energy to a defect-assisted transition.[64] The reason for the redshift of the InAlAs PL after annealing is not currently understood. However, Ohbu *et al.* observed a similar effect in low-T_g GaAs, where high temperature annealing extinguished the near-band edge emission, while creating new luminescent defect levels.[112] It is also possible that the InAlAs PL has been quenched by the anneal, while the shoulder on the InP peak results from a new defect-assisted transition near the InP-InAlAs interface.

The presence of defect levels within the InAlAs is not surprising, given that the low T_g required for smooth growth also promotes incorporation of excess As and other point defects.[113] The PL of both InAlAs(110) samples is much weaker than typical for InAlAs(001) (not shown). The relatively weak InAlAs(110) PL suggests that point and extended defects in the buffer contribute significantly to non-radiative recombination. Increasing T_g regime is clearly desirable, to mitigate point defects and improve the optical properties. However, our attempts to increase T_g to 320 °C led to the creation of hillocks on the surface, similar to the case of InGaAs(110) discussed below.

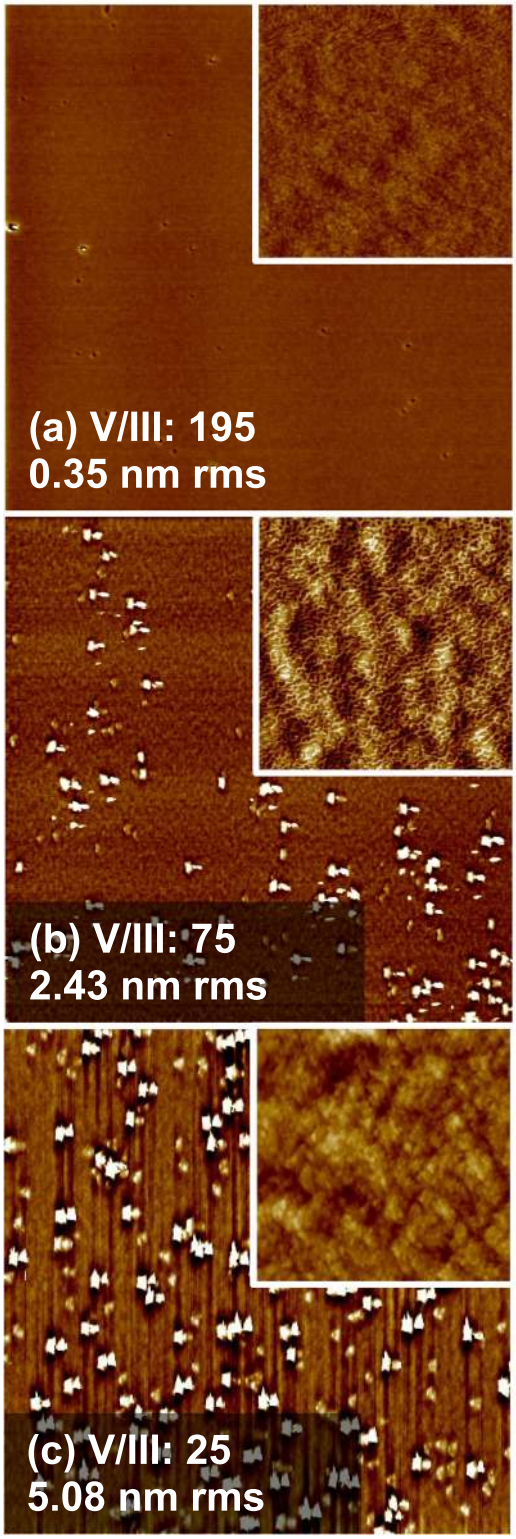

FIG. 27. (Color online) (a)–(c) AFM images ($15 \times 15\,\mu m^2$, 15 nm z-scale) of InGaAs(110) showing effect of V/III ratio at $T_g = 280$ °C (Insets: $1 \times 1\,\mu m^2$ AFM images, 5 nm z-scale). Rms roughness values averaged over $225\,\mu m^2$.

3. InAlAs(110): Summary

The growth of smooth InAlAs on InP(110) is possible using low T_g and high V/III, although defects from stacking faults and excess arsenic impair the optical quality. Overall, our recommended growth conditions for InAlAs(110) follow Brown *et al.*: $T_g = 280$ °C and V/III ratio = 80.[64] However, this recommendation is tentative, since substantial improvements are needed to improve the radiative efficiency.

D. InGaAs on InP(110)

1. InGaAs(110): Surface morphology

We studied the effect of growth conditions for 200 nm InGaAs(110) grown at 0.17 μm/h. For a fixed V/III = 75, the effect of T_g on surface morphology is shown by the Nomarski images in Fig. 26. A high density of trapezoidal hillocks appeared at all T_g, increasing in size and decreasing in density as T_g was increased. The effect of T_g on InGaAs(110) morphology in Fig. 26 is very similar to the trend noted by Yasuda *et al.* for InAlAs(110);[38] very low T_g is required to eliminate hillock formation. However, even at 280 °C, faint hillocks can still be seen by Nomarski, albeit with weak contrast [Fig. 26(d)]. We conclude therefore that InGaAs requires even lower T_g than InAlAs to achieve smooth growth. The high mobility of Ga adatoms means that even lower T_g is required to prevent their incorporation into hillocks. As for InAlAs(110), we observed a streaky RHEED (1 × 1) pattern for InGaAs(110) growths at 280 °C.

The faceted hillocks on both InGaAs(110) and InAlAs(110)[38] exhibit trapezoidal/nearly triangular geometry over a wide range of T_g. The hillocks have mirror symmetry along the in-plane [001] direction, as reported for GaAs(110) buffers.[101] For InGaAs and InAlAs, the asymmetric morphology is indicative of different adatom incorporation rates on different hillock facets, similar to GaAs(110).[101] The formation of facets indicates that the (110) surface is less energetically stable than the new facets that emerge. Our results suggest that suppressing adatom diffusion kinetics through the use of low T_g prevents adatoms from incorporating into hillocks.

The influence of V/III ratio on InGaAs(110) morphology is shown in Fig. 27 for samples grown at $T_g = 280$ °C; the sample at V/III = 75 is the same as in Fig. 26(d). Small hillocks and hillock pairs clearly remain for all V/III ratios up to ~75. The presence and morphology of hillocks on GaAs(110) have been attributed to asymmetric adatom incorporation along the [001] direction,[101] which may also produce the hillock pairs observed here. Hillock size and density both decreased with increasing V/III, disappearing entirely at V/III = 195 and yielding a smooth surface with a $15 \times 15\ \mu m^2$ rms roughness of 0.35 nm. Elevated V/III thus has the same effect as reduced T_g, where lower adatom mobility prevents adatom incorporation into faceted hillock structures.

Although low T_g and high V/III ratio promote smooth InGaAs and InAlAs(110) growth, these conditions also create point defects that degrade the optical and electrical properties, as discussed below. We thus attempted to increase T_g of the InGaAs(110) to 320 °C, while maintaining a high V/III of 195 (not shown). Hillocks formed once again, with size and density similar to that of Fig. 27(b). We conclude that low T_g is essential for smooth InGaAs and InAlAs buffer growth on (110) surfaces.

2. InGaAs(110): Electrical properties

The effects of T_g and V/III ratio on n_0 are shown in Figs. 28(a) and 28(c). InGaAs(110) samples grown with $T_g > 350$ °C were too resistive to measure, and all other

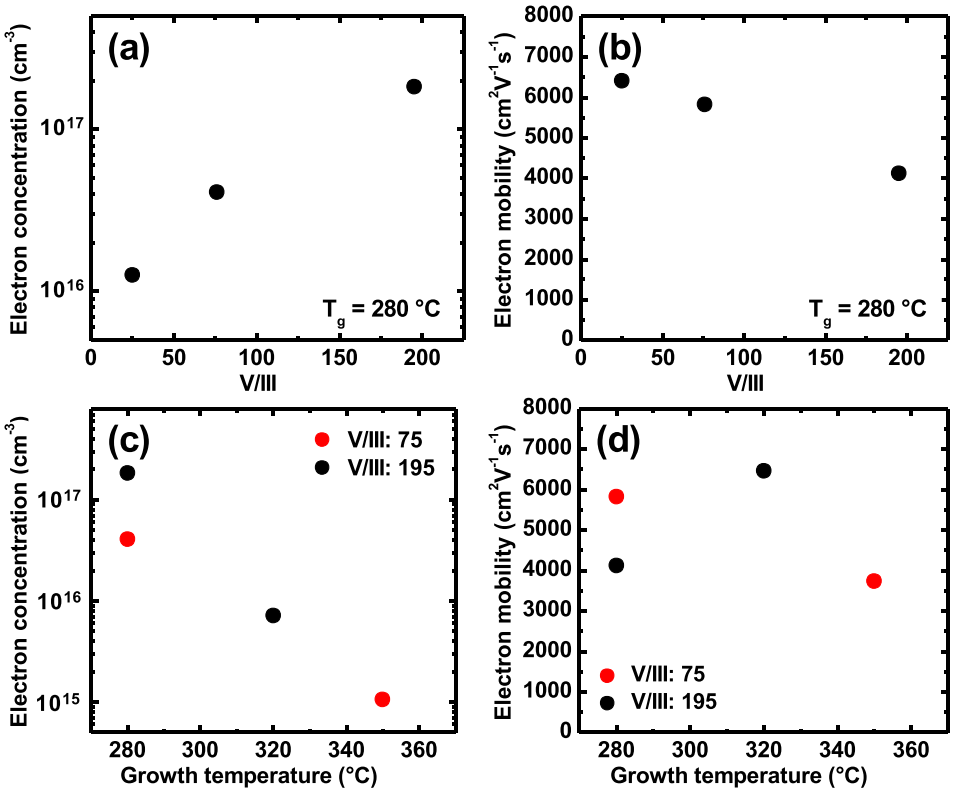

FIG. 28. (Color online) Effect of V/III ratio on (a) n_0 and (b) μ_n of InGaAs(110) samples grown at 280 °C. Effect of T_g on (c) n_0 and (d) μ_n of InGaAs(110) samples grown at V/III of 75 and 195. Hall measurements done at 300 K.

samples were unintentionally n-type. T_g strongly affects n_0 values [Fig. 28(c)], raising n_0 from 1×10^{15} to $4 \times 10^{16}\,\mathrm{cm}^{-3}$ as T_g was reduced from 350 to 280 °C, for V/III = 75. Similar trends in n_0 values have been reported for (001)-oriented III–Vs grown in this low T_g range, including GaAs (Ref. 114) and InGaAs.[115] As T_g is reduced, the arsenic desorption rate falls, allowing a higher amount of arsenic to incorporate into the crystal than normally allowed by stoichiometry. Excess arsenic creates antisite defects (As_{Ga}),[114] occupying cation sites in the crystal lattice and thereby functioning as electron donors.[116] The density of As_{Ga} defects increases, and hence n_0 in the InGaAs increases at lower T_g.[114] We observed a similar increase in n_0 for InGaAs(110) when V/III ratio was increased, as shown in Fig. 28(a). For samples at 280 °C, increasing V/III from 25 to 195 increased n_0 from 1×10^{16} to $2 \times 10^{17}\,\mathrm{cm}^{-3}$. This behavior is again consistent with elevated levels of As_{Ga} antisite defects in the crystal as a result of the higher As_4 overpressure.

The effect of growth parameters on μ_n is shown in Figs. 28(b) and 28(d) for samples grown at 280 °C. As V/III ratio was increased we observed a monotonic decrease in μ_n, which is likely caused by impurity and Coulomb scattering from elevated levels of As_{Ga}. Charged and neutral states of As_{Ga} are typically present after low temperature growth,[114] and both contribute to electron scattering.

The effect of T_g on μ_n is more complex, such that the T_g trend depends on V/III ratio. At V/III = 195, μ_n increases with increasing T_g, while for V/III = 75, μ_n decreases with T_g. For V/III = 195, the improvement in μ_n with T_g corresponds to the observed decrease in n_0 shown in Figs. 28(c) and 28(d). This can be explained by a reduction in impurity scattering from charged As_{Ga}, since As_{Ga} concentration decreases with increasing T_g.[114,115] The unexpected μ_n trend at V/III = 75 is difficult to elucidate, but may be related to hillocks that become larger at lower V/III. Christou *et al.* have shown that antiphase domains can cause rough InAlAs/InGaAs(110) surfaces.[117] Roughening and defects associated with the hillocks are scattering sources that may reduce μ_n, but further work is needed to confirm this hypothesis. We note that the sample grown at 400 °C and V/III = 75 was too resistive for Hall measurement, which could be caused by further degradation in μ_n as larger hillocks form. In summary, the electrical properties of InGaAs(110) are influenced by a combination of factors including arsenic antisite defects, and possibly hillocks.

Overall, the lowest n_0 value for InGaAs(110) was achieved under the lowest V/III (~25) and the highest T_g (≥350 °C) conditions explored in this study. Meanwhile, the best μ_n values were obtained at higher T_g (320 °C) and high V/III to minimize As_{Ga}, or low T_g (280 °C) and low V/III, where hillocks play a weaker role. Under these guidelines, $\mu_n \sim 6500\,\mathrm{cm}^2/\mathrm{V\,s}$ and $n_0 \sim 1 \times 10^{16}\,\mathrm{cm}^{-3}$ were obtained in this work; these are the highest μ_n values obtained in the present work, but still substantially lower than achieved on the (001) surface.[84]

3. InGaAs(110): Photoluminescence

InGaAs(110) PL is sensitive to T_g and V/III ratio as shown in Fig. 29. As in the case of InAlAs(110), InGaAs(110) PL is weak at 300 K, so we performed measurements at 77 K. Since PL intensities were affected by sample positioning in the cryostat, the spectra in Fig. 29(a) are normalized. All InGaAs samples show a primary PL peak at 790–810 meV, while additional, low-energy peaks emerge for samples grown at higher T_g [Fig. 29(a)]. Our PL measurements agree with the calculated band gap of 804 meV for lattice-matched InGaAs at 77 K. Unlike InAlAs(110),[64] the InGaAs(110) emission appears less susceptible to shallow luminescent defects formed during low temperature growth. At V/III = 75, as T_g was raised from 280 to 350 °C a new peak emerges at 763 meV, and at 420 °C, another peak at

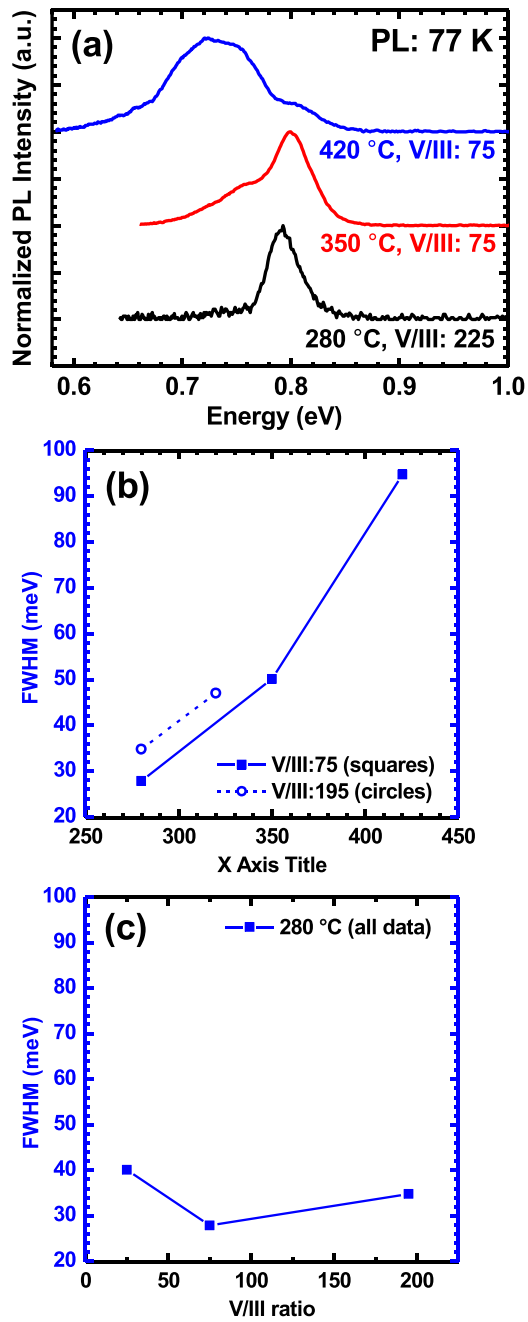

FIG. 29. (Color online) PL at 77 K for InGaAs(110) grown under different conditions. (a) PL spectra of representative samples. Effect of (b) T_g and (c) V/III ratio on PL FWHM.

730 meV is also present. At these higher temperatures, excess-arsenic incorporation in InGaAs is greatly mitigated,[115] suggesting that the new peaks are not arsenic-related defects. These peaks instead form concurrently with large faceted hillocks on the InGaAs(110) surface. Facet-dependent incorporation rates have been observed for a number of materials including GaAs,[118,119] InGaN,[120] and InGaAsP.[99,100] For the latter two materials, different incorporation rates of each atomic species produce orientation-dependent alloy compositions. Similarly, for InGaAs(110), indium and gallium are likely to incorporate at different rates on different facets, leading to the appearance of the additional PL peaks. Note that the increase in the PL linewidth with T_g is also consistent with increased compositional nonuniformity.

The effects of growth conditions on PL linewidth are shown in Figs. 29(b) and 29(c). In Fig. 29(b), a strong increase in FWHM is associated with increasing T_g, reflecting the formation of multiple PL peaks as hillocks emerged. The V/III trend in Fig. 29(c) shows that higher V/III ratios are needed to maintain lower linewidths. In this case, separate peaks were not discernable in the spectra (not shown), but small hillocks were present at V/III = 25 that could be responsible for broadening the linewidth. Thus, the low T_g and high V/III conditions corresponding to smooth surfaces are also most favorable for narrowing PL linewidths.

4. InGaAs(110): Summary

In summary, InGaAs on InP(110) requires very low T_g (~280 °C) and very high V/III ratios (~200) to form smooth surfaces. Electrical properties can be improved outside of this growth window, but only at the cost of hillock formation. The highest μ_n and n_0 values were observed at low V/III ~ 25 with $T_g = 280$ °C, or at high V/III ~ 195 with $T_g = 320$ °C. These characteristics appear to be influenced by As_{Ga} incorporation as well as hillock formation. The narrowest PL linewidths were achieved at conditions that promoted smooth morphologies. At present the morphological, electrical and optical properties of InGaAs(110) cannot be simultaneously optimized, and the choice of growth conditions must therefore be informed by the desired application for the material.

VI. EFFECT OF SURFACE ORIENTATION ON GROWTH PARAMETERS

In this section, we compare trends in material properties across different surface orientations. We compare our experimental results for InAlAs and InGaAs to previous GaAs results found in the literature (from Secs. III A, IV A, and V A). We present parameter space maps as a roadmap to the optimal growth conditions for InAlAs, InGaAs and GaAs on (111)A, (111)B, and (110) surface orientations.

A. Effects of surface orientation on surface morphology

Surface orientation and substrate offcut directly determine the dominant type of morphological defects that form during growth and also dictate the best strategy for mitigating these defects. For a given surface orientation, the morphological features observed are very similar for InAlAs, InGaAs, and GaAs. GaAs homoepitaxy on exact (111)A, (111)B, and (110) surfaces results in hillocks that share the symmetry of the crystal lattice, as discussed in Secs. III A, IV A, and V A. GaAs(110) forms hillocks elongated along [001], reflecting the twofold surface symmetry, while the hillocks for GaAs(111)B and (111)A are threefold symmetric.[73,85] Hillocks on GaAs(111)B are broader and shorter than those on GaAs(111)A, since the former hillocks are composed of vicinal surfaces.[85] The major surface features observed for InAlAs and InGaAs in this work are reviewed in Fig. 30. The InAlAs(111)B and InGaAs(111)B morphologies are notably free from hillocks as a direct result of the 2° substrate offcut. Instead, the (111)B surfaces are dominated by closely spaced

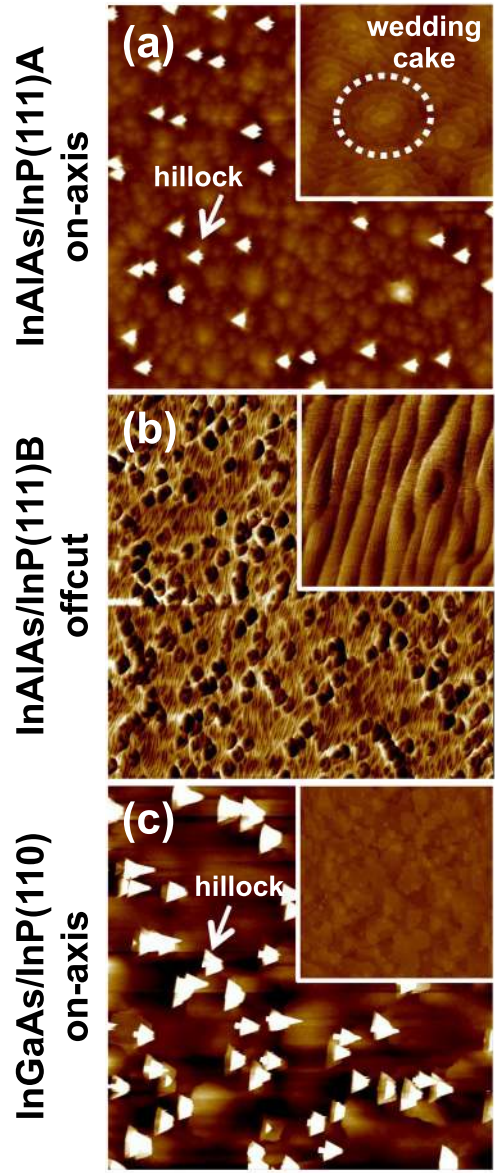

FIG. 30. (Color online) AFM images (15 × 15 μm^2, 15 nm z-scale) highlighting major surface features for InAlAs and InGaAs buffers grown on (a) (111)A, (b) (111)B, and (c) (110) InP surfaces (Insets: 1 × 1 μm^2, 5 nm z-scale).

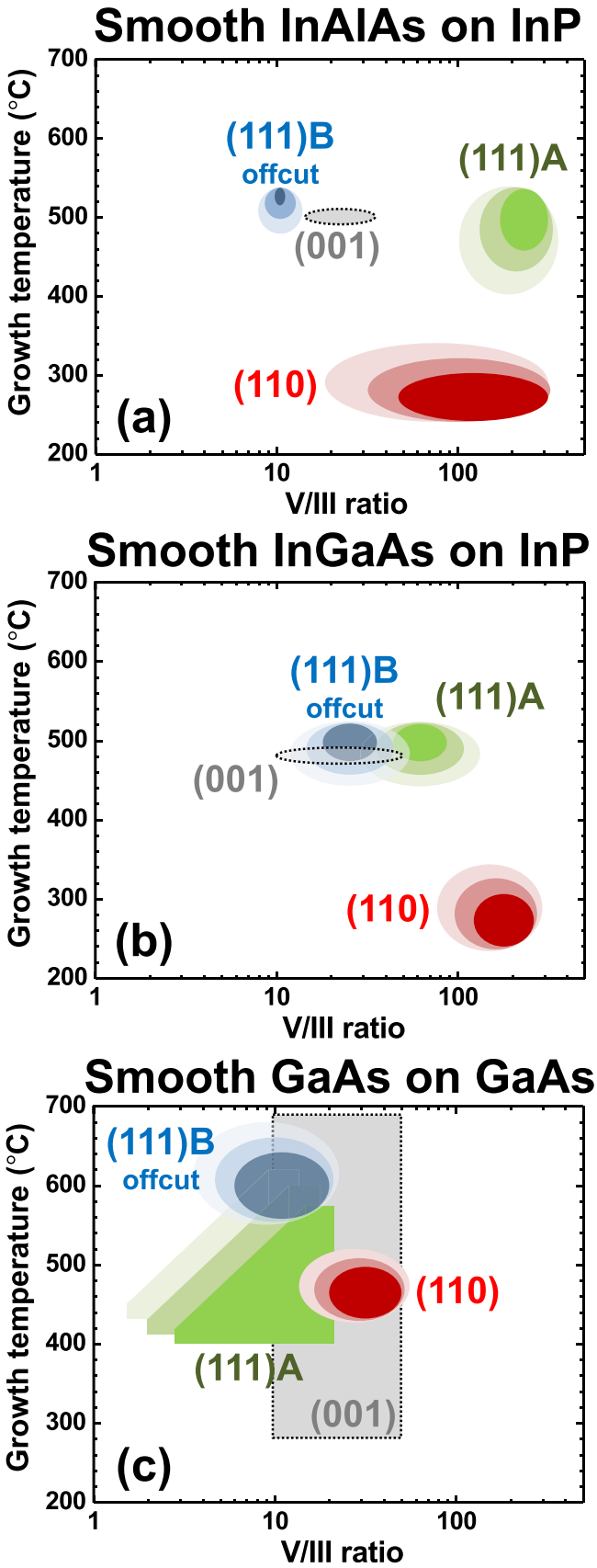

FIG. 31. (Color online) Growth windows for optimizing surface morphology of (a) InAlAs, (b) InGaAs, and (c) GaAs on different surface orientations. Contours of increasing intensity show how growth conditions improve surface roughness. In (c), parameters for optimal GaAs on different surfaces are taken from references cited in Secs. III A, IV A, and V A.

offcut steps, which can group together into larger morphological defects such as step-bunched pits and macrosteps.

Figure 31 shows the optimal growth windows to achieve smooth surfaces for InAlAs, InGaAs and GaAs for each of the low index surfaces discussed in this work. The darker shaded areas indicate conditions where the surface is smoothest. Smooth GaAs (001) homoepitaxy is possible across a wide range of temperatures and V/III ratios. In contrast, the growth windows for other materials are typically much narrower, outside of which we see surface roughening and crystalline defects.[121,122] Note that the GaAs temperature range extends to higher values than InAlAs and InGaAs for some surface orientations. These high temperature ranges are not compatible with indium containing compounds due to their lower decomposition temperature of ~550 °C. Turning to non-(001) surfaces, the optimal growth conditions have a limited range for most materials and generally do not overlap for the different surface orientations. As a result, ideal growth conditions for (001) surfaces often make poor starting points for investigating growth on (110) or (111) surfaces.

Crystallographic orientation plays a prominent role in determining the influence of growth conditions on morphology, while the material itself (e.g., InGaAs versus InAlAs) plays a lesser role. The three non-(001) substrate orientations each require a different growth strategy to achieve a smooth surface. For most (110) and (111)A materials discussed in this work, hillocks increase in size and decrease in density as adatom diffusion length increases. In these cases, the two limiting approaches for achieving surface smoothness are (1) to lower adatom mobility until hillocks shrink to zero size; or (2) to raise adatom mobility to increase the spacing between the hillocks as much as possible.

1. Growth on (111)A

For (111)A growth, low adatom mobility conditions fail to smooth the surface for some materials because either new surface defects form (InAlAs) or because the hillocks do not reach zero size (InGaAs). Therefore we recommend adopting a high adatom mobility strategy that uses high T_g to lower the hillock density as much as possible. In contrast, GaAs(111)A can be grown using low adatom mobility conditions, since morphological problems were not observed at low T_g.[59] Between InAlAs and InGaAs, V/III ratio plays a much different role. Smooth InGaAs(111)A requires lower V/III, consistent with raising adatom mobility to remove hillocks. InAlAs(111)A requires higher V/III ratios to smooth the surface, a trend that suggests it behaves more like GaAs(111)A, in which hillocks are associated with the low arsenic sticking coefficient.[59]

The (111)A surfaces of InAlAs and InGaAs have the additional complexity of atomic wedding cakes that arise from the nucleation of 2D islands. GaAs(111)A differs from InAlAs and InGaAs in this respect, since wedding cakes are not observed near the ideal GaAs growth conditions.[27] For InAlAs and InGaAs, growth conditions that reduce the occurrence of wedding cakes, presumably by reducing the 2D nucleation rate, include high T_g and high V/III ratio. This trend nearly overlaps the strategy for hillock reduction in these ternaries, though in

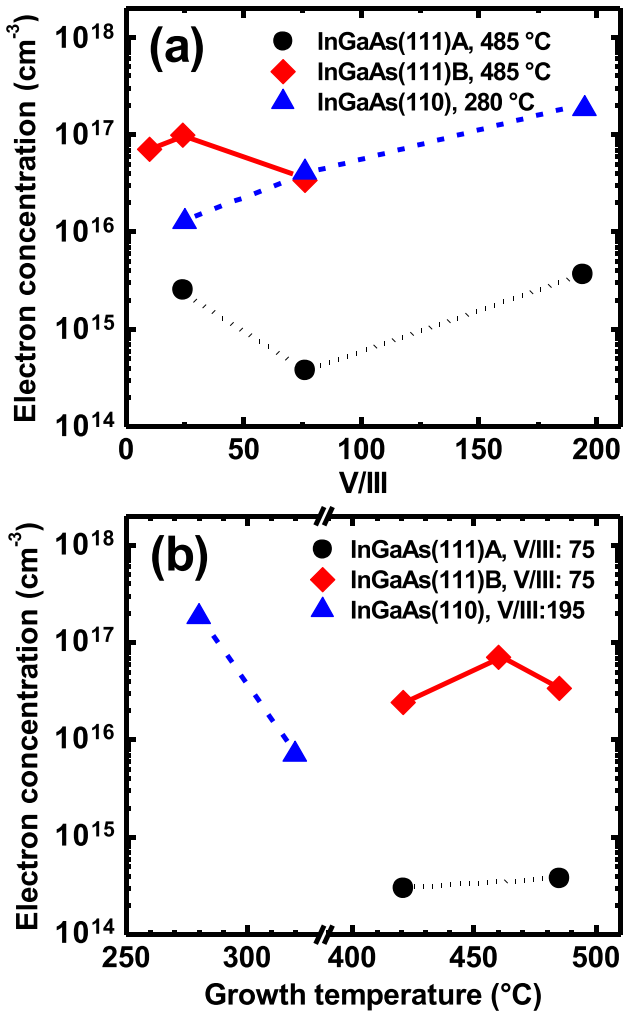

FIG. 32. (Color online) Effect of (a) V/III ratio and (b) T_g on n_0 for InGaAs grown on InP(111)A, offcut (111)B, and (110). Hall measurements done at 300 K.

the case of InGaAs(111)A, V/III ratio requires a slight tradeoff between hillock density and wedding cake roughness.

2. Growth on (111)B

The use of offcut InP(111)B substrates in this work for InGaAs and InAlAs growth changes the relationship between morphology and growth conditions compared to on-axis substrates. Little is understood about the smoothening and roughening mechanisms of offcut (111)B, so we can only comment on empirical trends observed during growth optimization. For InAlAs(111)B and InGaAs(111)B, high T_g is required to avoid step bunching, while in contrast, high T_g causes step bunching for offcut GaAs(111)B.[69] However, the effect of lower T_g on offcut GaAs(111)B has not been reported, and this approach could potentially exhibit similarities with InAlAs and InGaAs(111)B. In addition, the ternary (111)B materials show different forms of roughening for low or high V/III extremes. InAlAs and InGaAs both form pits at low V/III, and facets appear at high V/III. Literature reports suggest that GaAs(111)B is less sensitive to high V/III than the ternaries studied here.[69]

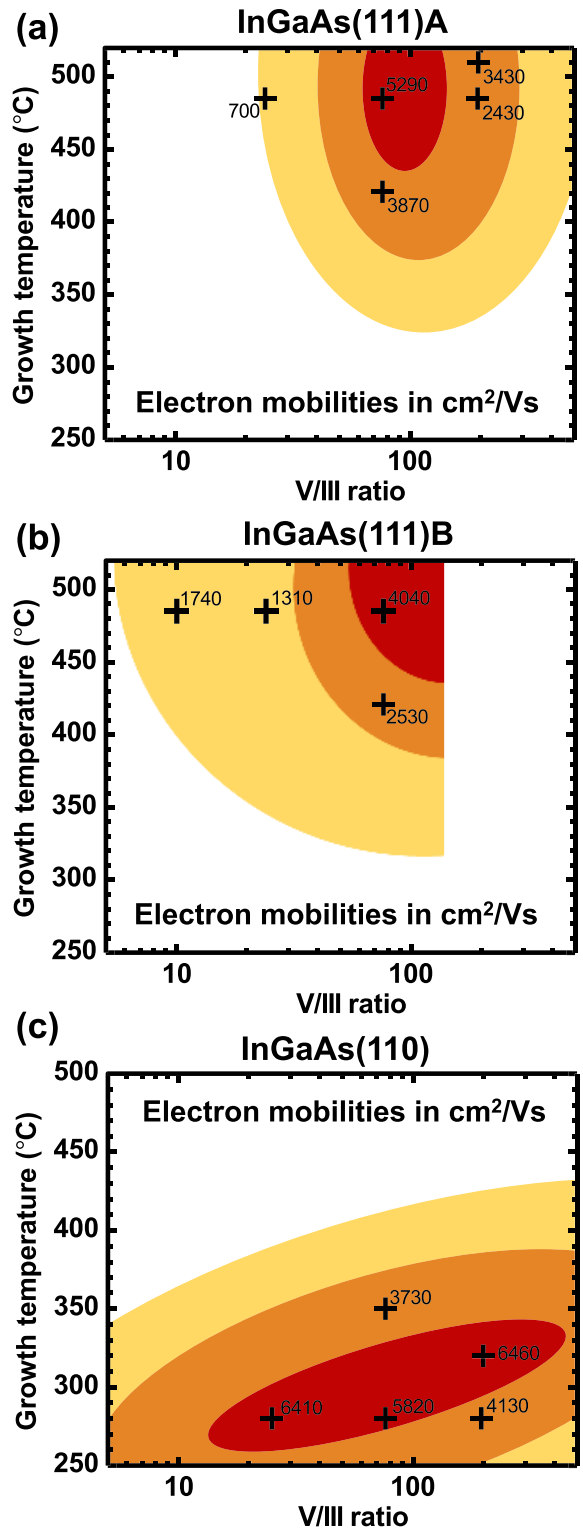

FIG. 33. (Color online) Growth windows for InGaAs μ_n on (a) (111)A, (b) (111)B, and (c) (110) InP. Contours of increasing intensity show how growth conditions improve μ_n. Hall measurements done at 300 K.

3. Growth on (110)

For (110) growth, high adatom mobility is less desirable because of the large hillock size and density observed at higher T_g. Thus, for all materials grown on (110) in Fig. 31, a low adatom mobility approach is preferred where low T_g

and high V/III ratio are used to minimize hillock size. The temperature required to smooth InAlAs and InGaAs (~300 °C) is much lower than required for GaAs (470–500 °C),[104,106] which is a function of the higher surface diffusivity of indium adatoms compared to gallium.

B. Effects of surface orientation on electrical properties

With the exception of InAlAs(111)B, electrical measurements on InAlAs films were not possible. As a result, the discussion here is limited to InGaAs growth. The effect of surface orientation on the electrical properties of InGaAs is independent of the surface orientation to some extent (Figs. 32 and 33). First, all InGaAs samples measured were unintentionally *n*-type, regardless of surface orientation; an *n*-type background is also the norm for In-containing III–V semiconductors on (001) surfaces. Though we have not fully optimized conditions for electrical properties, μ_n values obtained for non-(001) growth are reasonably high at 4000–6500 $cm^2/V\,s$, where $\mu_{n,(110)} > \mu_{n,(111)A} > \mu_{n,(111)B}$.

n_0 varies greatly depending on surface orientation and growth conditions as shown in Fig. 32. The InGaAs(111)A epilayers exhibited the lowest n_0 of $4 \times 10^{14}\,cm^{-3}$ (Fig. 32), a value that is comparable to typical MBE-grown GaAs(001).[123] InGaAs(110) and (111)B had significantly higher $n_0 \geq 6 \times 10^{15}\,cm^{-3}$. Trends in μ_n as a function of T_g, V/III ratio, and surface orientation are shown in Fig. 33. Similar growth conditions were found to optimize μ_n for InGaAs(111)A and (111)B, namely high T_g and high V/III ratio. For both (111) surfaces, these conditions corresponded to lower n_0 (Fig. 32), indicating that reduced charged impurity scattering plays a role. In the case of InGaAs(111)A, improved μ_n also corresponded to reduced hillock density. Though we have not fully optimized conditions for electrical properties, μ_n values obtained for non-(001) growth are reasonably high at 4000–6500 $cm^2/V\,s$, where $\mu_{n,(110)} > \mu_{n,(111)A} > \mu_{n,(111)B}$. However, μ_n values of 6000–10 000 $cm^2/V\,s$ are typical for InGaAs(001) at similar carrier concentrations, suggesting that electron scattering is higher in non-(001) InGaAs.[124] Further optimization of growth conditions and crystal quality should improve the μ_n values on each surface.

Hillocks on the (111)A surface produce substantial roughness and also contain high densities of crystallographic defects, making their elimination crucial to achieving high μ_n. In contrast, InGaAs(111)B surface roughness does not change dramatically with growth conditions, so surface morphology is less of a consideration for electrical properties.

For InGaAs(110), Fig. 33 shows that much lower T_g is required for high μ_n than on the (111) surfaces. Low T_g is essential for smoothing the (110) surface (see Fig. 31), which reduces surface scattering and avoids crystallographic defects associated with the hillocks. However, the optimum point in Fig. 33(c) lies at slightly higher T_g and lower V/III ratio than the InGaAs(110) morphology optimum in Fig. 31. At very low T_g and high V/III ratios, high densities of arsenic-related defects appear that also degrade μ_n.[114,115] Figure 32 illustrates the remarkable increase in n_0 as T_g was lowered from 320 to 280 °C, corresponding to the incorporation of arsenic antisite defects.[114,115] Therefore, the extreme conditions that smooth the morphology do not necessarily improve the electrical properties, and some compromise must be made between the two.

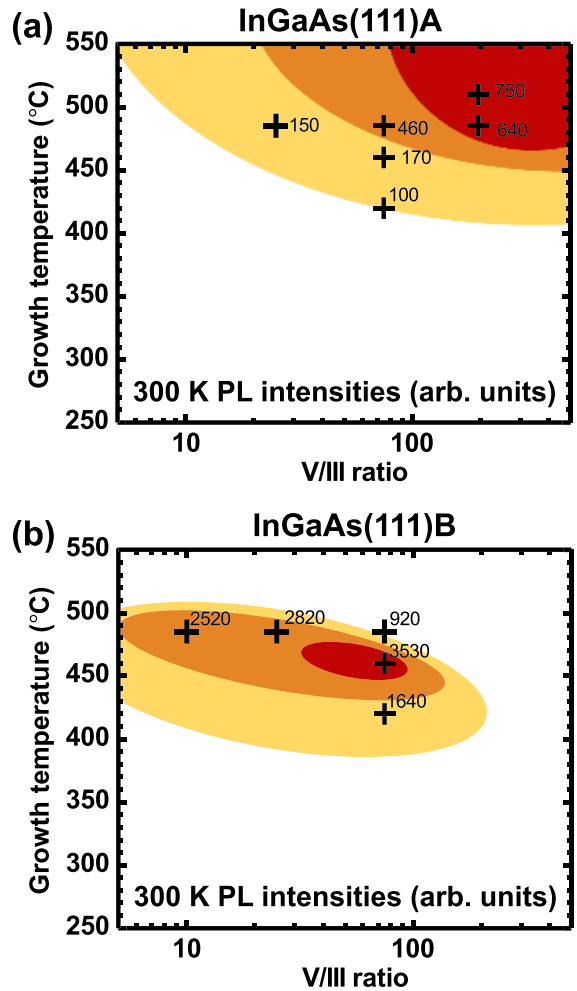

FIG. 34. (Color online) Growth windows for highest PL intensities for (a) InGaAs(111)A and (b) InGaAs(111)B. Contours of increasing intensity show how growth conditions increase PL intensity.

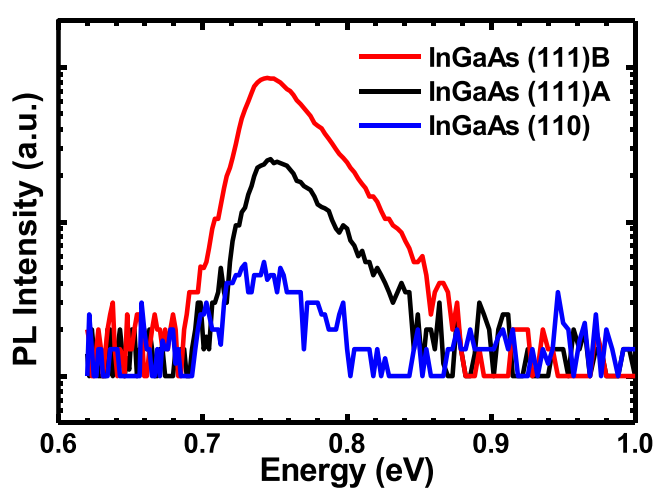

FIG. 35. (Color online) PL spectra at 300 K of brightest InGaAs layers grown here on InP(111)B, (111)A, and (110).

C. Effects of surface orientation on photoluminescence

PL from InAlAs (111)A and (111)B were relatively insensitive to growth conditions, while PL from InAlAs(110) was weak and dominated by defects; it is worthwhile to mention that InAlAs(111)B exhibited integrated intensity ∼40% of InAlAs(001). No strong trends were noted for InAlAs PL, and thus, as in Sec. VI C, we focus our discussion on InGaAs growth.

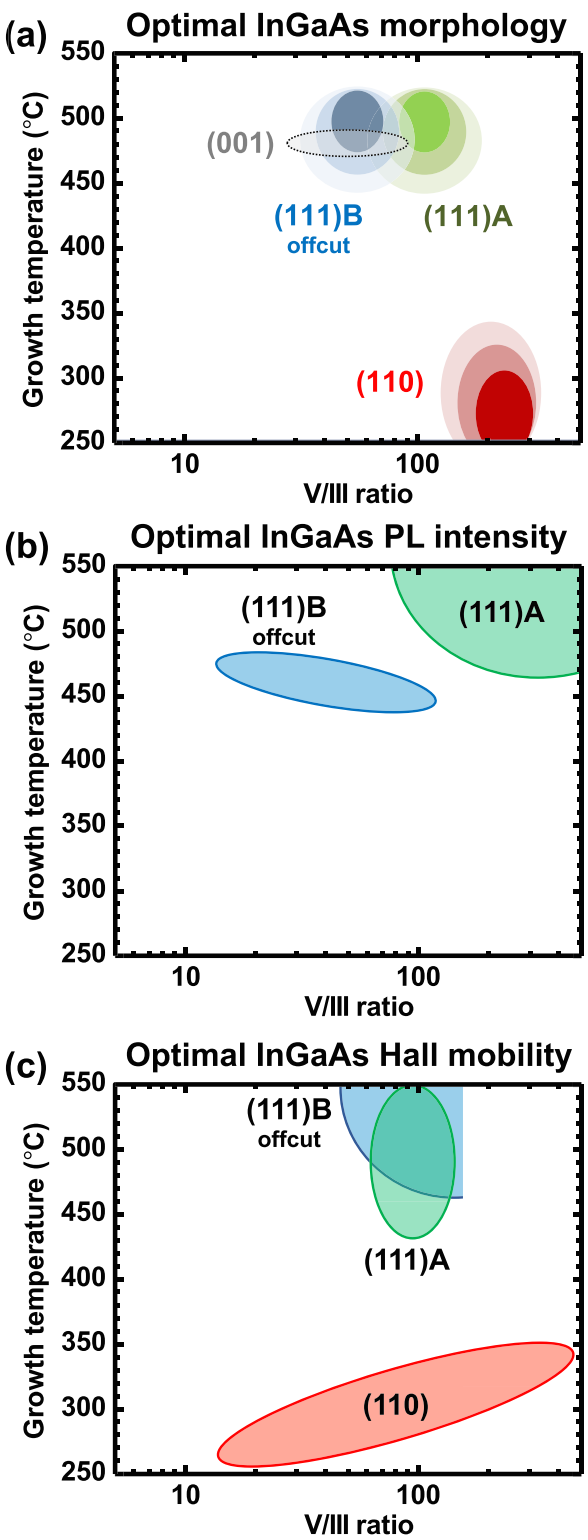

FIG. 36. (Color online) Comparison of InGaAs growth conditions across surface orientations for optimization of (a) morphology, (b) PL intensity at 300 K, and (c) μ_n at 300 K.

PL linewidths on (110), (111)A, and (111)B generally narrowed as the surface became smoother, which suggests that the uniformity of indium and gallium incorporation is associated with surface roughness. For (111)A and (111)B samples, PL linewidth was found to reduce with increasing PL intensity, such that both PL attributes improved simultaneously.

The effect of growth parameters on PL intensity at 300 K for InGaAs (111)B and (111)A is shown in Fig. 34; the low signal-to-noise ratio for PL of InGaAs(110) at 300 K prevented a meaningful analysis for this orientation. Similar to the morphology trends, PL intensity varied significantly with surface orientation. InGaAs(111)A required a higher T_g to optimize PL (∼510 °C) than InGaAs(111)B (∼460 °C). For (111)A, high T_g corresponded to low hillock densities and higher μ_n for InGaAs, both of which provide evidence for higher crystalline quality. In contrast, the moderate T_g used to increase the PL intensity of InGaAs(111)B in Fig. 34(b) corresponded to elevated n_0 levels in Fig. 32. Thus, when interpreting PL intensities, it is important to consider the fact that higher n_0 increases the radiative recombination rate. InGaAs(111)A is influenced by n_0 to a weaker extent, in that the high V/III used to improve the PL also slightly increased the n_0 level. However, the T_g trend for InGaAs(111)A is not related to n_0 and instead indicates improvement in optical quality.

We compare the PL spectra of InGaAs (111)A, (111)B, and (110) in Fig. 35. The PL intensity of InGaAs(111)B is the strongest, four times more intense than that of InGaAs(111)A and nearly 20× stronger than InGaAs(110). That PL from InGaAs(111)B is stronger than InGaAs(111)A is largely attributed to the former's much higher n_0 (Fig. 32). The PL of InGaAs(110) is weaker than the others due to the low T_g and concomitant arsenic-antisite defects. InGaAs(111)A and InGaAs(111)B have good optical quality, while further work is needed to minimize nonradiative recombination in InGaAs(110) and improve luminescence.

D. Overview of buffer optimization

Finally, we compare the effect of surface orientation on the simultaneous optimization of the morphology, electrical, and optical properties of InGaAs. Figure 36 compares the points in parameter space that optimize the surface morphology (rms roughness), the PL intensity, and μ_n for InGaAs on each surface orientation. InGaAs(111)A has the best overlap of properties in parameter space, where the highest μ_n, strongest PL, and lowest hillock density all occur at V/III ∼ 75 and ∼510 °C. For InGaAs(111)B, some separation exists between optimal surface roughness and the highest μ_n, where a higher T_g and V/III ratio were needed for better electrical properties. InGaAs(110) is the most difficult to jointly optimize, since surface morphology is anticorrelated with μ_n. Optimal morphology was produced at low T_g and high V/III ratio to suppress hillocks, while higher T_g and low V/III

were needed to mitigate excess-arsenic for improvements in μ_n. The combined trends for each surface show the extent to which compromises must be made when optimizing material properties. While precise growth conditions are expected to vary between different research groups and different MBE chambers, we believe that the trends we have reported will be robust and useful to other researchers.

VII. CONCLUSIONS

We have presented a literature review and experimental investigation into the optimal conditions for MBE growth of InAlAs and InGaAs on InP (111)A, (111)B, and (110) substrates. We report trends in growth parameters toward the optimization of surface morphology, electrical properties, and optical quality. We have emphasized morphological optimization, and for each surface, we have shown that atomic level smoothness is possible, and that large morphological defects can either be eliminated or minimized. Growth conditions for optimal smoothness vary substantially with surface orientation. However, we report that different materials appear to have similar growth trends for a given surface orientation [e.g., InGaAs(110) behaves similarly to InAlAs(110)], meaning that insights learned from a particular surface orientation could perhaps be used to develop a range of materials on that same surface.

Strong electrical and optical properties can be obtained from most of the materials studied in this work, despite the challenges with achieving flat surface morphologies. We measured electron mobilities at 300 K as high as 4000, 5300, and 6500 $cm^2/V\,s$ for InGaAs on InP (111)B, (111)A, and (110), respectively. InAlAs(111)B was particularly noteworthy in its optoelectronic properties, exhibiting higher μ_n and comparable PL intensity to InAlAs(001). We anticipate that the trends in electrical and optical properties we report here will enable the growth of device quality InGaAs and InAlAs on each of these surfaces.

This work provides a foundation for the development of novel materials and devices on the (111) and (110) surfaces of InP. As an example, the InAlAs and InGaAs layers explored here have already been employed to facilitate growth of highly tensile quantum dots on (111) and (110) surfaces.[9,10,30] This achievement allows strong bandgap tuning for long wavelength optoelectronics. Furthermore, symmetric QDs with ideal electronic characteristics for entangled photon emitters have been demonstrated using the InAlAs/InP(111)A buffers achieved in our experiments.[10,21] GaAs(110) quantum wells have been used to make encouraging spintronic devices,[33–36] and the developments we report here may soon help enable InP(110)-based spintronics. Smooth buffer layers on InP (111) surfaces are anticipated to provide ideal templates for the growth of topological insulators and transition metal dichalcogenides. Finally, MOSFETs that employ smooth, high-mobility III–V materials grown on (111) surfaces are predicted to have characteristics that rival silicon. III–Vs based on (111) and (110) materials are anticipated to drive a host of new technologies in the upcoming years.

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