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Invited Review

Review of carbon nanotube nanoelectronics and macroelectronics

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Abstract

Carbon nanotubes have the potential to spur future development in electronics due to their unequalled electrical properties. In this article, we present a review on carbon nanotube-based circuits in terms of their electrical performance in two major directions: nanoelectronics and macroelectronics. In the nanoelectronics direction, we direct our discussion to the performance of aligned carbon nanotubes for digital circuits and circuits designed for radio-frequency applications. In the macroelectronics direction, we focus our attention on the performance of thin films of carbon nanotube random networks in digital circuits, display applications, and printed electronics. In the last part, we discuss the existing challenges and future directions of nanotube-based nano- and microelectronics.

Keywords: carbon nanotube, nanoelectronics, macroelectronics, transistor, circuit, electronics, application

(Some figures may appear in colour only in the online journal)

Introduction

Recently, the feature size of semiconductor transistors has reached the nanometer regime following the scaling trend described by Moore's law. In the nanoelectronics field, carbon nanotubes (CNT) have advantages owing to their one-dimensional geometry. The inherently small geometric size of single-wall carbon nanotubes (SWCNTs) of ~1 nm leads to the optimization of the coupling between the gate and the channel of a transistor and provides great potential in the application of nano-scale devices and circuits [1–16]. The chemical bonds of all the C atoms in a CNT are satisfied without dangling bonds, so a high dielectric constant and crystalline insulator can be applied in CNT-based devices [17].

In the application of nanoelectronics, semiconducting SWCNTs are usually used as the channel material. Due to the one-dimensional transport and long mean free path (in the order of a few hundred nanometers), CNT can offer scattering-free ballistic transport and enable the possibility of ballistic transport for short channel devices, resulting in low power dissipation [17–19]. The good thermal conductivity of SWCNTs also brings benefits for reducing power consumption in devices and circuits. All these unique geometrical, electronic, thermal, chemical and mechanical properties will make carbon nanotube field-effect transistor (CNTFET) very competitive in future electronics [20–22]. In order to fulfill the potential of CNTs for nanoelectronics, significant progress has been made in the past and will be discussed in this review. On the material side, controlled synthesis of CNT has advanced from chemical vapor deposition (CVD) of single-walled nanotubes to synthesis of predominantly semiconducting nanotubes [23], and then chirality-controlled synthesis of CNTs using vapor phase epitaxy (VPE) [24], On the device side, the nanotube field has witnessed progress from demonstration of ballistic transistors based on individual nanotubes, to transistors and circuits based on aligned nanotubes synthesized, and more recently microprocessors based on p-type aligned nanotube transistors [8, 18, 25, 26]. Furthermore, n-type CNT transistors have been demonstrated using various means [27–29], and large-scale assembling of CNT has been reported using Langmuir–Schaefer assembly [30], both of which are important building blocks for nanotube

nanoelectronics. In parallel, significant advance has also been made with nanotube-based RF electronics [11, 16, 31], with demonstration of planar RF transistors, self-aligned T-gate RF transistors, transistors with embedded bottom gate, and RF circuits such as mixers and frequency doublers [11, 12, 16, 31].

In the application of macroelectronics, nanotubes have many advantages as well, transistors based on CNT random network exhibit superior properties in terms of their electrical performance, reliability, flexibility, transparency, and printability [32–41], so multifunctional and multipurpose transistors and circuits become feasible. The random network CNT thin-film transistors (TFTs) use semiconducting enriched nanotubes as the channel material for the transistors, hence the effect of metallic nanotubes in the channel will be mitigated, and there will be no additional post-fabricated metallic tube removal process required. With the advancement in the separation of CNTs metallic and semiconducting, i.e. separation of semiconducting tubes from metallic ones, CNT solution with exceptional high semiconducting tube purity (>99.99%) can be envisaged for the future [42]. Moreover, the CNT-based TFTs exhibit excellent transparency and flexibility, which are critical criteria for the development of transparent and flexible electronics. In addition, the CNT thin films can be deposited at room temperature which enables them to be used for flexible electronics on polymeric substrates. The fabrication process of CNT TFTs is compatible with standard printing techniques; as a result, it can be readily adopted for the development of low-cost and large-scale printed electronics.

Many research groups have demonstrated the potential of nanotubes as building blocks in applications such as TFTs, back panel electronics for displays, flexible electronics, and printable electronics [33, 36, 38]. CNT network-based field-effect transistors (FETs) demonstrate a mobility tantamount to that of amorphous silicon based transistors or organic FETs [34]. CNT random network is a desirable material for the transistors used in drivers for display applications such as active matrix organic light-emitting diode (AMOLED) arrays [35]. More importantly, CNT network-based FETs can be processed at room temperature, which is essential for electronics fabricated on flexible substrates [43]. The low temperature processing aspect of CNT FETs has proven to be more advantageous than other materials such as polycrystalline silicon [36]. In addition to the aforementioned merits of CNT-based transistors, it is also a semiconducting material that can be printed, and this allows it to be an essential component in the development of low-cost, scalable, printed electronics [39, 41, 44]. In spite of the above-mentioned progress, more efforts will be needed to address the issues of nanotube assembly and integration, metallic nanotube removal, diameter and chirality control, and rendering of n-type CNT transistors stable in air for the long term.

CNTs possess exceptional high specific surface area, which makes them ideal for sensing applications. It has been demonstrated as early as 2000 that an individual CNT transistor was sensitive to low concentrations of NO_2 and NH_3 [45]. This was interpreted by the charge transfer mechanism between gases and CNTs. Briefly, the exposure of CNTs to electron-withdrawing gases such as NO_2 (or electron-donating gases such as NH_3) would increase (or decrease) the hole concentration in CNTs, thus leading to an increase (or decrease) in the conductance of the CNT transistors. Later, Schottky barrier modulation was also shown to be responsible for some CNT sensors, where the Schottky barrier formed between CNT and metal electrodes and the exposure of devices to gases led to a change in the height of such a Schottky barrier [46]. Further developments have shown that the CNT sensors can detect 100 ppt level of NO_2 gas [47]. In addition, the functionalization of CNT surface renders selectivity to CNT sensors, i.e., the sensor will be only responsive to a specific analyte [47–49]. Very recent development in this direction also shows that the diameter and chirality of CNTs have effects on the sensitivity and stability of CNT sensors [50]. There are several review articles about CNT sensing applications published already [48, 51]. In our review paper, we will focus on electronic applications of CNT.

In this review, we will first discuss the digital electronics application of CNT toward nanotube-based computing system and the key factors including realization of N-type CNTFET and large-scale assembling of CNT. Then we will discuss the radio frequency (RF) electronics application of CNTFET as a competitive candidate in high-performance RF designs and systems. In the second part of this review, we will discuss the progress in the area of CNT random network-based transistors fabricated through direct CVD synthesis and transfer of CNTs, and the applications in digital circuits, display applications, and printed electronics. In the last part, we will discuss the further development of carbon nanotube-based electronics.

1. Carbon nanotube nanoelectronics

1.1. Quantum simulation of carbon nanotube transistor

CNT have been predicted to have superior electronics properties and have drawn a lot of attention in the transistor application due to the outstanding carrier mobility and velocity. In order to understand the transistor physics and to optimize the device performance, researchers have performed numerical simulation together with experimental study of transistors made of individual CNT. Techniques including low-Schottky-barrier contact and high-k dielectric insulator have been introduced to short-channel CNT transistors. Significant progress has been made in the simulation and modeling of CNTFET for further understanding [52–55]. Among these methods, Guo *et al* developed a self-consistent quantum simulation to study CNT device physics and electrical performance [55]. The non-equilibrium Green's function (NEGF) calculation was introduced in the ballistic quantum simulation of single CNT transistor as shown in figure 1(*a*) Staring from dialogizing the Hamiltonian matrix in a discrete real space lattice and solving the Schrödinger equation, charge density can be derived from Green's function, which can be further iterated in the Poisson equation. Through the self-consistently simulated iteration between NEGF transport and the Poisson equation, the electrical parameters of the CNT transistor including charge density and current can be obtained (figure 1(*b*)). As presented in the schematic of figure 1(*c*), a CNT transistor of channel length of 50 nm was fabricated with

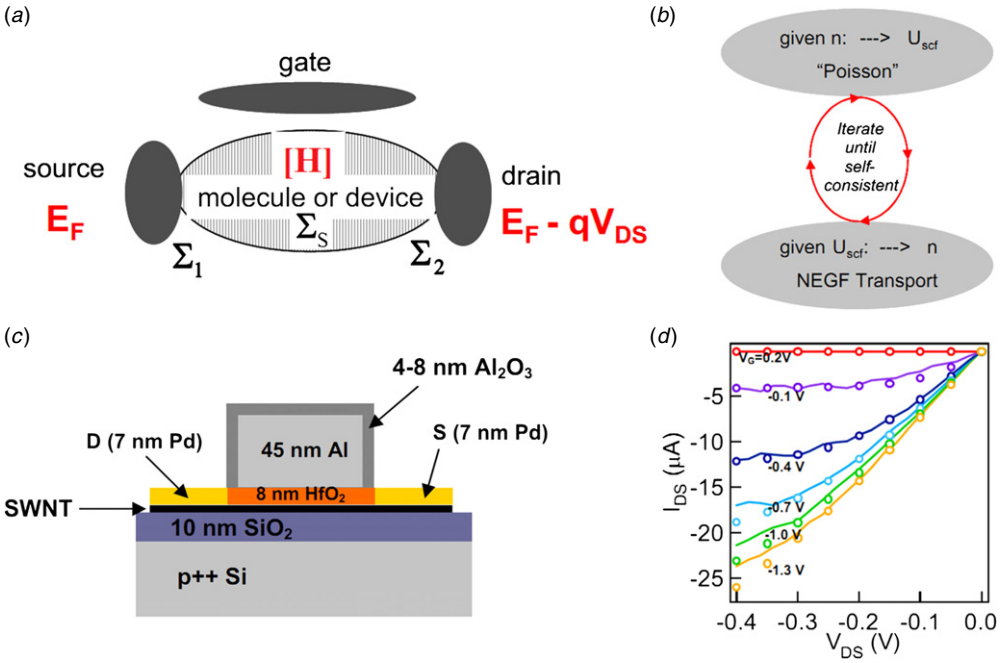

Figure 1. (*a*) Diagram showing the quantities in NEGF simulation. (*b*) Diagram showing the self-consistent iteration between NEGF transport and electrostatic Poisson equation. (*c*) Device schematic of single CNT transistor with 50 nm channel length. (*d*) Output characteristics of the single nanotube device in (*c*). Symbols are quantum simulation result, and solid lines are experimental measurement data. Adapted with permission from [55]. Copyright UMI-Dissertations Publishing (2004).

Palladium as metal contact and HfO_2 as gate dielectric. Guo *et al* derived the electrical characteristics of the CNT transistor based on the NEGF simulation, which matches well with the experimental data illustrated in figure 1(*d*). Furthermore, the scaling limit and diameter dependence of CNT transistors with Schottky contact have been discussed in this work as well, which helps to understand the device physics and further optimize the CNT transistor [55].

1.2. Digital electronics

Due to their high carrier mobility and current-carrying capacity, semiconducting SWCNTs are good candidates for next-generation nanoelectronics. For the past decade, CNT have attracted tremendous attention for their applications in digital nanoelectronics [4–7].

1.2.1. Controlled synthesis of carbon nanotubes. Various techniques have been developed for the growth of SWCNTs since their first discovery, and the most commonly used methods include arc discharge [21, 22, 56], laser ablating [57, 58], and CVD [59, 60]. Among these three techniques, CVD process has generated significant interest over the years due to its relatively low growth temperature, easy operation, good controllability, and low cost. However, the available synthesis methods usually produce inhomogeneous mixture of nanotubes in chirality, electronic type, bandgap, etc, which limit the use of CNT in many applications. It is generally believed that the growth condition, catalyst, and supporting substrate play imperative roles in determining the nanotube properties. Therefore, intensive efforts have been made to investigate the growth mechanism and the effect of various process parameters involved in the CVD processes, including catalyst, temperature, carbon sources, and carrier gas. Moreover, remarkable progress has been achieved to control the orientation [61–63], diameter [64–67] and electronic property [68–70].

Recently, Che *et al* found that by using isopropanol alcohol as the carbon source, wafer scale semiconducting-enriched SWCNT arrays can be grown [71]. The preferential growth of semiconducting SWCNTs with purity up to 97% was verified by multiple laser Raman spectra, and individual and aligned SWCNT array FETs.

Despite the numerous research efforts invested in the design and selection of different catalyst compositions and growth condition as discussed above, chirality-controlled CNT synthesis remained unrealized for an extended time. Inspired by the difficulty of achieving chirality-pure CNT growth from metal catalyst, the concept of using different carbon structures as templates is starting to attract more attention from the research community.

Smalley and co-workers were the pioneers in this field. Their approach was to cut the nanotubes into short segments, and then dock both ends of those segments with Fe-nanoparticles for the so-called amplification growth [72]. Various groups also investigated the use of organic molecules as seeds for nanotube growth [73–77]. However, the drawback of this approach was the lack of control during thermal oxidation step or seed stability at high temperature, which resulted in nanotubes with wide diameter and chirality distribution.

Recently, we developed an approach to achieve chirality-controlled synthesis which utilized both nanotube separation and VPE growth. In particular, we have demonstrated

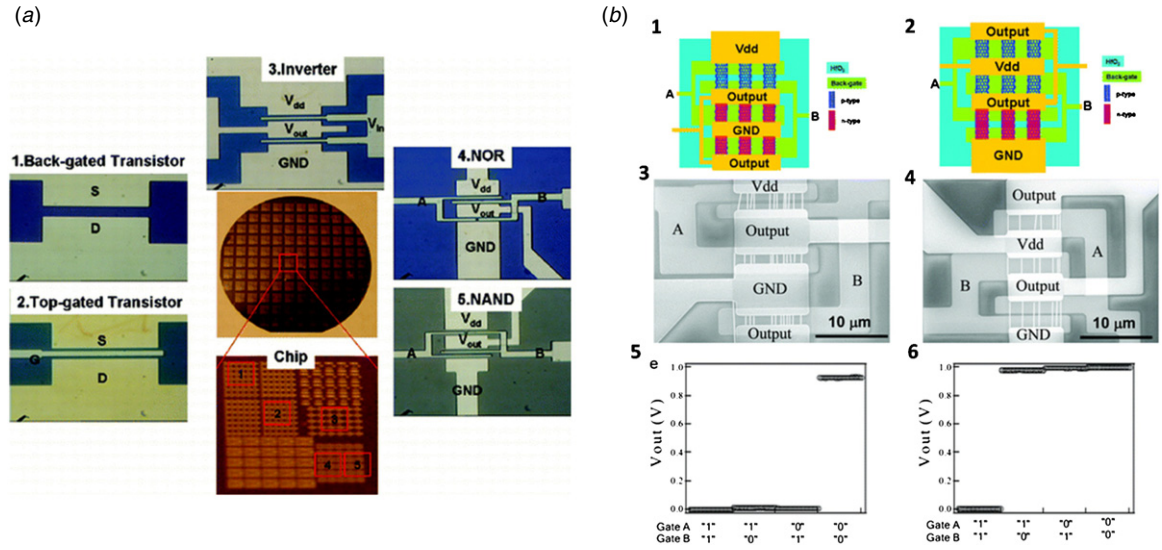

Figure 2. (*a*) Optical images of CNT transistors and circuits built on a 4 inch Si/SiO_2 wafer: 1, back-gated transistor; 2, top-gated transistor; 3, CMOS inverter; 4, NOR logic gate; 5, NAND logic gate. (*b*) Defect-tolerant CMOS NOR and NAND with individual back-gated transistors. (1), (2) Schematic diagrams of CNT-based CMOS NOR and NAND, respectively. (3), (4) SEM images of CNT-based CMOS NOR and NAND, respectively. (5), (6) Output characteristics of CNT-based NOR and NAND. Adapted with permission from [8]. Copyright (2009) American Chemical Society.

successful growth of both semiconducting (6, 5) and (7, 6) SWCNTs, as well as metallic (7, 7) SWCNTs [24]. In our process, single-chirality SWCNT seeds with purity up to 90% or higher were first separated by DNA-based nanotube recognition and separation method [78]. Then, the DNA-wrapped nanotube seeds were dispersed on quartz or SiO_2/Si substrates and underwent a three-step pretreatment process, including annealing in air, annealing in water, and annealing in hydrogen. Finally, methane or ethanol was introduced to initiate nanotube VPE growth at 900 °C. Atomic force microscopy (AFM) revealed a dramatic increase in length from around 300 nm to more than 30 μm after VPE process for (7, 6) nanotubes. Raman spectra using multiple lasers showed that the VPE-grown SWCNTs had the same radial breathing mode positions using the original nanotube seeds for all chiralities we tested. However, further understanding of the mechanism and optimized growth condition is still required to synthesize those structurally uniform CNT with large quantity.

1.2.2. Transistors and digital circuits based on aligned nanotubes. People started studying the possibility of building digital circuits, such as logic gates based on CNT transistors and significant progress has been made in CNT-based integrated circuits. In 2001, groups led by Zhou, Avouris, and Dekker independently reported CNT-based logic gate by integrating p-type nanotube transistors and n-type nanotube transistors, as the first step toward digital circuit application for a complicated computing system. [3–5].

On the basis of massive aligned nanotube arrays synthesized with CVD method on sapphire, our group reported a high-yield and registration-free nanotube-on-insulator approach to fabricate nanotube transistors, similar to the silicon-on-insulator process adopted by the semiconductor industry [79]. Our group demonstrated truly integrated nanotube circuits and wafer-scale fabrication, overcoming the challenges of small sample size, micrometer-scale channel length, and a lack of controlled doping (figure 2). The processing started with the wafer-scale synthesis and transfer of aligned nanotubes arrays up to 4 inches in size. Aligned nanotube array transistors with top-gate were used. Based on the sub-micrometer-scale device platform, controlled electrical-breakdown was used to remove metallic and high-leakage semiconducting nanotubes to improve the on/off ratio. Meanwhile, potassium and electrostatic doping were applied to convert p-type nanotube transistors to n-type. In this way, a truly integrated CMOS logic inverter based on nanotube array transistors was successfully realized. In addition, defect-tolerant circuit design was proposed and employed for NAND and NOR gates, as an essential feature for integrated nanotube circuits.

Shulaker *et al* in Stanford also developed a large-scale integration (VLSI)-compatible metallic CNT removal technique, so-called VLSI-compatible metallic CNT removal (VMR) technology [80]. This technology combines design and processing to create CNT transistors and circuits immune to metallic and mispositioned nanotubes. In this work, combinational and sequential CNTFET logic circuits such as half-adder sum generators and D-latches have been realized as the fundamental building blocks of VLSI digital systems. Moreover, this CNTFET-based digital electronics shows great potential in low-power application due to the large improvement in energy-delay product. They further presented a complete sub-system of a sensor interface circuit, which is entirely implemented using CNTFETs [81]. The CNTFET-based sub-system was demonstrated to interface successfully with a sensor to control a handshaking robot with correct operation.

Recently, the first CNT computer has been demonstrated as an important milestone in the practical application of CNT digital electronics [26]. A scanning electron microscopy

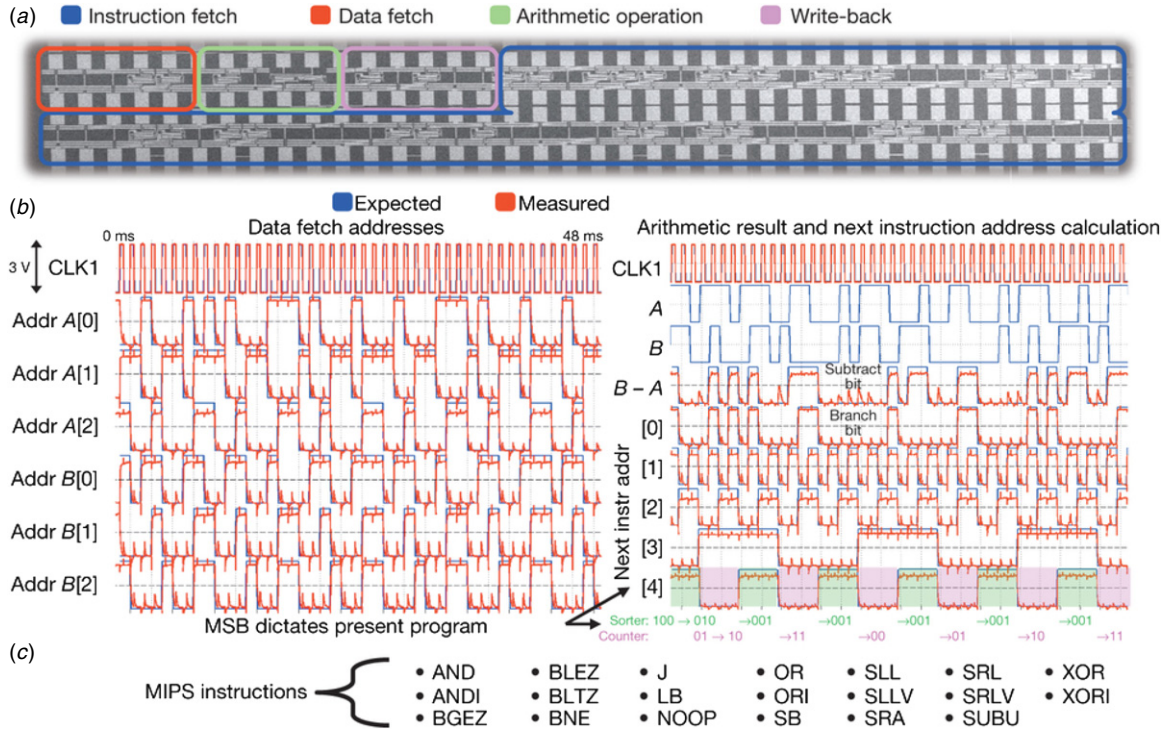

Figure 3. CNT computer (*a*) SEM of the CNT computer. (*b*) As-measured and expected output waveforms for the CNT computer. In this program, the CNT computer is switching between performing counting and sorting. (*c*) A list of MIPS instructions tested on the CNT computer. Adapted with permission from [26]. Copyright (2013) American Association for the Advancement of Science.

(SEM) image of the fabricated CNT computer is presented in figure 3(*a*). It is demonstrated that the CNT computer runs an operating system and achieves multitasking of counting and integer-sorting simultaneously. Even though the operation frequency of this CNTFET-based is only 1 kHz due to the capacitive loading introduced by the measurement setup and academic experimental limitations, the experimental demonstration in this work is a considerable advancement in the development of complex and highly energy-efficient CNT-based electronic system.

With all the achievement discussed above, CNTFET-based digital electronics, as an exciting complement to existing semiconducting technologies, is a good candidate that can outperform silicon.

1.2.3. N-type nanotube transistors. In order to realize CNT-based CMOS integrated circuits, both n-type and p-type CNTFETs are required. Recently, through applying metal contact engineering to the existing nanotube platform, both n-type and p-type CNTFETs have been demonstrated. Based on metals with a work function larger than the valence band edge of CNTs, such as palladium (Pd), people have realized perfect p-type CNTFETs with a barrier-free contact for hole carrier transport [18, 82]. In order to achieve nanotube transistors with n-type behavior, metals with small work function need to be used. This allows the Fermi level of the electrodes to align with the conduction band edge of CNTs, providing an Ohmic contact for electron carrier transport. Chemical and electrostatic doping methods have been applied to achieve n-type CNT transistors by providing excess positive charges in the vicinity of contacts to facilitate electron tunneling [83, 84]. Recently, different kinds of technologies have also been developed to form n-type Ohmic contact in CNTFETs, ideally with no parasitic resistance [27, 28, 85–87].

Ding *et al* applied Y to the contact of CNTFETs and discussed that Y makes a perfect Ohmic contact with the conduction band of the CNT [27]. As illustrated in figure 4(*a*), a self-aligned top-gate device has been fabricated with Y metal contact. This device showed high performance with a room temperature conductance approaching the theoretical quantum conductance limit of CNT-based devices ($4e^2/h$). Figure 4(*d*) presents the transfer characteristics of an as-fabricated top-gate CNTFET with gate length of ~0.8 μm and a gate dielectric HfO_2 with thickness of 15 nm. Based on the analysis, the n-type CNTFET reported in this work shows a subthreshold swing (SS) of 73 mV/decade at room temperature, approaching the theoretical limit (~60 mV/decade) [88].

Meanwhile, our group also introduced the small work function metal gadolinium (Gd) for n-type contact and demonstrated air-stable n-type aligned nanotube transistors [28]. Gd with a work function of ~3.1 eV was used as the metal contact in source and drain electrodes, as shown in figure 4(*b*). The transfer characteristics of the transistor after electrical breakdown are presented in figure 4(*e*) with different drain bias voltages. The linear output characteristics reported in our work also indicate that n-type ohmic contacts can be formed between the Gd electrodes and CNTs.

Recently, Shahrjerdi *et al* performed a thorough experimental study of n-type contacts for CNTFETs based on several kinds of low work function metal contacts, including

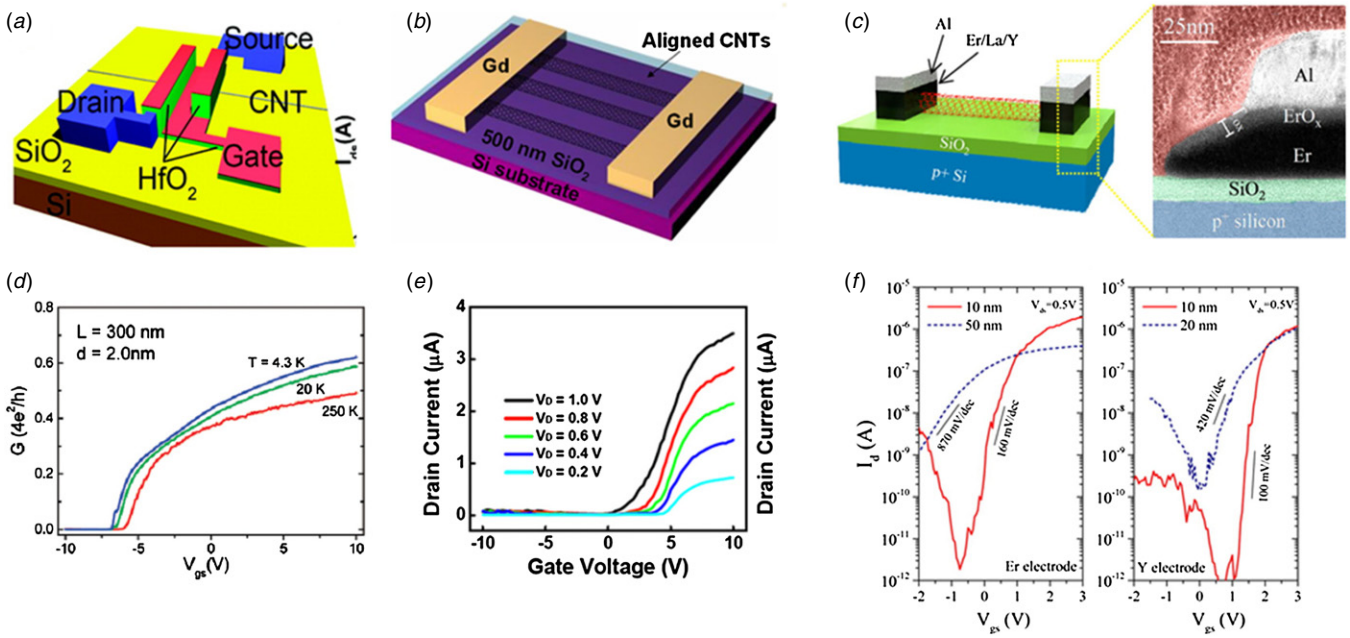

Figure 4. (*a*)–(*c*) Schematic of N-type transistor from reference [27, 28, 85], respectively. (*d*)–(*f*) Representative transfer characteristics of N-type transistor corresponding to transistor structure (*a*)–(*c*). Adapted with permission from [27, 28, 85]. Copyright (2009, 2011, 2013) American Chemical Society.

erbium (Er, $\Phi_M = 3.0$ eV), lanthanum (La, $\Phi_M = 3.5$ eV), and yttrium (Y, $\Phi_M = 3.1$ eV) [85]. Figure 4(*c*) shows a representative transmission electron microscopy (TEM) image of Er contacting CNT transistor, where the Er contact was capped *in situ* with aluminum (Al). The corresponding n-type transfer characteristics of the resulting devices with Er and Y contacts are plotted in figure 4(*f*), showing that the performance of n-type CNTFETs degraded with contact layer thickness increased, due to a higher degree of the metal contact oxidation. It has been discussed that high oxidation rates and sensitivity to deposition conditions of low work function metal contacts results in lower yield and large variation in performance of n-type CNTFETs. To avoid this problem, proper passivation of Er electrodes with a monolayer of hydrophobic polymer was applied to improve device durability in this work.

To further advance CNT-based CMOS integrated circuits, a lot of efforts have been made in improving the scalability and stability of n-type CNTFETs, and those results suggest practical and promising approaches for nanotube-based CMOS integrated circuit applications.

1.2.4. Large-scale assembling of carbon nanotube. In order to become a viable alternative to silicon technology, nanotube-based electronics require scalable assembling of high-density aligned CNT arrays. Dense nanotube arrays are essential to optimize CNT-based electronics through maximizing device packing density and providing sufficient drive current. Previously, our group reported the combined use of low-pressure CVD and stacked multiple transfer to achieve aligned nanotubes with high density up to 55 tubes μm^{-1} [89]. Recently, Cao *et al* presented the Langmuir–Schaefer method to assemble aligned arrays of semiconducting CNT (figure 5) [30]. Starting with pre-processed nanotube solution with a semiconducting purity of 99%, they reported that nanotube arrays assembled using this method can fully cover a surface with a density of more than 500 tubes μm^{-1}. Due to the high density, semiconducting purity, and quality of alignment, the CNTFETs fabricated using this approach present improved electrical properties with a drive current density of more than 120 mA mm^{-1}, transconductance greater than 40 mS mm^{-1}, and on/off ratios of $\sim 10^3$.

These CNT-assembling results show the great potential for using CNT arrays in scalable high-performance beyond-silicon electronics through CMOS-compatible circuit- and system-level implementation. Meanwhile, the scale assembling of CNT also motivates other emerging applications, including thin-film electronics, transparent electronics, and stretchable electronics.

1.3. Radio frequency electronics

The unique characteristics of SWCNT such as high mobility, small dimension, low capacitance, and large transconductance generate great interest in CNT-based analogue electronics, which is of great importance. Analogue electronics only requires high transconductance but not high on/off ratio for RF transistors [9–16]. Recently, RF transistors and circuits that incorporated densely aligned arrays of SWCNTs enabled comprehensive experimental and theoretical evaluation of their intrinsic properties, toward practical application of SWCNTs.

1.3.1. Carbon nanotube RF transistor. The typical layouts used in CNT RF transistor are presented in figure 6(*a*) consisted of a double channel configuration in which two gate electrodes and two source electrodes surround a common drain

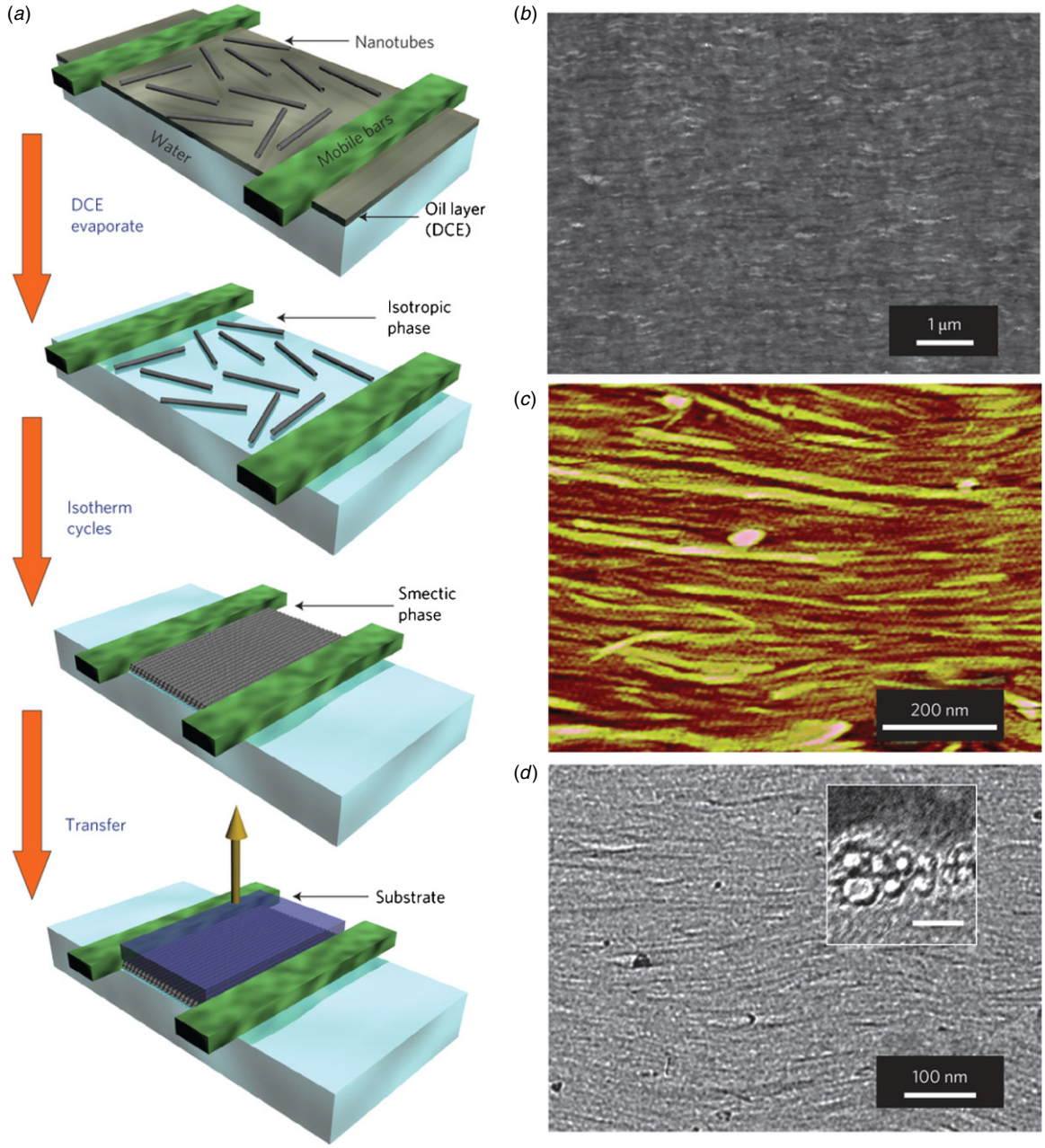

Figure 5. Langmuir–Schaefer assembly of full-coverage aligned semiconducting CNT arrays. (*a*) Schematic of the Langmuir–Schaefer assembly process flow. (*b*)–(*d*) SEM (*b*), AFM (*c*), TEM (*d*) images of aligned nanotube arrays on substrates. Adapted with permission from [30]. Copyright (2013) Nature publishing Group.

electrode [12, 90]. This layout design is fully compatible with conventional small signal models of RF response. Previously, device structure in figure 6(*b*) was commonly used, where horizontally aligned arrays of SWCNTs occupy the channel region of RF transistor and provide an electrically continuous and independent pathway for charge transport. On the basis of this device design, Kocabas *et al* reported submicrometer channel length RF transistors that involve perfectly aligned nanotube array with densities of 2 or 5 SWCNTs μm^{-1} [90]. The transistors reported in this work show unity current gain (f_t) and unity power gain frequencies (f_{max}) as high as ~5 and ~9 GHz, respectively. The small signal models of the devices provide the essential intrinsic parameters: intrinsic f_t of ~30 GHz for a gate length of 700 nm. The results provide clear insights into the challenges and opportunities of CNT arrays for applications in RF electronics.

Recently, a self-aligned T-shaped gate fabrication approach developed by our group has been introduced for high-performance SWCNT RF transistors, representing an important step toward RF applications (figure 7(*a*)) [15, 31]. With this self-aligned design, the parasitic effects of fringe gate capacitance, access resistance, and gate charging resistance can be significantly reduced. Furthermore, the channel length can be scaled down to 100 nm and the Al_2O_3 gate dielectric was reduced to 2–3 nm, contributing to the quasi-ballistic and quasi-quantum capacitance operation for nanotube transistors

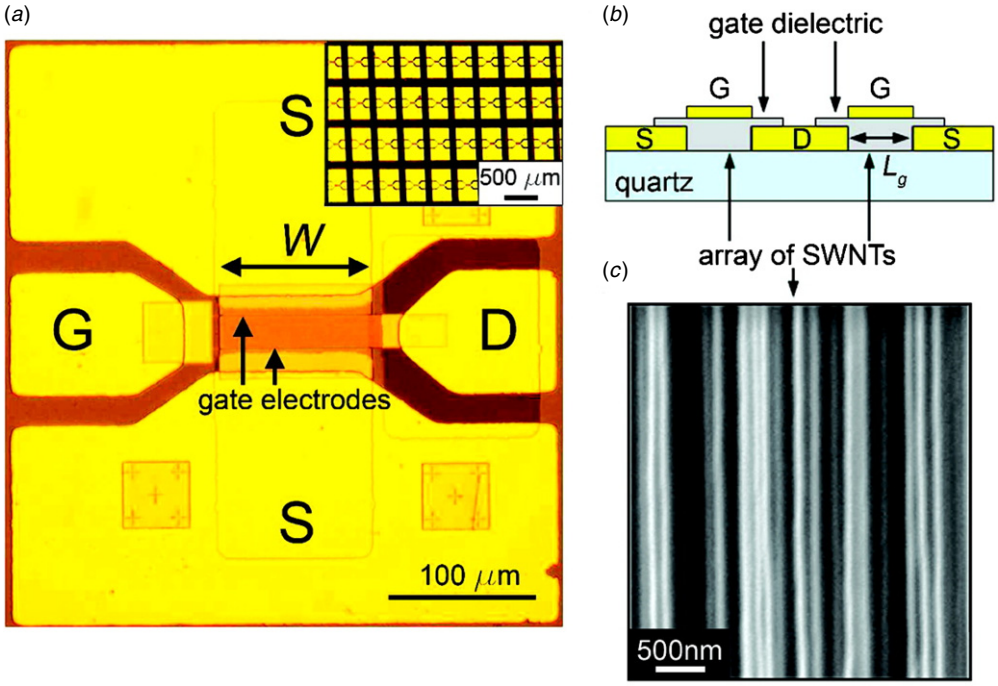

Figure 6. (*a*) Optical images of nanotube array RF transistors on a quartz substrate. (*b*) Schematic of aligned nanotube RF transistor. (*c*) SEM of aligned nanotube arrays. Adapted with permission from [11]. Copyright (2009) American Chemical Society.

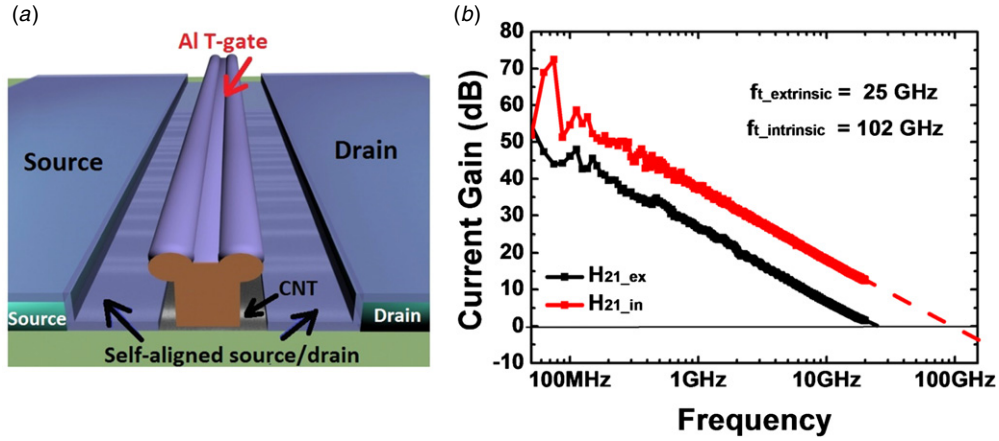

Figure 7. (*a*) Schematic of self-aligned T-gate aligned nanotube RF transistor. (*b*) Extrinsic and intrinsic frequency response of self-aligned T-gate aligned nanotube RF transistors. Adapted with permission from [31]. Copyright (2013) American Chemical Society.

[15]. An extrinsic f_t up to 25 GHz before any de-embedding procedure was achieved for RF transistors consisted of aligned nanotube arrays synthesized by CVD method (density ~5 tubes μm^{-1}), as the highest extrinsic cut-off frequency reported to date for nanotube RF transistors (figure 7(*b*)) [31].

Meanwhile, Steiner *et al* reported a planar device platform with embedded electrodes combined with dense aligned high-purity semiconducting CNT assembled through dielectrophoresis (figures 8(*a*), (*b*)) [16]. In this work, as-measured, extrinsic f_t and f_{max}, respectively, of 7 and 15 GHz were obtained for a RF transistor of 100 nm channel length (figure 8(*c*)). After de-embedding, intrinsic f_t and f_{max} of 153 and 30 GHz were observed (figure 8(*d*)).

These high-performance nanotube RF transistors pave the path toward practical RF circuits operated in gigahertz regime.

1.3.2. Linearity of carbon nanotube RF transistor. Linearity is a significant figure of merit for analogue and RF/microwave circuit and system designs. CNT-based transistors with inherent linearity are anticipated to enable emerging designs and systems requiring highly linear transistors [91].

The linearity performance of the carbon-based transistors was firstly estimated indirectly, through use of the transistor in a mixer by our group [14]. In 2012, our group further presented a 1 dB compression point measurement of nanotube RF transistors directly with positive power gain.[15] In this measurement, CNT RF transistors were used in constructing

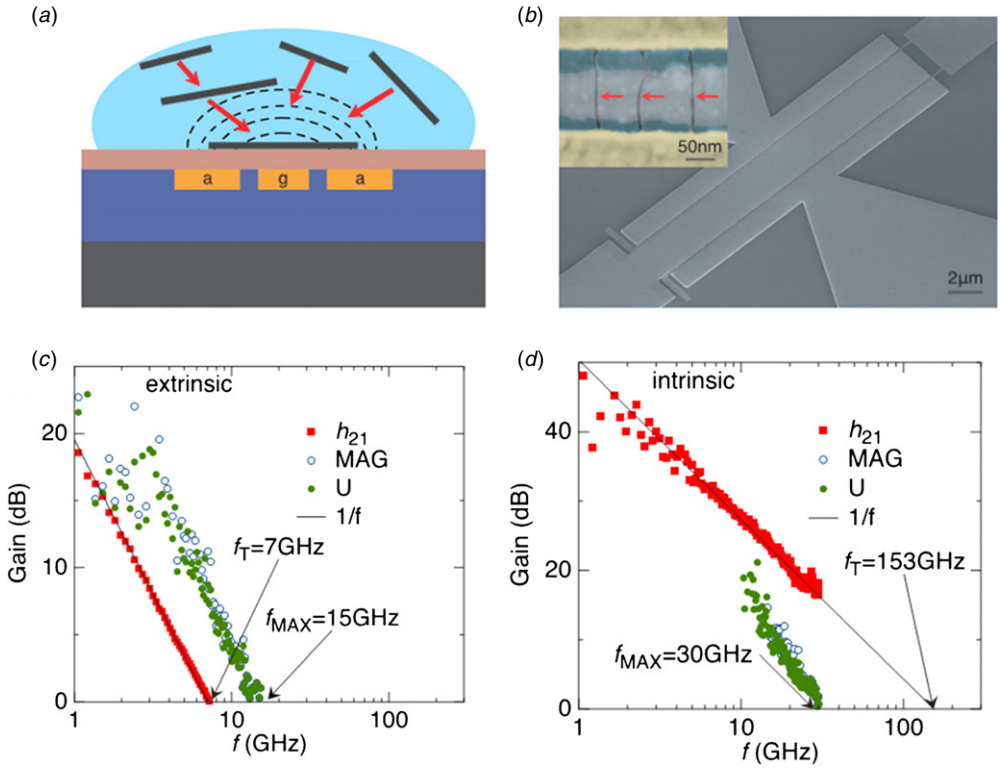

Figure 8. (*a*) Schematic of a planar CNT RF transistor with embedded gate structure. (*b*) SEM image of the CNT RF transistor. (*c*) The extrinsic current gain and extrinsic maximum available power gain. (*d*) The intrinsic current gain and intrinsic maximum available power gain. Adapted with permission from [16]. Copyright (2013) American Institute of Physics.

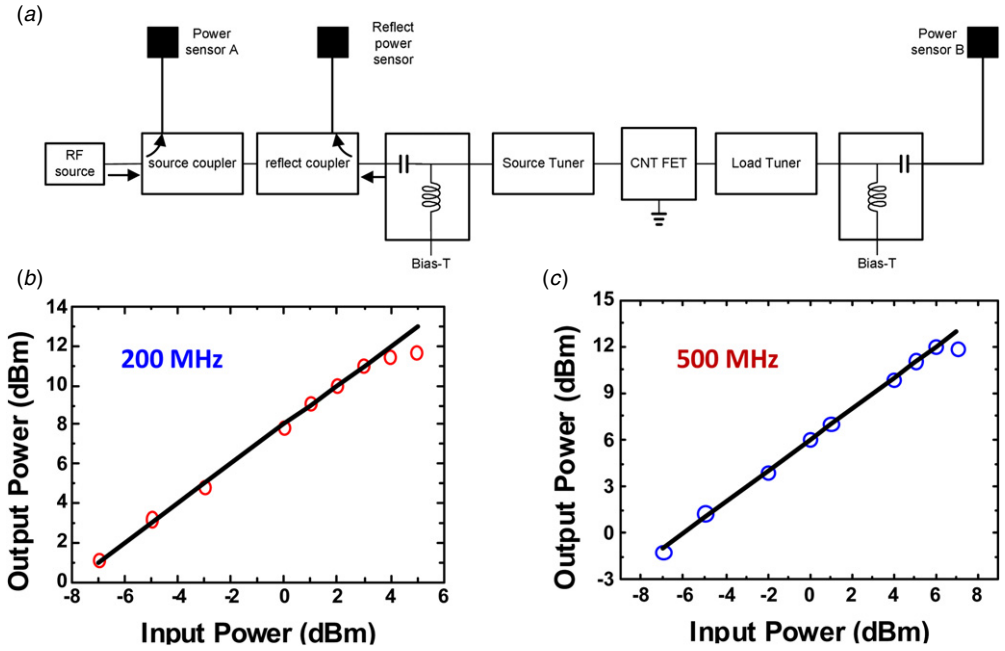

Figure 9. Linearity characteristics of T-gate self-aligned separated nanotube RF transistors. (*a*) Schematic of load and source pull setup system to capture the nonlinearity for the nanotube RF transistor. (*b*), (*c*) 1 dB compression point plots measured at 200 MHz (*b*) and 500 MHz (*c*). Adapted with permission from [31]. Copyright (2012) American Chemical Society.

a class-A power amplifier (figure 9(*a*)), and the device was characterized in a large signal domain. Two 1 dB compression point plots, at 200 and 500 MHz input frequency are illustrated in figure 9(*b*) and (*c*), respectively. The 200 MHz input frequency measurement reveals a 1 dB output referred compression point of 11.6 dBm, while 500 MHz input frequency measurement indicates a 1 dB output referred compression point of 11.9 dBm.

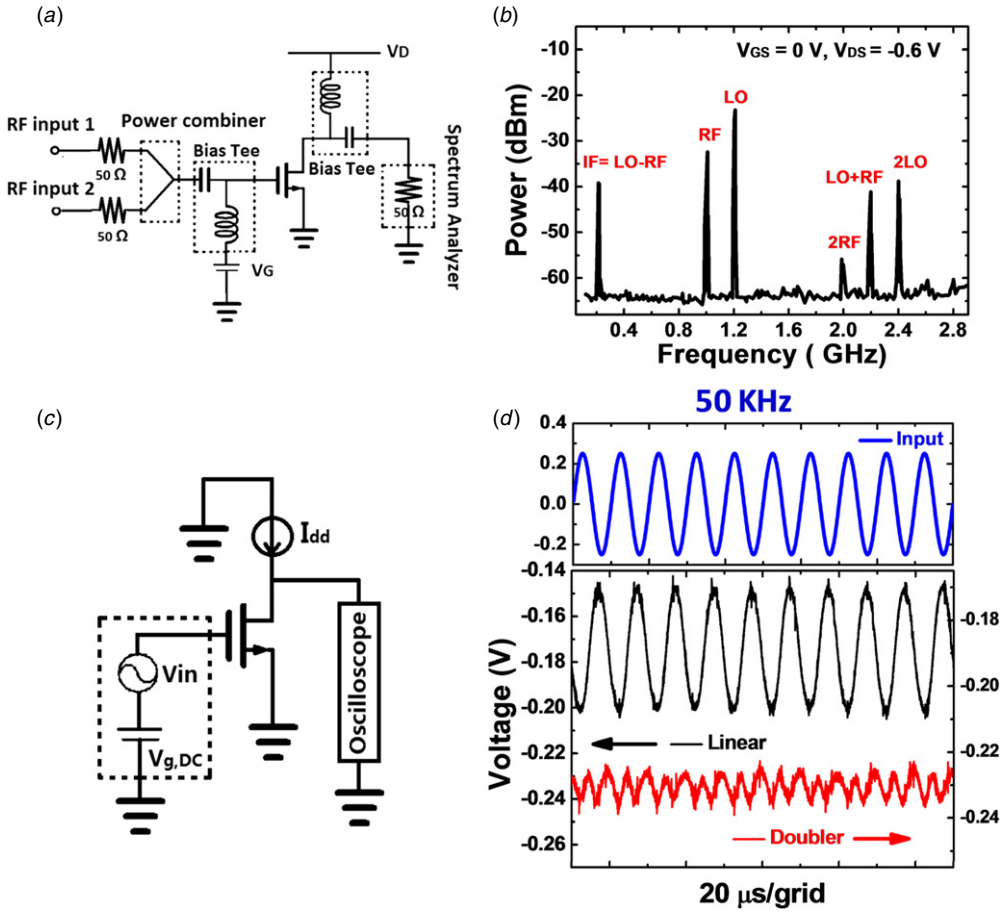

Figure 10. (*a*), (*b*) Circuit diagram and output spectrum of CNT-based mixer. (*c*), (*d*) Circuit diagram and output waveform of CNT-based frequency doubler. Adapted with permission from [31]. Copyright (2013) American Chemical Society.

1.3.3. Nanotube-based RF circuits. For the past few years, many groups have gone beyond device characterization and demonstrated practical applications of CNT in actual radio circuits and systems.

Rutherglen *et al* in UC Irvine and Jensen *et al* in UC Berkeley have demonstrated a nanotube demodulator in a radio receiver, as part of a functioning radio that can receive a signal and play music broadcasted wirelessly [92, 93]. Meanwhile, collaboration between the group led by Rogers at the University of Illinois at Urbana-Champaign and Northrop Grumman also demonstrated a RF amplifier based on a CNTFET that was applied in an entire AM radio system [12]. These demonstrations of CNT-based RF systems present an important milestone to enable the realization of operating systems.

Armed with the excellent on-chip performance of CNT RF transistors, our group also carried out an extensive analogue circuit study including mixing and frequency doubling circuits operated in gigahertz regime [31]. Aligned nanotube transistor-based mixer is configured by mixing the LO and RF signals at the gate (figure 10(*a*)). Figure 10(*b*) shows the output spectrum of mixer with the transistor with testing frequency ranged in 1–2 GHz. Other than amplifiers and mixers, aligned CNT transistors can find applications in frequency doubling circuit based on the ambipolar transport property. A frequency doubler consisting of CNT RF transistor is achieved with a circuit diagram as shown in figure 10(*c*). The as-measured output waveform (figure 10(*d*)) presents a good frequency doubling function.

2. Carbon nanotube macroelectronics

2.1. Gaseous phase carbon nanotube network electronics

Many research groups including our own have demonstrated high performance FETs comprised of CNT random network based on CVD synthesized CNT [23, 33, 36, 94]. During the synthesis of the CNTs, growth substrates, such as quartz or Si/SiO_2 wafers decorated with catalysts (Fe particles or ferritin) were placed in a furnace at elevated temperatures ($>800\,^{\circ}C$). Then a precursor containing carbon feedstock, such as methane or isopropyl alcohol was introduced into the growth chamber for the dissociation of hydrocarbon molecule from the feedstock. The hydrocarbon molecules then facilitated the growth of the CNT on the catalysts [23, 33]. Ohno's group introduced a floating-catalyst CVD technique with monoxide (CO) as the carbon source. The as-grown nanotubes were collected through a simple gas-phase filtration process [32, 36, 95]. The CNTs were transferred onto the device substrate by dissolving the filter in acetone. The advantage of utilizing as-grown CNTs directly for fabrication of devices is that there are more Y-type junctions between the nanotubes

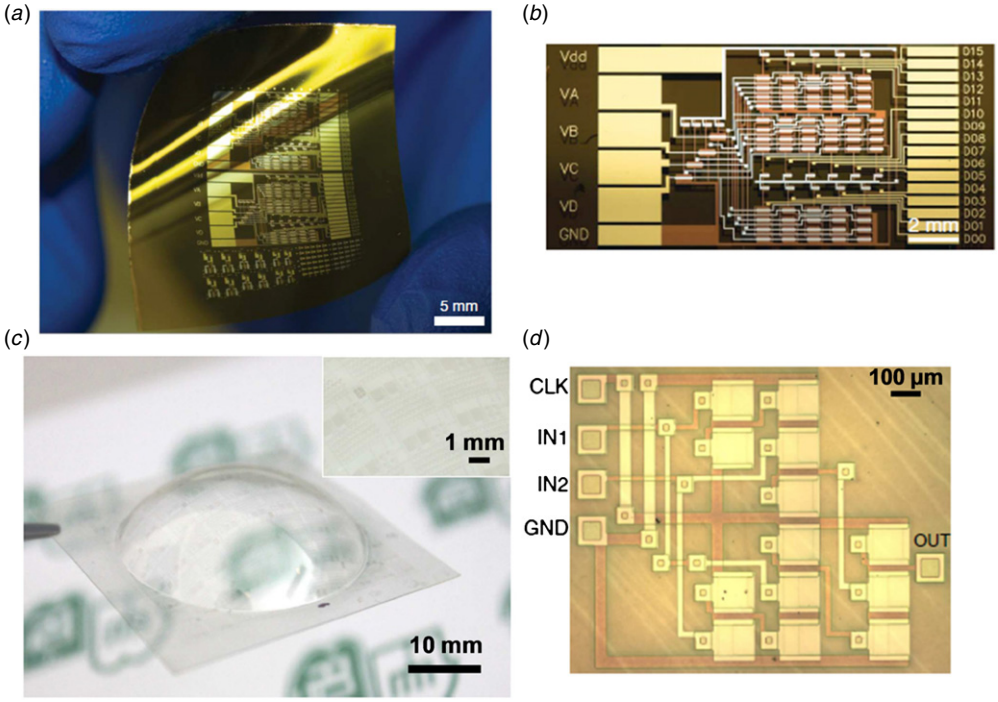

Figure 11. (*a*) Photographic image of CNT network-based decoder on polymeric substrate. (*b*) High magnification photographic image of the decoder consisting of 88 CNT transistors. Adapted with permission from [24]. Copyright (2008) Nature Publishing Group. (*c*) Dome-shaped CNT-based transistors. (*d*) CNT-based XOR gate on flexible substrate. Adapted with permission from [36]. Copyright (2013) Nature Publishing Group.

than the X-junctions, which can result in a higher mobility of the transistors [32]. The transfer process of the CVD grown CNTs is carried out at room temperature, which is desirable for the fabrication of flexible electronics.

Figure 11(*a*), illustrates an integrated circuit chip fabricated on a polyimide flexible substrate based on CVD grown CNT random network-transistors [33]. The largest circuit on the chip is a four-bit decoder consisting of 88 transistors. The decoder operated correctly at 1 kHz. The CNT random network in this work was synthesized by CVD, and the CNT network in conjunction with predefined drain/source electrodes were transfer printed onto the flexible polyimide substrate [33, 96]. Figure 11(*b*), shows an optical micrograph of the four-bit row decoder. The CNT FETs used in the integrated circuits (ICs) exhibited desirable performance with a typical mobility of ~70 $cm^2\ V^{-1}\ s^{-1}$ with typical current on/off ($I_{on/off}$) ratio of 10^3. The four-bit row decoder generates a correct signal for all 16 of its output lines corresponding to the specific combination of the four input signals. This demonstrates the reliability of using CNT random network for this medium-scale integrated circuit. Inverters fabricated based on the CNT network exhibited minimal variation during bending test on the flexible circuits. This underscores the advantage of flexibility of CNT random network-based FETs.

Figure 11(*c*), further demonstrates the applicability of expending CVD-based CNT random network transistors in flexible electronics [36]. In the study, floating catalyst CVD was employed to synthesize the CNTs, and the as-grown CNTs were transferred onto polyethylene naphthalate for flexible and mouldable integrated circuits. The CNTs were used to fabricate inverters; 11- and 21-stage ring oscillators; NOR, NAND and XOR gates; and static random access memory cells [36]. The CNT-based transistors exhibited mobility as high as 1027 $cm^2\ V^{-1}\ s^{-1}$, not only exceeding the performance of earlier reported results of CNT network-based transistors, but also that of Si-based metal-oxide-field-effect-transistors [32, 97, 98].

2.2. Solution-based carbon nanotube random network electronics

In addition to the study of CVD-based CNT random network electronics, there has also been extensive research in the area of solution-based CNT electronics [34, 35, 40, 43, 99–101]. The as-grown CNT contain approximately 1/3 metallic tubes and 2/3 semiconducting nanotubes [102]. This presents a negative effect in CNT-based transistors because the metallic nanotubes in the CNT film may contribute to direct conducting paths between the drain and source electrodes in a FET, and this can result in low $I_{on/off}$ for the transistors [103–106]. Due to the advancement in enrichment of semiconducting CNT, CNT solution with higher percentage of semiconducting tubes can be sorted with techniques such as density-gradient ultracentrifugation [102, 105, 106].

Many methods of separating metallic/semiconducting or even single chirality of nanotubes have been achieved. Particularly, DNA-wrapped nanotubes can be separated into nearly single-chirality nanotubes by ionic exchange chromatography [78]. Density-gradient ultracentrifugation can realize the separation of nanotubes dispersed by widely-used cheap surfactants [107]. Furthermore, the simple and scalable gel chromatography can also be applied to achieve

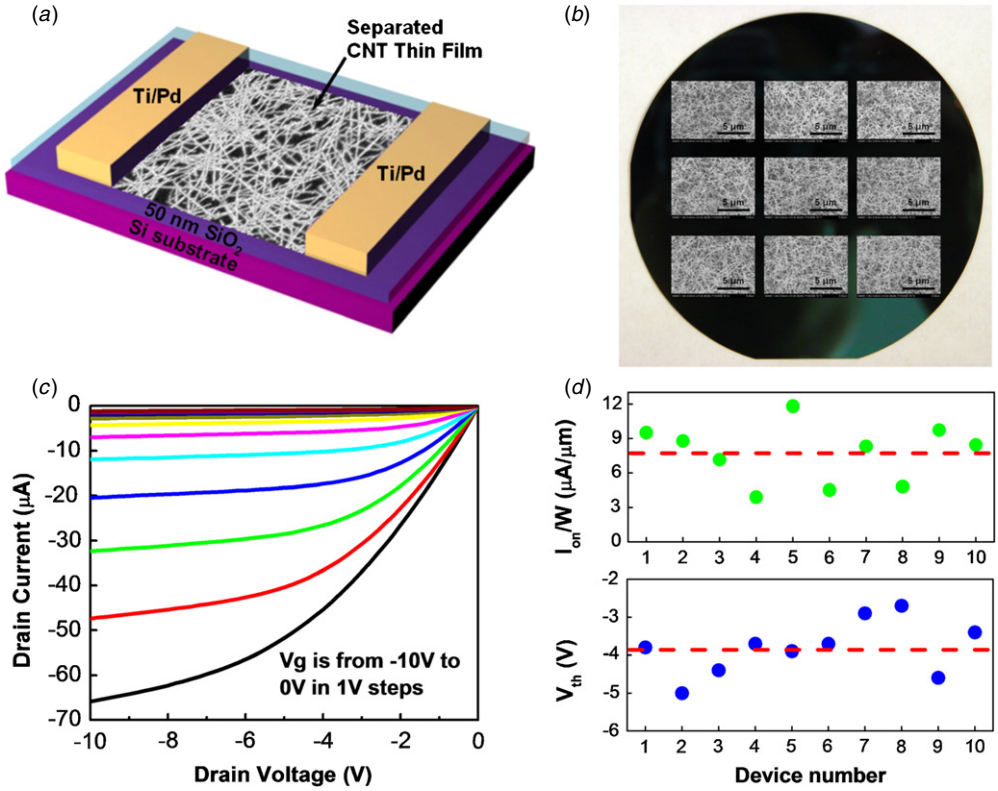

Figure 12. (*a*) Schematic diagram of a back-gated transistor based on separated semiconducting enriched CNT random network. (*b*) SEM images of CNT random network captured at different region of a wafer after CNT deposition. (*c*) Output characteristic of a CNT network-based transistor. (*d*) Statistical study of current density (I_{on}/W) and threshold voltage (*V*th) measured ten CNT-based devices. Adapted with permission from [34]. Copyright (2009) American Chemical Society

the separation of the surfactant-dispersed nanotubes without ultracentrifugation [108]. Selectively dissolving nanotubes by designed polymers has also achieved great success, but the polymers are not readily available [109]. Recently, the aqueous two phase separation, which could tune the hydrophobicity and hydrophilicity of the two phases and cause the partitioning of the tubes, is a promising, scalable, and fast separation method [110].

Many research groups including our own have demonstrated high performance CNT TFTs based on the sorted semiconducting CNT solution [25, 34, 43, 99, 111, 112]. The CNT TFTs have been employed in the applications of drivers for AMOLEDs, pressure sensors and integrated digital circuits [35, 40, 100]. CNT random network thin film exhibits excellent transparency, which makes it a desirable channel material for the driver circuitry in transparent display applications [35, 43]. In comparison with amorphous silicon FETs and organic transistors, CNT TFTs have been demonstrated to exhibit superior performance in terms of mobility [113, 114]. CNT TFTs with mobility greater than 100 $cm^2\ V^{-1}\ s^{-1}$ have been reported [97, 115, 116], which exceed the mobility of amorphous and organic FETs by at least two orders of magnitude. And comparing CNT TFT with polycrystalline silicon FETs, they can be processed at room temperature, which is essential for the fabrication of flexible electronics on polymeric substrates [43, 113]. In addition to the aforementioned merits of CNT TFTs, CNT solution can be printed with various techniques such as inkjet printing, screen printing or gravure printing etc [37–39, 44, 117]. Printing for electronics is an inexpensive and scalable technique that can be expended to fabricate circuits in a large area of flexible substrates at low cost. This advantage is unparalleled to the existing silicon process.

We are among the first few research groups to demonstrate CNT TFTs comprised of semiconducting enriched CNT random network [34, 111, 112]. Figure 12(*a*) illustrates a common back-gated TFT based on a random network of separated CNT solution [34]. In the study, CNT solution consisted of 95% and 98% enriched semiconducting tubes were used in the channel of the FETs. The CNT solution was uniformly deposited onto the device substrate by first functionalizing with aminopropyltriethoxy to terminate the surface of the substrate with a layer of amino-groups, which enhances the attraction between the CNTs and the surface [118]. As can be observed in figure 12(*b*), the CNT thin film can be deposited invariantly over the entire surface of a 3 inch Si/SiO_2 wafer, as shown by the SEM images captured at different regions of the wafer after CNT deposition. This proves that the deposition process is scalable, and can be used in industrial-scaled fabrication. The geometry of the channel in the transistors can be defined by standard photolithography, followed by O_2 plasma etching of the CNT film in the region outside the channel. This technique eliminates the issue of assembly of the nanotubes. The transistors fabricated with the 98% enriched CNT solution exhibited ideal p-type behavior with mobility as high as 52 $cm^2\ V^{-1}\ s^{-1}$, while maintaining

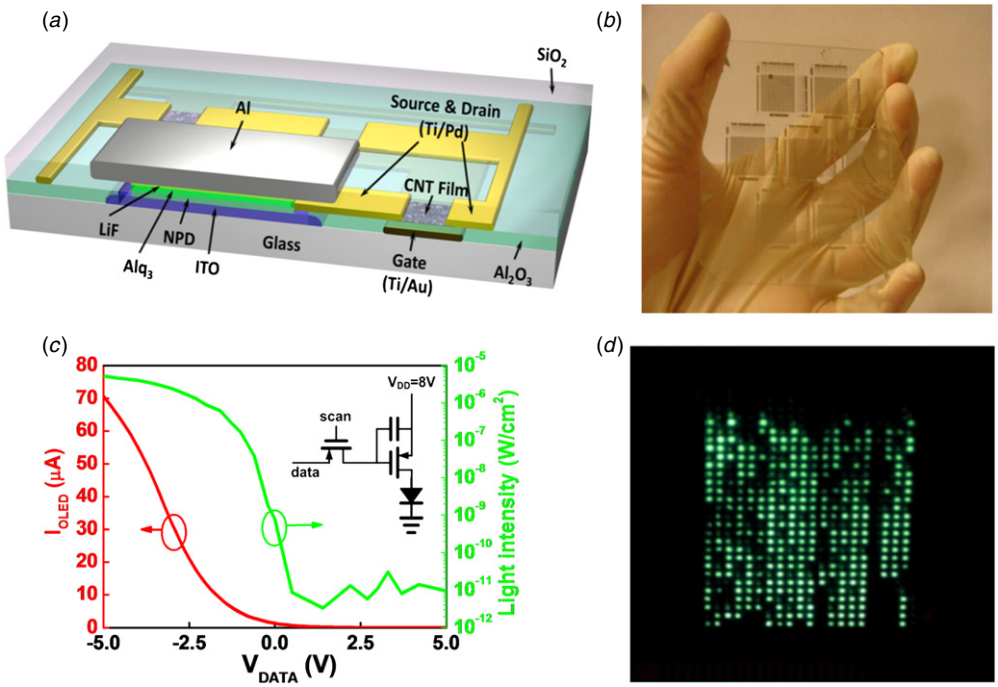

Figure 13. (*a*) Schematic diagram of one pixel of OLED controlled by CNT network-based driver circuitry. (*b*) Arrays of AMOLEDs controlled CNT circuits fabricated on a transparent glass substrate. (*c*) Current (IOLED) and light intensity behavior of a pixel of the CNT controlled OLED unit. (*d*) Arrays AMOLED illuminating green light after being turned on by CNT network-based driver circuit. Adapted with permission from [35]. Copyright (2011) American Chemical Society.

a current on/off ratio of 10^4. Although the mobility of the devices is not as high as that exhibited by silicon transistors, it is still an invaluable thin film material for applications such as drivers for display, or flexible electronics [98]. The output characteristic of the CNT TFTs is exhibited in figure 12(*c*). As can be observed in the plot, the output curves can be fully saturated. The uniformity of the devices is illustrated in figure 12(*d*). The normalized on current (I_{on}/W) and threshold voltage (*V*th) of 10 CNT TFTs were delineated in the figure. The results provided evidence for the applicability to implement the separated CNT thin films in large-scale fabrication processes.

In order to provide evidence for the practicality of employing CNT TFTs in actual applications, our research group has conducted a series of researches in CNT TFTs for displays and digital circuits [25, 35, 43, 99]. Due to the excellent transparency of CNT thin films, they were used as the channel material for the FETs in the drivers of arrays of AMOLEDs fabricated on glass substrate, which is an essential demonstration for the practicality of adopting the CNT TFTs in transparent display applications. As can be observed in figure 13(*a*), the device structure of one unit of the transparent AMOLED array was illustrated conceptually in the schematic diagram. This is the first demonstration of monolithically integrated AMOLED arrays with 500 pixels driven by 1000 CNT TFTs [35]. Figure 13(*b*) shows that all of the display elements in conjunction with the CNT TFT-based driver circuitry were fabricated on a glass substrate. The CNT TFTs in the drivers exhibited desirable electrical properties with mobility of around 30 $cm^2\ V^{-1}\ s^{-1}$ and $I_{on/off}$ of $\sim 10^4$. The mobility and $I_{on/off}$ were extracted based on the transfer characteristic presented in figure 13(*c*). Figure 13(*d*) illustrates a photographic image of 500 AMOLEDs pixels that were turned on by the CNT TFTs in the drivers, and the yield of the pixels was 70%. Most of the failure in the AMOLEDs was caused by the failure of the OLEDs themselves, not the CNT TFTs. The results clearly demonstrate the uniformity and reliability of the CNT TFTs.

One of the aforementioned advantages of CNT thin films is their flexibility, and that makes them an invaluable candidate in flexible electronics. Our group has previously demonstrated extremely flexible circuits based on CNT thin films exhibiting desirable electrical performance [100]. CNT thin films have also been employed in control circuits for pressure sensing elements in electronic skin [101]. Figure 14(*a*) illustrates the schematic diagram of an element in user-interactive electronic skin arrays [40]. The user-interactive electronic skin is a combination of CNT TFT-based control circuits, AMOLEDs and pressure sensing elements. When pressure is applied to a certain region on a continuous piece of pressure sensitive rubber (PSR), arrays of CNT TFTs located under the region will turn on the OLEDs connected to the corresponding CNT TFTs under the same region. With this design mechanism, an area on the electronic skin is lit up whenever pressure is exerted to that area, and this mechanism is illustrated in figure 14(*b*). This is further demonstrated in figure 14(*c*) with pixels of different colors of OLEDs connected to the CNT-based control circuits and the PSR. In the figure, it shows that polydimethylsiloxane (PDMS) slabs of different letters were placed onto the electronic skin, and a high proportion of the OLED pixels underneath the PDMS slabs were lit when pressure was applied to the configuration.

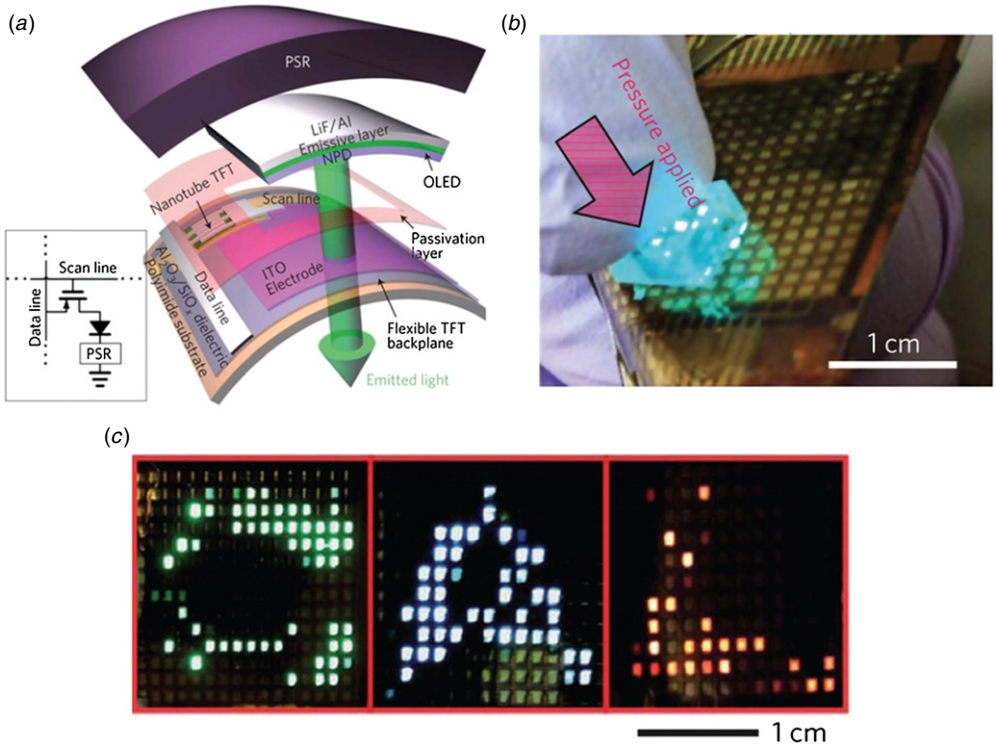

Figure 14. (*a*) Schematic diagram of a pixel of PSR-based sensor integrated with an OLED in conjunction with a CNT thin film-based driver. (*b*) Demonstration of lighting arrays of OLEDs under the region where pressure is applied on the e-skin. (*c*) Illustration of letter C, A and L illuminated by the e-skin as pressure is applied to PDMS stamps formed in the letter shapes. Adapted with permission from [40]. Copyright (2013) Nature Publishing Group.

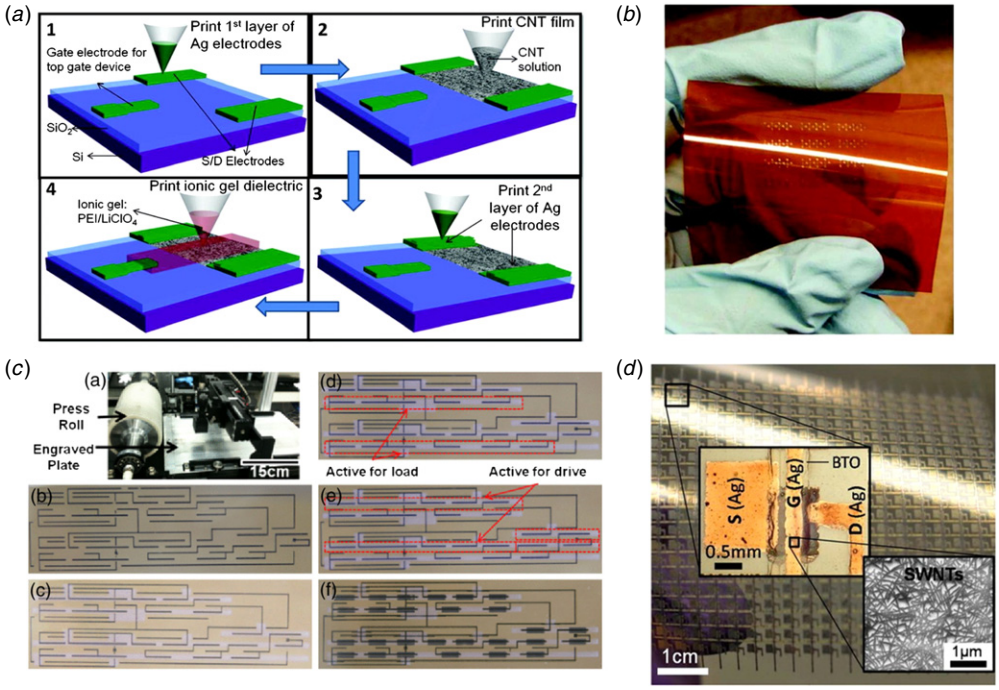

Figure 15. (*a*) Schematic diagram fully printed CNT random network-based devices; panel 1, printing of Ag nanoparticle-based electrodes; panel 2, printing of CNT solution; panel 3, printing of second layer of Ag nanoparticle electrodes; panel 4, printing of ionic gel dielectric material. Adapted with permission from [32]. Copyright (2011) American Chemical Society. (*b*) Fully printed CNT transistors on a Kapton substrate. (*c*) Gravure roll-to-plate printing of CNT-based full adder. (*d*) Gravure printed CNT-based transistors on a PET substrate. Inset (middle): optical micrograph of a gravure printed transistor. Inset (bottom right): SEM image of printed CNT random network thin film. Adapted with permission from [44]. Copyright (2011) American Chemical Society.

2.3. Printed carbon nanotube random network electronics

One of the substantial merits of solution-based CNT random network for flexible electronics is its printability [37–39, 41, 44]. Printing is a low-cost and highly scalable technique for fabrication of flexible electronics in low temperature. Our group has demonstrated fully printed CNT-based transistors using inkjet printing [41], which is shown in figures 15(*a*) and (*b*). Figure 15(*a*) illustrates that the metal electrodes, dielectric materials and CNT channels can be all printed with inkjet printer. The process is fully compatible on both rigid and flexible substrates, as can be observed in figure 15(*b*) of the fully printed CNT transistors on Kapton. In addition to the inkjet printing technique, printed CNT-based flexible electronics have also been realized with gravure printing [38, 39, 44]. Figure 15(*c*) shows a gravure roll-to-plate printed full-adder circuit on polyethyleneterephthalate (PET) foils with CNT random network as the channel materials in the transistors [39]. All of the materials employed in the circuit were printed, and the process is highly scalable due to the nature of gravure roll-to-plate printing. Figure 15(*d*) illustrates gravure printed CNT-based transistors with an alternative method for dispersion of CNT solution during the fabrication process [44]. In Figure 15(*d*), CNT network was deposited onto the PET substrate by first functionalizing of the surface of the substrate, and then followed by immersion of the substrate in a solution of 99% enriched semiconducting CNT solution. The process resulted in high performance printed CNT transistors. The inset at the center of figure 15(*d*) illustrates a printed CNT-based device, and the SEM image at the bottom right corner of the figure shows the morphology of the CNT random network thin film in the channel of the device.

Summary and outlook

As a summary, CNTs are promising candidates in next-generation nanoscale electronic applications. The unique geometric structure and electronic properties of CNT contribute to their great potential in high-performance and energy-efficient digital and analogue electronics. Meanwhile, large-scale aligned nanotube arrays provide a platform for practical integrated circuit applications. In spite of the major milestones achieved, further improvement is still required to advance nanotube-based electronics. Preparation of scalable, dense, and high-purity semiconducting nanotube arrays is of great importance in integrated circuit configuration. To take advantage of the superior intrinsic properties of CNT, transistor characteristics such as contact resistance and gate control are expected to be further optimized. With further development, CNT nanoelectronics are anticipated to be promising in beyond-silicon electronics.

In the macroelectronics field, transistors based on CNT random network exhibit high mobility, high transparency, and high flexibility. These are desirable factors in flexible electronics. The CNT thin film-based FETs are processed at room temperature which is critical for the fabrication of circuits on flexible polymeric substrates. The solution-based CNT random network is an unparalleled building block for circuits fabricated with various printing techniques. The process is highly scalable and can be readily adopted in the existing printed electronics industry.

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