Review of Packaging Schemes for Power Module

Hou, Fengze; Wang, Wenbo; Cao, Liqiang; Li, Jun; Su, Meiying; Lin, Tingyu; Zhang, Guoqi; Ferreira, Braham

DOI
10.1109/JESTPE.2019.2947645

Publication date
2020

Document Version
Accepted author manuscript

Published in
IEEE Journal of Emerging and Selected Topics in Power Electronics

Review of Packaging Schemes for Power Module

Fengze Hou, Wenbo Wang, Liqiang Cao, Jun Li, Meiying Su, Tingyu Lin, Guoqi Zhang, *Fellow, IEEE*, and Braham Ferreira, *Fellow, IEEE*

***Abstract*— SiC devices are promising for outperforming Si counterparts in high-frequency applications due to its superior material properties. Conventional wirebonded packaging scheme has been one of the most preferred package structures for power modules. However, the technique limits the performance of a SiC power module due to parasitic inductance and heat dissipation issues that are inherent with aluminum wires. In this article, low parasitic inductance and high-efficient cooling interconnection techniques for Si power modules, which are the foundation of packaging methods of SiC ones, are reviewed first. Then, attempts on developing packaging techniques for SiC power modules are thoroughly overviewed. Finally, scientific challenges in the packaging of SiC power module are summarized.**

***Index Terms*— High-efficient cooling, low parasitic inductance, packaging schemes, scientific challenges, SiC power module.**

I. Introduction

SILICON carbide (SiC) is a promising semiconductor material in high operating temperature, high blocking voltage, and high switching frequency applications due to its excellent electrical and thermal properties [1]–[4]. Compared with Si counterparts, SiC devices are cable of switching at higher speed and thus enable increased operation frequency of SiC power modules [5]. However, these features pose substantial challenges to packaging of a SiC power module.

Aluminum (Al) wirebonded packaging scheme has been the most preferred package structure for power module up to now. Fig. 1 shows a power module with a conventional packaging scheme. The bottom side of a power semiconductor device is attached to a ceramic substrate [direct-bonded copper (DBC)], usually using solder, while the top side is connected using wirebonds. DBC is basically a ceramic tile with two layers of copper (Cu), with one of them patterned to form an electrical circuit [6]. The conventional package provides electrical interconnects (via Al wirebonds and upper Cu tracks of DBC ceramic substrate), electrical insulation (using the DBC ceramic substrate), device protection (by encapsulation material), and thermal management (through bottom side). This typical package structure is used in the vast majority of the power modules that are currently manufactured [7].

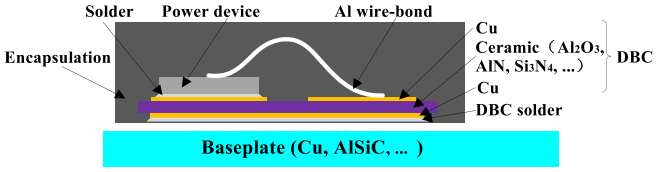

Fig. 1. Conventional packaging scheme for a power module.

The conventional wirebonded interconnection solution, however, limits the performance of a SiC power module. Wirebonds have inherent parasitic inductance that could exceed 10 nH. High *di/dt* at turn-off transient would easily lead to voltage overshoot, increasing switching loss of power devices, causing electromagnetic interferences (EMIs), limiting switching frequency, and affecting switching waveforms [7]–[9]. From a heat dissipation point of view, heat generated by power devices is dissipated through its bottom side only, which affects the thermal performance of the power module. Moreover, as power loss increases with switching frequency, a cooling system that could remove heat through both sides of the die in a power module would be much more efficient for high-frequency operation of a power module [7]. Therefore, new low parasitic inductance and high-efficiency cooling interconnection solutions need to be developed to push the development of a power module.

In Section II, SiC material properties and SiC device potentials are introduced. In Section III, a comprehensive review of packaging schemes for Si power module is performed. In Section IV, packaging techniques for SiC power module are thoroughly overviewed. In Section V, scientific challenges in the packaging of SiC power module are summarized.

II. SiC Material Properties and Device Potentials

Fundamental properties of several different semiconductor materials are listed in Table I [3]. Compared with Si

Manuscript received May 31, 2019; revised September 15, 2019; accepted September 24, 2019. Date of publication October 15, 2019; date of current version February 3, 2020. This work was supported by the National Natural Science Foundation of China under Grant U1537208. Recommended for publication by Associate Editor Jason Neely. *(Corresponding authors: Liqiang Cao; Guoqi Zhang; Braham Ferreira.)*

F. Hou is with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China, with the Department of Microelectronics, Delft University of Technology, 2628 CT Delft, The Netherlands, and also with the National Center for Advanced Packaging, Wuxi 214135, China (e-mail: houfengze@ime.ac.cn).

W. Wang is with the Shenzhen Institute for Wide Bandgap Semiconductors (WinS), Shenzhen 518055, China (e-mail: wenbo.wang@iwins.org).

L. Cao, J. Li, and M. Su are with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China, and also with the National Center for Advanced Packaging, Wuxi 214135, China (e-mail: caoliqiang@ime.ac.cn; lijun@ime.ac.cn; sumeiying@ime.ac.cn).

T. Lin is with the National Center for Advanced Packaging, Wuxi 214135, China (e-mail: tingyulin@ncap-cn.com).

G. Zhang is with the Department of Microelectronics, Delft University of Technology, 2628 CT Delft, The Netherlands (e-mail: g.q.zhang@tudelft.nl).

B. Ferreira was with the Department of Electrical Sustainable Energy, Delft University of Technology, 2628 CT Delft, The Netherlands. He is now with the Department of Telecommunication Engineering, University of Twente, 7522 NB Enschede, The Netherlands (e-mail: j.a.ferreira@utwente.nl).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JESTPE.2019.2947645

TABLE I
FUNDAMENTAL PROPERTIES OF VARIOUS SEMICONDUCTOR MATERIALS

Property	4H-SiC	GaN	GaAs	Si
Bandgap (eV)	3.25	3.44	1.43	1.12
Intrinsic carrier concentration (cm^{-3})	8.2×10^{-9}	1.9×10^{-10}	1.8×10^{-6}	1.5×10^{10}
Breakdown electric field (MV/cm)	2.2	3.0	0.3	0.25
Thermal conductivity (W/mK)	370	130	55	150
Saturation drift velocity (10^7cm/s)	2.0	3.0	1.0	1.0
Dielectric constant	9.7	9.0	12.8	11.8
CTE (ppm/°C)	5.1	4	5.73	2.6
Young's modulus (GPa)	400	181	70	131
Density (g/cm^3)	3.21	6.15	5.3	2.3

material, the bandgap of 4H-SiC is about three times higher and the intrinsic carrier concentration of 4H-SiC is much smaller. The wide bandgap energy and low intrinsic carrier concentration allow SiC devices to operate at much higher temperature (approximately five times higher than Si devices). The breakdown electric field of 4H-SiC is an order magnitude higher than Si, making SiC devices capable of sustaining higher voltage. Moreover, a SiC device can switch at higher speed because saturation drift velocity of such device is twice of Si and thus enable at least 5–10 times higher switching frequency [3], [10], [11].

Up until now, SiC devices, such as SiC MOSFET, Schottky diode, junction gate field-effect transistor (JFET), and insulated-gate bipolar transistor (IGBT), have been produced or demonstrated. Among these devices, SiC MOSFET has received most of the attention due to its promising capabilities of replacing Si IGBT in power electronics systems [11], [12].

A SiC MOSFET is comprised of more than 10 000 small parallel-connected n-channel enhancement mode MOSFET cells. A cross section of a SiC DMOSFET half-unit cell is shown in Fig. 2 [13]. A SiC MOSFET is fabricated by beginning with an n-drift layer grown on a heavy-doped n+ substrate. In order to attain high breakdown voltage, the drift layer is lightly doped. The breakdown voltage $V_{\rm BR}$ of SiC MOSFET is influenced by the doping concentration of n-drift layer N_D and the thickness of n-drift layer w_B. The relationships can be expressed as follows, respectively [14]–[16]:

$$N_D = \left(\frac{4.45\times10^{13}}{1.25V_{\rm BR}}\right)^{4/3} \tag{1}$$

$$w_B = \sqrt{\frac{2\varepsilon_{\rm sic}V_{\rm BR}}{qN_D}} \tag{2}$$

where $\varepsilon_{\rm SiC}$ is the buck electron mobility of SiC and q is the electron charge. The drift layer resistance $R_{\rm drift}$ is given in [16], which is expressed as

$$R_{\rm drift} = \frac{w}{\varepsilon_{\rm SiC}\cdot q\cdot A_{\rm GD}\cdot N_D} \tag{3}$$

$$w = w_B - w_{\rm DSJ} \tag{4}$$

where $A_{\rm GD}$ is the gate–drain overlap area, w is the drain–source undepleted drift width, and $w_{\rm DSJ}$ is the drain–source

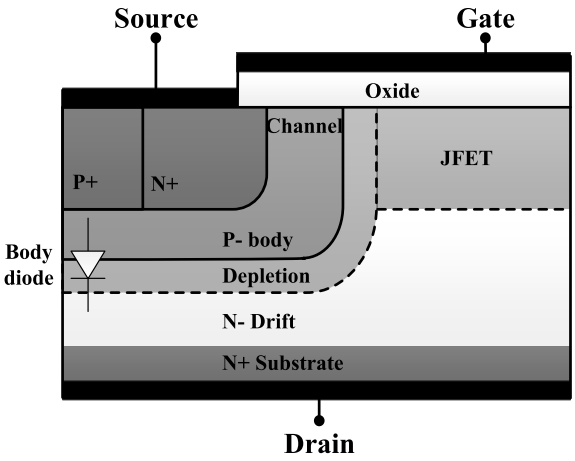

Fig. 2. Typical structure of a SiC DMOSFET half-unit cell.

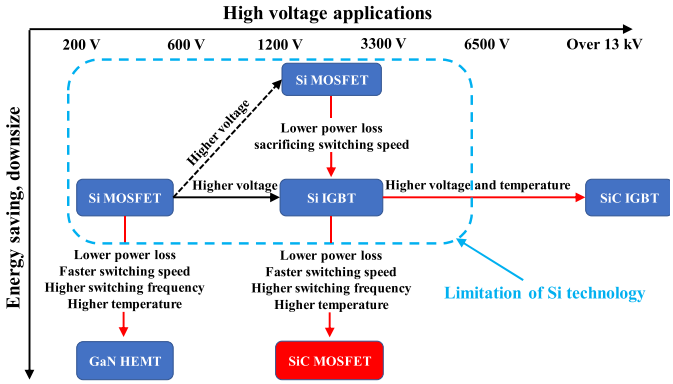

Fig. 3. Application range of Si, GaN, and SiC power devices.

depletion width. According to (1) and (2), the thicker the drift layer and the lower its doping level, the higher the breakdown voltage. On the contrary, in accordance with (3) and (4), the thinner the layer and the higher the doping level, the lower the drift layer resistance. Thus, a tradeoff exists between breakdown voltage and drift layer resistance. Moreover, the high breakdown electric field of SiC allows SiC power MOSFET with thinner and more highly doped drift layer. The more highly doped drift layer (more than ten times higher) provides lower drift layer resistance for SiC MOSFET. The thinner drift layer of SiC devices (1/10 that of Si devices) also contributes to the lowering of the drift layer resistance by a factor of 10. The combination of 1/10 the drift layer thickness with ten times the doping concentration can yield a SiC device with a factor of 100 advantages in resistance compared to that of a Si device [13], [14].

Fig. 3 shows the application range of Si, GaN, and SiC devices [17]–[20]. Switching loss of a unipolar device, such as SiC MOSFET, is relatively low as its switching speed is faster, so it can be used in high-frequency conditions. In comparison, switching loss of IGBT is higher due to its inherent slower switching speed attributed to its bipolar nature [17]. Compared with Si IGBT, the conduction loss of SiC MOSFET is lower because of its higher doping concentration in the drift region. The smaller depletion width reduces the ON-state resistance

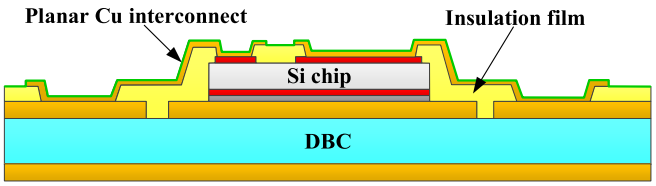

Fig. 4. Cross section of power module with planar interconnects.

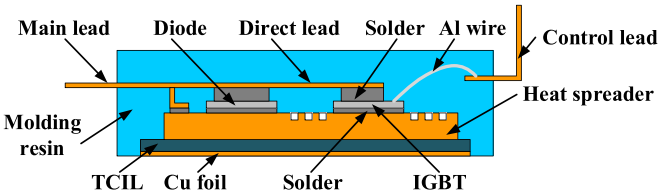

Fig. 5. Structure diagram of DLB package.

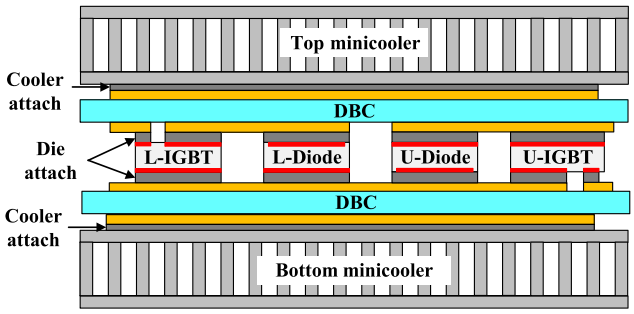

Fig. 6. Multilayer planar interconnection package structure.

of SiC MOSFET, resulting in less conduction loss. Besides, SiC MOSFET has much lower output capacitances and gate charge, and they can switch at much higher *dv/dt* and *di/dt*. High switching speed enables low switching loss and high switching frequency, which can improve the power density and efficiency of power module [18]. Moreover, switching loss of Si IGBT will increase significantly in higher operational temperature, while switching loss of SiC MOSFET has little variation over temperature [19]. Therefore, SiC MOSFET possesses definite advantages in middle-high voltage applications over competing Si counterparts.

III. Packaging Schemes for Si Power Module

Packaging techniques of Si power modules, which are the foundation of packaging methods of SiC ones, are reviewed first. Various packaging schemes for Si power module have been developed, such as planar interconnection, press pack, chip embedded package, 3-D interconnection, and hybrid package.

A. Planar Interconnect Scheme

1) Siemens Planar Interconnect Technology: Siemens introduced a novel packaging technique for power modules based on a planar interconnect technology (SiPLIT), as shown in Fig. 4. The SiPLIT featured thick Cu interconnects on a high-reliable insulating film for top contacts of power chip. Due to the conductor structure and contact technology, ON-resistance and parasitic inductances of the power module were very low in comparison to state-of-the-art Al wirebonded interconnection. In addition, the large area contacting improved power cycling capability and surge current robustness significantly. Through electrical and thermal characterization, it was found that up to 50% reduction in parasitic inductances of the interconnects and a remarkable 20% decrease in thermal resistance were achieved [21].

2) Transfer-Molded Power Module Package: Mitsubishi reported a simple, compact, robust, and high-performance transfer-molded power module (T-PM) with direct lead bonding (DLB) technology, as shown in Fig. 5. Cu lead was directly bonded on the emitter and cathode electrodes by a Pb-free solder, and Al conventional wire was bonded on the gate electrode. In order to improve the thermal performance of the T-PM, a high thermally conductive electrically insulated layer (TCIL) was applied to the module. Compared with conventional wirebonded power module, the TPM showed 43% and 50% reduction in parasitic inductance and parasitic resistance, respectively [22].

3) Multilayer Planar Interconnection Package: Liang *et al.* [23] proposed a multilayer planar interconnection package structure for a 200-A/1200-V IGBT phase-leg power module, as shown in Fig. 6. The switching dies were sandwiched between two symmetric substrates, providing planar electrical interconnections and insulation. Two minicoolers were directly bonded to outside of these substrates, allowing double-side integrated cooling. The upper switch pair and lower switch pair in the phase-leg were oriented in a face-up/face-down configuration. The bonding areas between the dies and the substrates, as well as the substrates and coolers, were designed to use identical materials and were formed in one heating process. Compared with wirebonded power module, total inductance and resistance of the planar bonded power module decreased by 62% and 90.6%, respectively. Besides, voltage overshoot reduced by 54%, and the total loss of the planar bond package was less than 10% of that of the wirebonded package. The double-sided cooling of the planar module reduced the specified thermal resistance to 0.33 $cm^2 \cdot °C/W$, which was 38% lower than that of the wirebonded power module.

4) Cu Clip Bonding Technology: The concept of Cu clip bonding technology is shown in Fig. 7. Conventional Al wirebonds were replaced with a flat Cu clip. Due to the high electrical conductivity and high thermal conductivity of Cu, the clip could not only improve the switching characteristics of the power module through reduction of parasitic inductance but also provide an additional heat conduction path from the top surface of the die [24], [25]. Compared with conventional wirebonded counterpart, up to 23% reduction in junction to case thermal resistance for one individual die and around 18% decrease for the parallel operation of two dies were observed in the single-sided cooling tests, while in the double-sided cooling experiments, an additional average of 18% thermal improvement was achieved due to the addition of a top fan-cooled heatsink mounted onto the Cu clip [25].

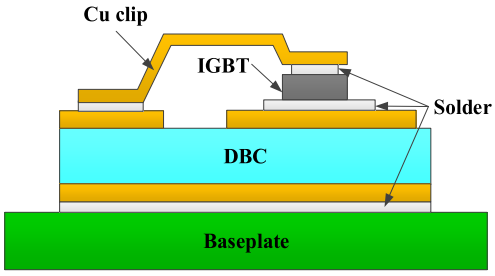

Fig. 7. Structure diagram of Cu clip bonding package.

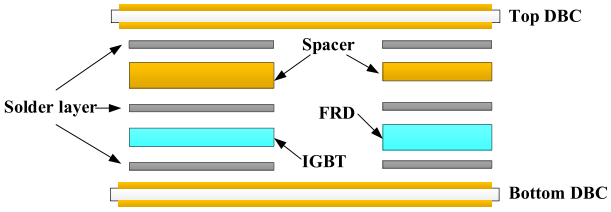

Fig. 8. Schematic of spacer-based sandwich structure.

5) Spacer-Based Sandwich Structure: Fig. 8 shows a schematic of spacer-based sandwich structure for power module. Cu spacers with different thicknesses were used to accommodate height differences between IGBT and diode in a power module [26], [27]. SAC305 solder sheet was selected as a die-attach material. To build solder bump on the IGBT and diode, an additional metallization layer was needed to be sputtered on the front-side source and gate pads to increase the wettability of solder. For this purpose, the original Al metallization of emitter, anode, and gate contact was modified by sputtering of Ti/Ni/Ag (60/500/800 nm) layers [26]. Compared with conventional IGBT module, 55.1% and 13.2% reduction in parasitic inductance and resistance and a 47.5% decrease in thermal resistance were achieved.

B. Press-Pack Packaging Scheme

Press pack is a packaging approach that uses pressure contact instead of wire bonding and soldering in conventional power modules. Press-pack packaging has been developed for high-voltage and high-current applications. Fig. 9 shows the internal construction of a rigid press pack IGBT from Westcode [28], [29]. This package employs a hermetically sealed ceramic housing, with connections to the chips made by physical contact pressure via external clamping between rigid electrodes and strain buffers. In order to ease the stress of the package induced in the operating condition, molybdenum (Mo) plates are usually used.

Fig. 10 shows a construction of a compliant press-pack power module. Compliant press-pack devices are currently available, such as those manufactured by ABB, which employ a nonhermetic plastic housing, and the actual contact pressure made to the individual chip surfaces is controlled locally by disk spring assemblies inside the package [30].

C. Chip Embedded Packaging Scheme

1) Ceramic Embedded Power Module: Fig. 11 shows a structure schematic of a ceramic embedded power module [31]. Multiple power chips, such as IGBT, MOSFET,

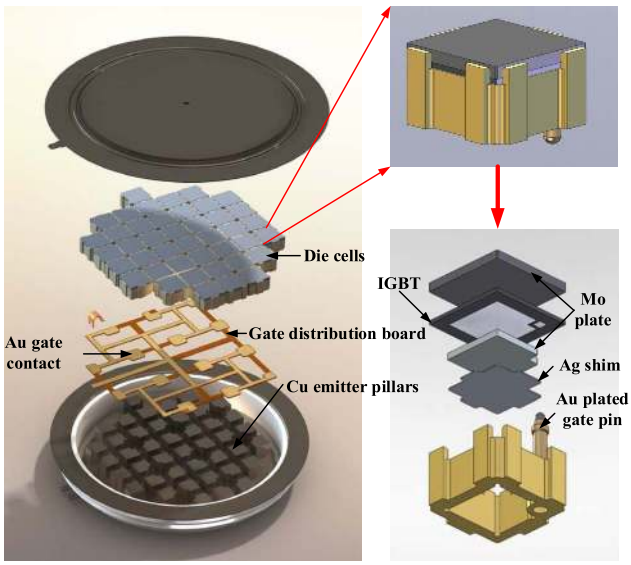

Fig. 9. Internal construction of a press pack IGBT from Westcode.

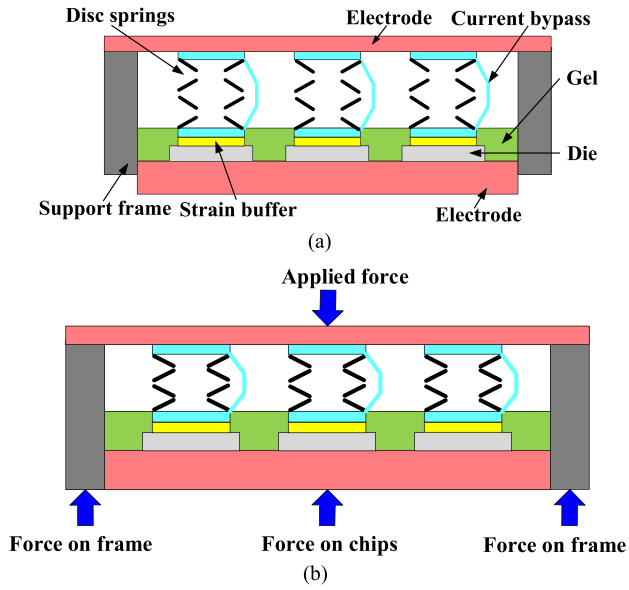

Fig. 10. Construction of a compliant press-pack IGBT. (a) Before compression. (b) After compression.

and diode, were embedded in a ceramic frame and covered by a dielectric layer with via holes on the Al pads of the chips. Then, metallization multilayers were deposited on the whole surface which formed contacts with the Al pads on the chips through via holes in the interlayer. Conventional sputtering was employed to deposit thin-film Ti and Cu layers. Electroplating was used to form thicker Cu deposition. Finally, the metallization layer was patterned to form both power and control circuits as well as their I/O terminals. Compared with conventional wirebonded package, a 75% reduction in parasitic inductance and a 44% improvement thermal dissipation performance were achieved.

2) PCB Embedded Power Module: Printed circuit board (PCB) embedded package, also called "chip in polymer" technology, was first introduced by Fraunhofer IZM and TU Berlin. The ultrathin semiconductor chips were

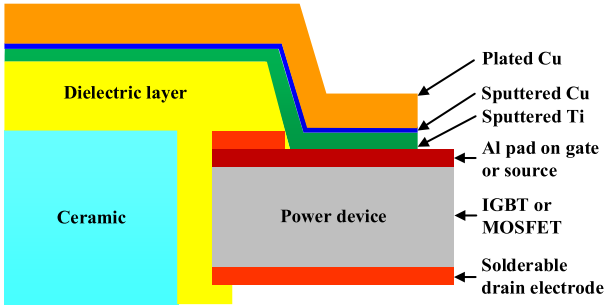

Fig. 11. Structure schematic of a ceramic embedded power module.

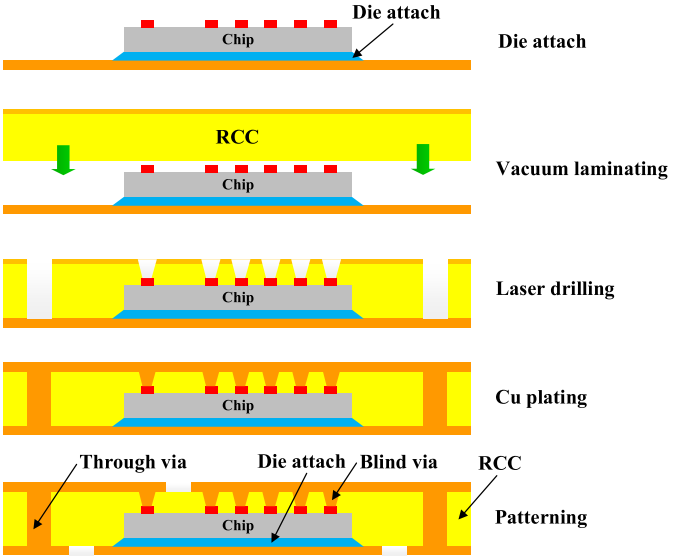

Fig. 12. Process flow of PCB embedded package developed by Fraunhofer IZM and TU Berlin.

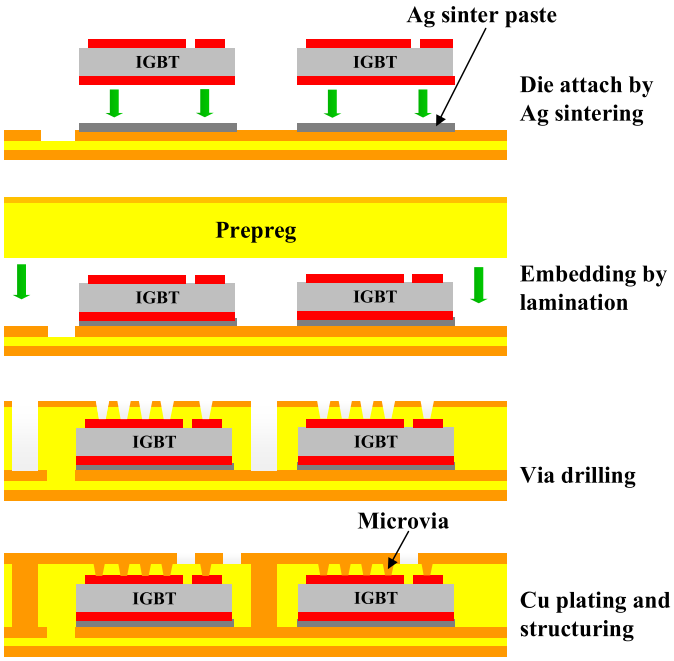

Fig. 13. Process flow of PCB embedded IGBT module developed by Fraunhofer IZM and TU Berlin.

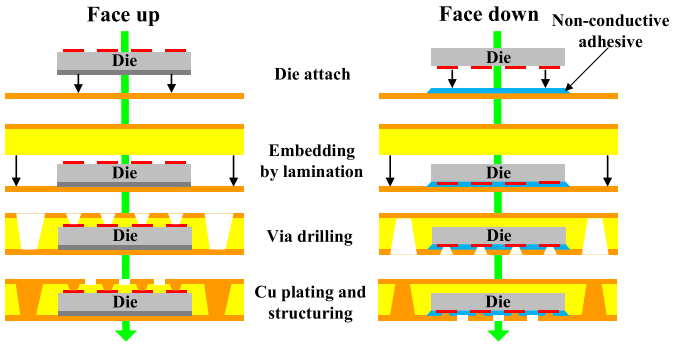

Fig. 14. PCB embedding process flows: face-up (left) and face-down (right).

embedded into the build-up layers of PCB together with integrated passive components. Electrical interconnection between chip and outer layer footprints were realized by laser-drilled and metallized microvias [32]–[34]. The detailed packaging process is shown in Fig. 12 [33].

In 2013, Fraunhofer IZM and TU Berlin developed a PCB embedded packaging scheme for IGBT power module. In order to be compatible with laser drilling and Cu plating, a thin electroless Ni/Pd layer was added on IGBT and diodes [34]. The process flow is shown in Fig. 13. At first, a base substrate was manufactured by lamination of thick Cu and a thermally conductive prepreg layer. The top Cu layer was structured and selectively metalized by immersion Ag. Then, Ag sinter paste was printed to Ag areas and IGBTs and diodes were placed and sintered into the substrate at 200 °C with a relatively low pressure of 2 MPa. Third, IGBTs and diodes were embedded into a prepreg layer with 105-μm Cu foil through vacuum lamination. Vias to chip pads and thick Cu were drilled by laser. Finally, the vias were filled with Cu by electroplating and the Cu was structured by etching [35].

PCB embedded packaging technologies for power modules mainly include two process flows: face-up and face-down, as shown in Fig. 14 [36]. Die-attach material used in the face-down process is nonconductive adhesive, while for face-up technology, die-attach material can be nonconductive adhesive, solder, sintered Cu/Ag, and so on. The face-up technology is more suitable for high power-density vertical dies, such as MOSFET, IGBT, and diode.

Pascal *et al.* [37] proposed an innovative PCB embedded manufacturing process, as shown in Fig. 15. They used a piece of nickel foam to create a pressed contact between the top side of a PCB embedded power die and the rest of the circuit. The average pore diameter of the nickel foam was about 350 μm, and there were 57–63 pores/in. The detailed packaging process flow is as follows. First, as shown in Fig. 15(a), the bottom side of the diode is soldered onto a bottom PCB. Then, a piece of nickel foam, four layers of prepregs, and a top PCB are positioned above the bottom PCB, as shown in Fig. 15(b). Third, as shown in Fig. 15(c), the stack is laminated through high-temperature and high-pressure process, and the epoxy resin polymerizes and floods the foam. Compared with other PCB integration techniques, the proposed process is simple and cost-effective.

Munding *et al.* [38] reported a new lead frame-based laminate chip embedding technology. The packaging process

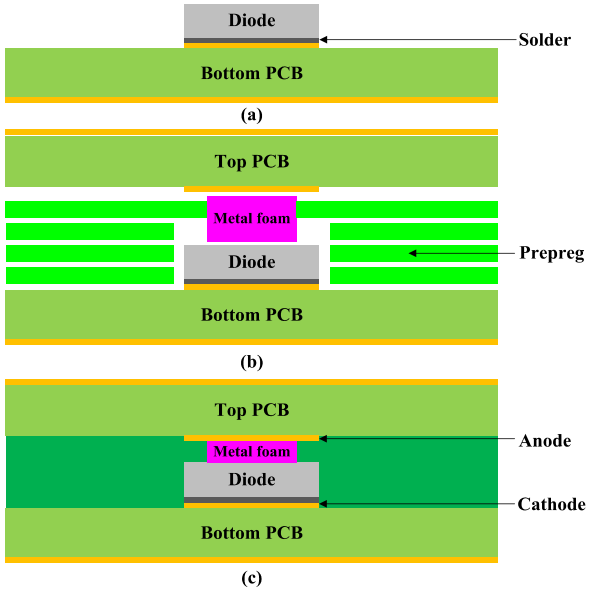

Fig. 15. Steps of packaging process using metal foam.

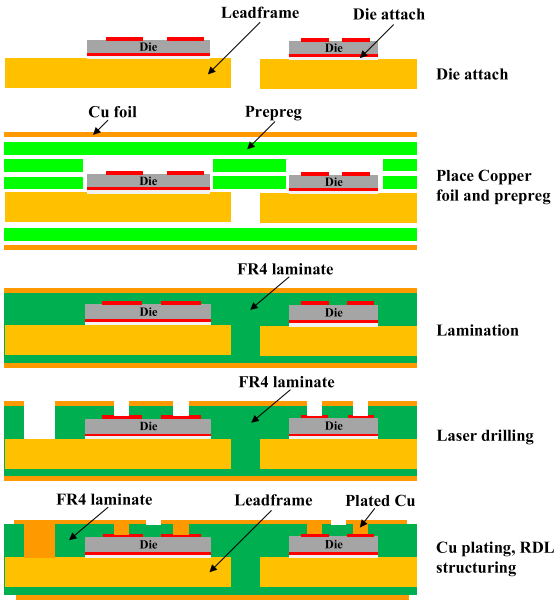

Fig. 16. Process flow of lead frame-based laminate chip technology.

flow is shown in Fig. 16 in detail. For power dies with vertical current flow, diffusion solder was adopted as die-attach layer, while for gate driver, insulating glue was also used. They presented a study on the laminate material choice and found that prepreg material with highly filled glass fibers and high Tg (glass transition temperature) was more robust than resin-coated copper (RCC) material. Then, they proposed a novel approach to avoid lamination voids, validated lamination process simulation based on the Monte Carlo method, and could predict process stability for a specific set of parameters and parameter variations. Third, they systematically analyzed the physics mechanism of laser-induced chip metallization damages and define countermeasures to avoid such damages.

Kearney *et al.* [39] developed a 1200-V PCB embedded three-phase IGBT inverter module, as shown in Fig. 17.

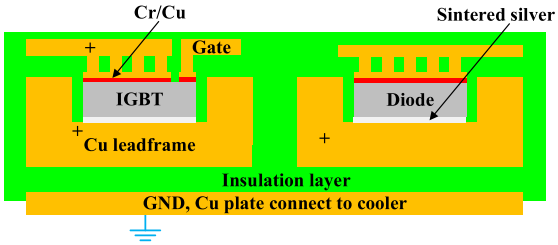

Fig. 17. PCB embedded three-phase inverter module.

The PCB embedded technology requires Cu metallization of the chips. The original Al metallization of emitter, gate, and anode contact was modified by sputtering Cr/Cu (5 nm/8 μm) layers, while a portion of the individual chip was protected with a shadow mask. Then, six pairs of IGBT and diodes were sintered into a Cu lead frame with premachined cavities. Cu vias from outer Cu traces to chip pads were formed by laser drilling, electroplating, and so on. Comparing the switching performance, thermal resistance, breakdown insulation, partial discharge, and long-term aging with Semikron MiniSKiiP 23AC126V1 that used a traditional DBC sandwich structure, the PCB embedded module improved thermal management, reliability, and insulation.

Chang *et al.* [40] presented an IGBT power module package by a chip embedding technology. The package process flow is shown in Fig. 18. Because the size and thickness of IGBT and diode adopted in the module are different from each other, a half-etched Cu lead frame was designed and fabricated. The IGBTs were attached to the lead frame by SAC305 solder paste, whereas the thicker diodes were sintered onto the half-etched Cu lead frame. Then, an ABF lamination process was conducted to form a built-up dielectric layer on the Cu lead frame. Next, the blind vias and circuits were formed on the built-up dielectric layer by a UV laser and were metalized with sputtered seed layer and electroplating. To form a circuit pattern, an additional 1-μm-thick Sn layer was subsequently plated as a patterning mask, and a laser skiving process was conducted to remove Sn above the Cu layer. Thereafter, the etching of Cu, Sn, and Ti processes was performed to remove the metal on the dielectric layer, thus forming the required circuit pattern. Finally, a layer of solder mask was printed to prevent electric shock on the surface layer.

AT&S developed a panel-level PCB embedded lateral device package technology, known as embedded component packaging (ECP). The packaging process flow is shown in Fig. 19 [41]. The micro-vias were used as electrical interconnections and thermal conduction between the chip and Cu layers on the top and bottom surfaces [42], [43].

D. 3-D Interconnect Scheme

1) Power Chip-on-Chip Package: In order to reduce parasitic inductances, Marchesini *et al.* [44] presented a power chip-on-chip (PCoC) packaging technology for IGBT power module, as shown in Fig. 20. Electrical interconnection of the switching cell was realized through two DBC substrates and a four-layer PCB. DC link and decoupling capacitors were integrated directly on the PCB. The experimental results

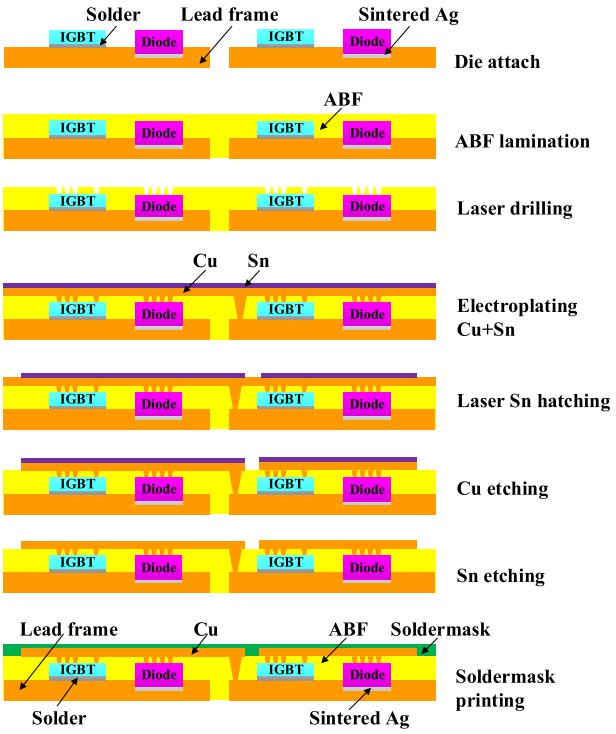

Fig. 18. Process flow of IGBT power module by chip embedding technology.

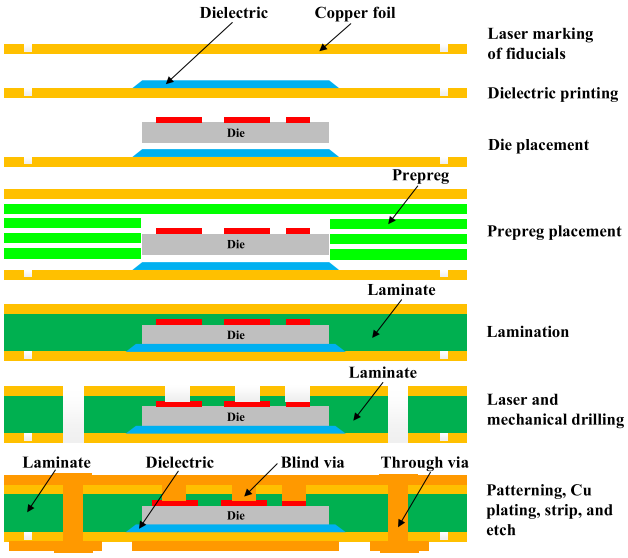

Fig. 19. AT&S ECP process flow.

showed that the parasitic inductance of the PCoC module was drastically reduced compared with planar ones, especially when internal decoupling capacitors were integrated in the assembly.

2) Power Chip-on-Inductor Package: In [45], a power chip-on-inductor (PCoI) packaging technique with double-sided cooling was presented. The structure diagram of PCoI package is shown in Fig. 21. A fan-out panel-level PCB embedded packaging technique for power MOSFETs and low-temperature co-fired ceramic (LTCC) inductor in a synchronous converter was proposed. The power MOSFETs and LTCC inductor were embedded in the top and the bottom PCB, respectively. A stacking of the top PCB and the bottom

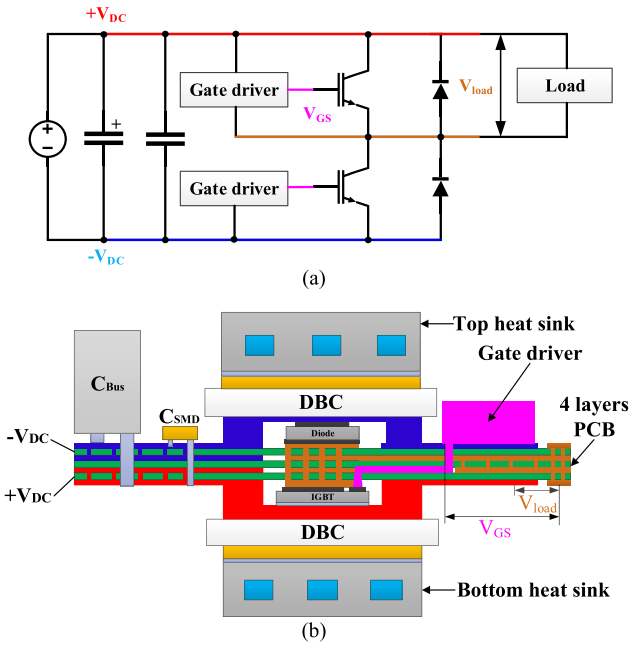

Fig. 20. PCoC package. (a) Electric circuit. (b) Structure diagram.

PCB was implemented to form a 3-D integrated power supply module. The MOSFETs, gate driver, and passive components were interconnected by the redistribution layer (RDL) and PCB vias. According to thermal simulation results, PCB vias could improve the thermal performance of the 3-D module with cap heat spreader, which could effectively dissipate heat of the PCB embedded 3-D power supply module.

3) Micro-Post-Based Sandwich Structure: Micro-post-based sandwich structure is one of the 3-D interconnection configurations with double-sided cooling capability. Fig. 22 shows the schematic of Cu micro-post interconnection for power module. The Cu micro-posts were electroplated on topside of the die. The die with its micro-posts was then attached to a top DBC substrate using a Cu/Sn transient liquid phase (TLP) technique. An assembly of backside of the die to a bottom DBC substrate was processed concurrently using the same TLP technique [47]. In this bonding technique, a layer of Sn (0.5 μm) was deposited on top of the posts, which was used as a solder between the posts and the Cu of the DBC substrate. Another bonding solution, Cu–Cu bonding, does not need any additional materials between micro-posts and the Cu of the DBC substrate [7].

The micro-post-based sandwich structure allows for cooling from two sides. The Cu posts provide spacing between the die and the top substrate. They are also useful to accommodate height differences between the dies in a multichip power module. Different types of dies (such as IGBT and diode), which are commonly used in a single module, do not always have the same thickness. The Cu micro-posts can compensate for thickness differences between the dies [6].

4) Solderless Lead Frame-Assisted Wafer-Level Packaging: In [46], a wafer-level packaging technique for power module was presented. Fig. 23 shows the schematic of the assembly with two Si wafers covered with Cu layer and the patterned and perforated Cu lead frame. A metallic lead frame was bonded between two wafers of semiconductor devices.

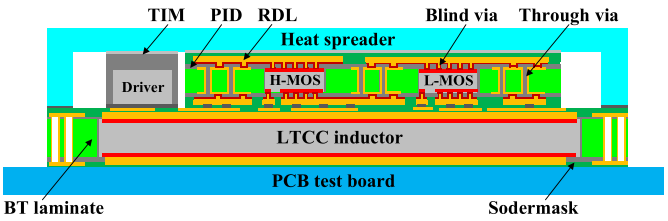

Fig. 21. Structure diagram of PCoI package.

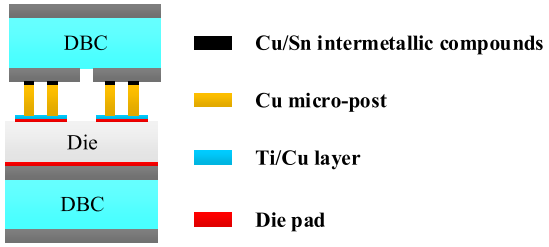

Fig. 22. Schematic of Cu micro-post interconnection for power module.

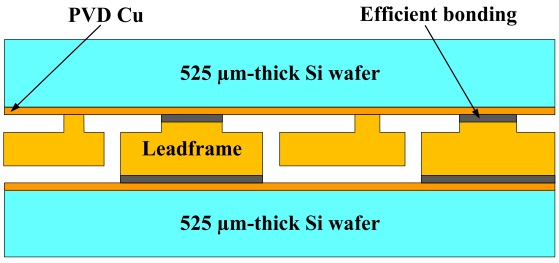

Fig. 23. Schematic of the assembly with two Si wafers covered with Cu layer and the patterned and perforated Cu lead frame.

The 3-D assembly of the power devices and the metallic lead frame was realized by a solderless, thermocompression bonding.

5) Hybrid Packaging Scheme: Since high-power devices are usually metallized by Al on the top pads to be suitable for Al bonding wires, almost all wirebondless package structures require that the top electrode pads of power devices are remetallized, while in some hybrid packages, remetallization process is not needed and wire bonding techniques are still suitable.

Switching Cell-Based Package: In [48], a switching cell-based IGBT phase-leg module was proposed. Fig. 24(a) and (b) shows the conventional module and p-cell and n-cell-based module, respectively. Compared with the conventional module, two devices in the commutation loop of the p-cell and n-cell module were placed at the same side, and thus, the physical length of the commutation loop was reduced. The parasitic inductance reduction of the layout design was in the range of 5–10 nH.

Table II presents a summary of different packaging schemes for Si power module.

IV. Packaging Techniques for SiC Power Module

Up to now, attempts for packaging SiC power module, e.g., planar packaging, press pack, 3-D packaging, and hybrid packaging techniques, have been performed.

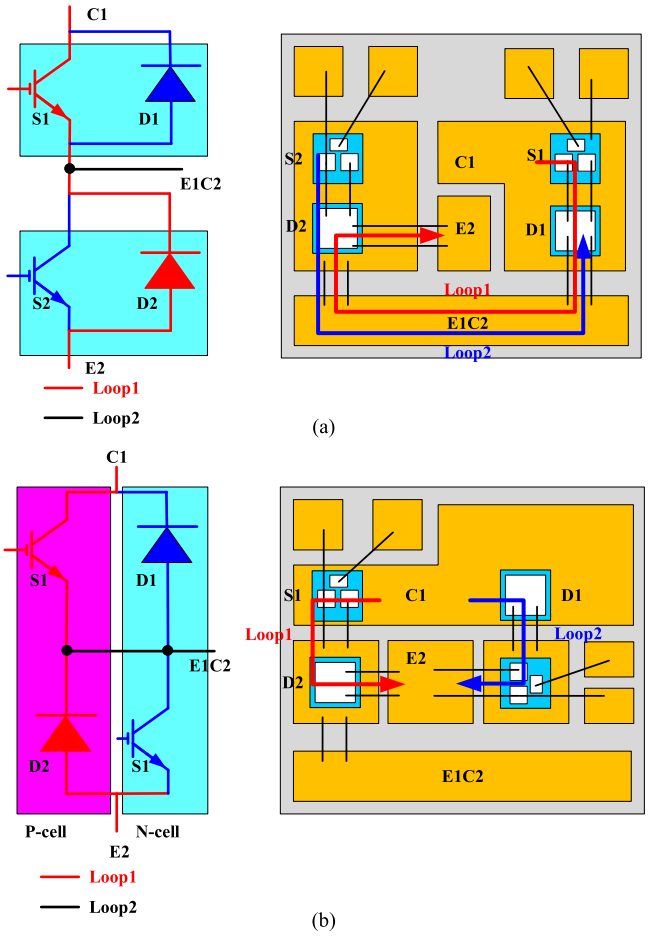

Fig. 24. Phage-leg package layout. (a) Conventional module. (b) p-cell and n-cell-based module.

A. Planar Packaging Technique

1) Miniaturized Double-Side Cooling: Rhee *et al.* [49] developed a miniaturized double-sided cooling packaging for SiC high-power inverter module using new materials to withstand high temperature over 220 °C, as shown in Fig. 25. The flip-chip bonding for source and gate interconnections was developed, and Bi–Ag solder paste was adopted. Its solidus temperature is around 260 °C and liquidus temperature is around 360 °C, which has much high thermal stability than conventional lead-free solder. In order to increase the wettability of solder paste, an electroless nickel immersion gold process on the Al bonding pads on the DMOSFET surface was performed. For drain interconnection, Cu clips were attached using Ag sintering materials. Through thermal modeling and characterization, thermal dissipation performance of power module was found to be enhanced by twice compared with the conventional single-side cooling-type power module.

2) Power Overlay Interconnect Packaging: General Electric developed a power overlay (POL) interconnect technology for SiC MOSFET packaging. The sources and gates of MOSFETs were interconnected by a flexible substrate, as shown in Fig. 26. Because the parasitic inductances of the package were greatly decreased, the POL showed low-voltage overshoot, which is the product of parasitic inductance and *di/dt*. When the drain–source voltage was 540 V and drain current

TABLE II
COMPARISON AMONG DIFFERENT PACKAGING SCHEMES FOR SI POWER MODULE

Packaging scheme	Features
SiPLIT [21]	• Thick Cu interconnects on a high-reliable insulating film. • 50% reduction in parasitic inductances of the interconnects and a remarkable 20% decrease in thermal resistance are achieved.
T-PM [22]	• Cu lead is directly bonded on the emitter and cathode electrodes by Pb-free solder; • TCIL is applied to the module.
Multilayer planar interconnection [23]	• Double-sided cooling; • Structure symmetry; • Switch pairs in phase-leg are oriented in face-up/face-down configuration; • Total inductance is 12.08 nH; • The specified thermal resistance is 0.33 $cm^2 \cdot °C/W$.
Cu clip [24]-[25]	• Wire-bonds are replaced with a flat Cu clip; • up to 23% reduction in junction to case thermal resistance for one individual die.
Spacer-based sandwich [26]-[27]	• Double-sided cooling; • Cu spacers with different thickness are used to accommodate height differences of IGBT and diode; • 55.1% and 13.2% reduction in parasitic inductance and resistance and a 47.5% decrease in thermal resistance are achieved.
Press-pack [28]-[30]	• High-voltage and high-current application.
Ceramic embedded package [31]	• Integrate all switches into a single embedded power module; • A 75% reduction in parasitic inductance and a 44% improvement thermal dissipation performance was achieved.
PCB embedded package [32]-[43]	• Small form factor; • Light weight; • Simple packaging process.
PCoC package [44]	• 3D integration through DBC substrate and PCB.
PCoI package [45]	• Low parasitic inductance; • Structure symmetry; • Double-sided cooling.
Wafer-level package [46]	• Power devices and metallic lead frame are bonded by a solderless, thermocompression process.
Micro-post-based sandwich [47]	• Double-sided cooling; • Micro-posts on the top of power dies can be performed at wafer level; • Micro-posts can compensate for thickness differences between the dies.
Switching cells-based package [48]	• Reduction in the physical length of commutation loop. The parasitic inductance reduction of the layout design was in the range of 5-10 nH.

was 300 A, the voltage rise time was 11.2 ns, and voltage overshoot was below 28% [50].

In 2018, they presented a power overlay kiloWatt (PO-kW) for SiC power module. The schematic of a typical POL-kW module structure is shown in Fig. 27. Cu vias were used as interconnects between dies (Al pads) and routings on the polyimide film surface. The adhesive layer was used to attach dies to the polyimide film. Cu vias were formed by laser drilling and subsequently filled by electroplating. DBC substrate (Ni/Au finish) was soldered to the die backside metallization (Ag finish). An underfill was applied for electrical isolation and mechanical strengthening. Compared with conventional wirebonded package, the utilization of polyimide-based Cu via interconnections resulted in much

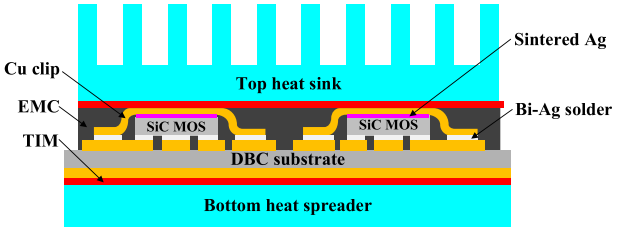

Fig. 25. Double-side cooling packaging for SiC high-power inverter module.

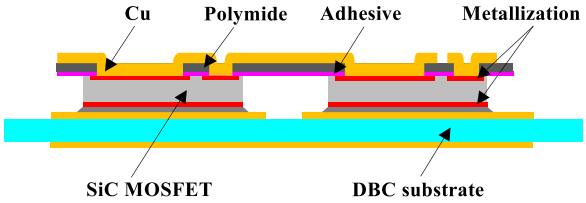

Fig. 26. Schematic of POL interconnect package for SiC MOSFETs.

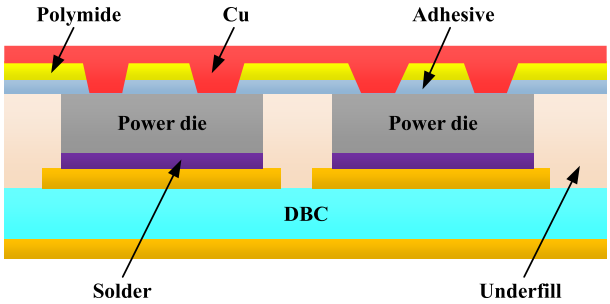

Fig. 27. Schematic of a typical POL-kW module structure.

reduced parasitic inductance, contributing to significantly lower switching loss and less voltage overshoot [51].

3) LTCC-Based Double-Sided Cooling Module: Zhang *et al.* [52] proposed a wirebondless SiC power module with a double-sided cooling capability. In this module, an LTCC substrate was used as a dielectric and chip carrier. Nano Ag paste was used to attach power devices to top and bottom DBC substrates as well as to pattern the gate connection. The top and bottom sides of DBC were plated with Ag on top of the 8-mil-thick Cu, and the subsequent layers of Cr/Ni/Ag were deposited on top of the anode of the diode, the source, and gate of the MOSFET through a liftoff process. To protect the power devices from electrical breakdown during operation, a high-temperature dielectric material was used to fill the gaps between the LTCC substrate carrier and the power devices. The cross section of the power module with double-sided cooling is shown in Fig. 28. Simulation results showed that the LTCC-based double-sided cooling module had the lowest junction to ambient thermal resistance compared to the embedded power and PBGA modules under similar operating conditions.

4) 6-in-1 Power Module: In order to reduce the inductance of wiring, magnetic cancellation effect was used. Fig. 29 shows the cross section of a 6-in-1 SiC power module with double-sided cooling. Heat spreader was utilized as magnetic cancellation. Laminated busbar had an insulation film between positive and negative terminals, in which current paths were in the opposite directions. Current paths between

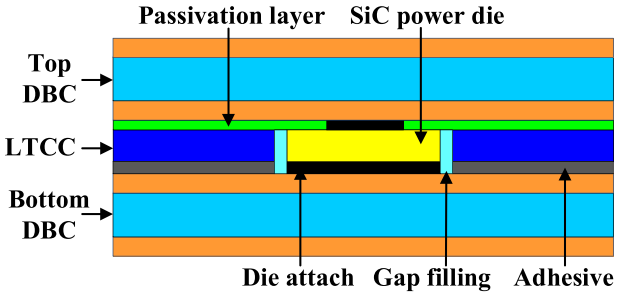

Fig. 28. Cross section of LTCC-based double-sided cooling for SiC module.

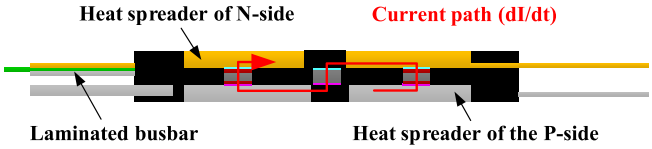

Fig. 29. Current path and structure view of 6-in-1 power module.

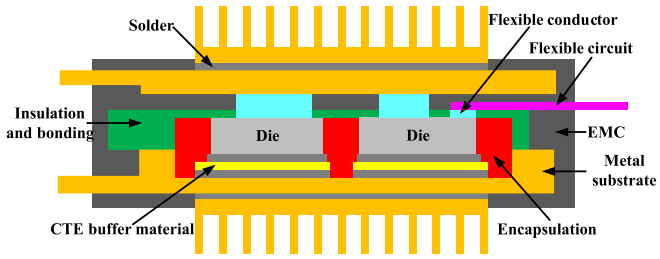

Fig. 30. Structural view of PCoB power module.

the chips were also configured to be in opposite directions. A parasitic inductance of 7.5 nH was obtained [53].

5) Power Chip-on-Bus Structure: In [54], a double-sided air-cooled power chip-on-bus (PCoB) power module was proposed. Fig. 30 shows the structural view of PCoB power module. Thick finned Cu acted as both heatsink and busbar. Power dies were electrically attached to two busbarlike power substrates directly. Mo spacers were used as CTE buffer between the die and bottom substrate for reducing thermomechanical stress caused by CTE mismatch. Through extensive multiphysics simulation and verification, 0.5 °C/W thermal resistance and 8-nH power loop parasitic inductance were achieved.

B. Press-Pack Packaging Technique

1) Press-Pack Packaging Solution Based on LTCC Interposer: Zhu *et al.* [55] proposed a press-pack packaging solution for SiC MOSFETs, as shown in Fig. 31. A pressure contact solution for SiC MOSFET die was developed using miniature and flexible press pins called "fuzz buttons" in a low-profile LTCC interposer. To minimize the loop parasitic inductance, ultrathin microchannel heatsinks were designed based on the LTCC technology. A phase-leg stack prototype with two press packs and three heatsinks was developed. According to the simulation results, the internal parasitic inductances of the press pack were less than 550 pH, and the parasitic inductance of a phase-leg stack formed by two press packs and three microchannel heatsinks was 4.3 nH at a frequency of 100 kHz.

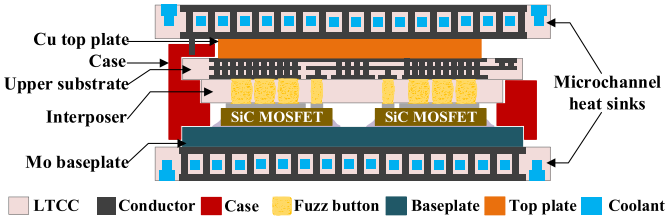

Fig. 31. Press-pack packaging solution for SiC MOSFETs.

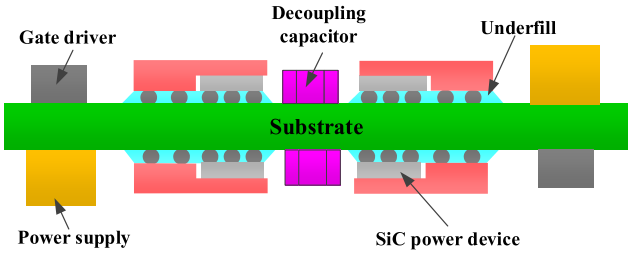

Fig. 32. Diagram of 3-D wirebondless switching cells.

C. 3-D Packaging Technique

1) Chip Scale, Flip-Chip Capable Package: Seal *et al.* [56], [57] and Mantooth and Ang [58] developed a chip-scale wirebondless packaging technology for a SiC Schottky diode that led to lower parasitics, higher reliability, lower costs, and lower losses. The approach used a flip-chip solder ball array to make connections to the anode. A Cu connector was used to make contact with the bottom cathode, thus reconfiguring the bare die into a chip-scale, flip-chip capable device. Compared with conventional wirebonded package, a 24% reduction in ON-state resistance was observed in the wirebondless package. In 2018, they presented a 3-D wirebondless switching cell using SiC power devices, as shown in Fig. 32. In order to obtain a solderable finish, a very thin zinc seed layer was deposited on the top Al pads, followed by the electroless plating of a thick nickel layer. Double-pulse tests showed that over three times reduction in the parasitic inductance of the 3-D cell compared with a conventional wirebonded module [59].

2) Cu Pin Connection Technology: Fuji Electric developed a Cu pin interconnection structure for SiC power module, as shown in Fig. 33. Conventional Al wirebonds, solder joints, and silicone gel encapsulating structures were replaced with Cu pin connections, Ag sintering joints, and epoxy resin molding structures, respectively. In order to further reduce thermal resistance, a much thicker Cu block was bonded to the silicon nitride (Si_3N_4) ceramic substrate. Compared with conventional alumina ceramic structure, the Cu pin structure enabled a 50% reduction in the thermal resistance of the overall structure. Compared with the conventional Si-based wirebonded package, the loss reduction with SiC devices was 57%–87% using the Cu pin structure [60], [61].

3) SKiN Interconnect Technology: SKiN technology comprises sintering of power chips to a DBC substrate, a top side sintering of the power chips to a flexible printed circuit (FPC), and sintering of the substrate to a pin-fin heat

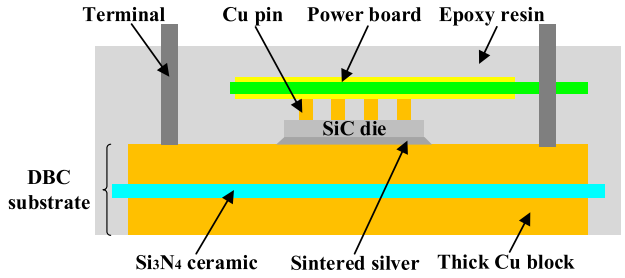

Fig. 33. Package structure schematic of SiC power module with Cu pin.

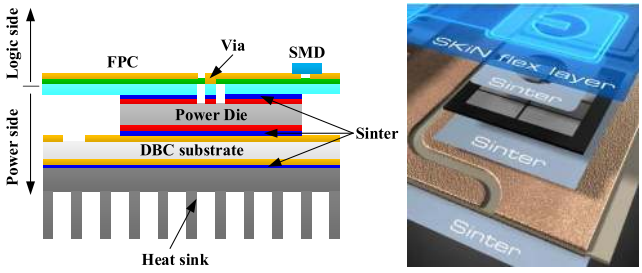

Fig. 34. SKiN double-side sintering package.

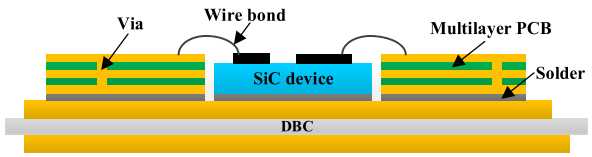

Fig. 35. Cross-sectional view of DBC and PCB hybrid structure.

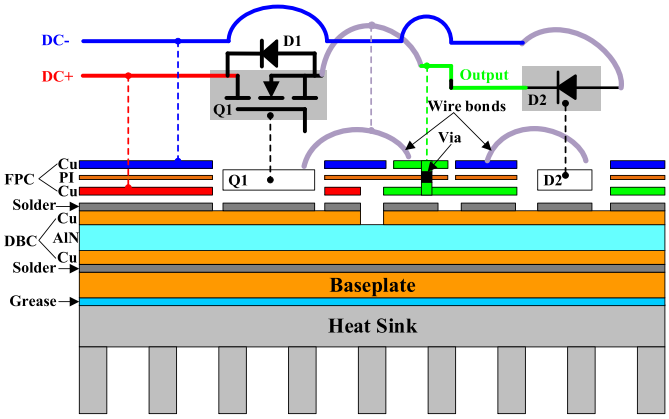

Fig. 36. DBC and FPC hybrid structure.

sink, as shown in Fig. 34. This technology was first introduced in 2011 in [62]. Now, it has been used in a 1200-V, 400-A phase-leg SiC power module. The phase-leg power module with 8 × 50 A SiC MOSFET chips in parallel had a total commutation parasitic inductance of less than 1.4 nH [63].

D. Hybrid Packaging Technique

1) DBC and PCB Hybrid Structure: In [64], a DBC and PCB hybrid structure for SiC power module was developed, as shown in Fig. 35. A multilayer PCB with grooves was attached on the DBC substrate. SiC devices were fit in the grooves and attached on the DBC substrate. Bonding wires were then used to connect the top electrodes of the device to top Cu trace on the PCB.

2) DBC and FPC Hybrid Structure: In [65], a 1200-V, 120-A SiC phase-leg power module based on DBC and FPC hybrid structure was proposed. Fig. 36 shows the DBC and FPC hybrid structure and the commutation loop associated with MOSFET (Q1) and diode (D2). Since the opposite currents flowed through the thin FPC board, the cancellation of the magnetic coupling effect was strong. The parasitic inductance of the power module could be significantly minimized to only 0.79 nH by using the thin FPC and proper layout design. Compared with the commercial module, voltage overshoot of the hybrid structure module was decreased by about 50%, and switching energies were only one-third of the commercial module under the same decoupling capacitors and driving conditions.

Up to date, several packaging technologies for SiC power module have been developed. Although some similar packaging schemes for Si-based power module has also been explored, requirements on parasitic inductance and heat dissipation for SiC power module package are more stringent. There exist challenges in the packaging of SiC power modules due to unique features of the newly developed modules, e.g., high-speed and high-frequency switching. Comparison among these packaging schemes for SiC power module is listed in Table III.

V. Challenges of Packaging Techniques for SiC Power Module

Compared with Si counterparts, SiC MOSFETs have faster switching speed, smaller form factor, and lower switching loss and can realize higher switching frequency and efficiency. In the same power module package, however, superior properties of a SiC MOSFET cannot be exploited if it is used simply as a direct replacement of Si device [64]–[66]. These features of SiC MOSFETs pose substantial challenges to packaging of SiC power module, e.g., fast switching speed and heat dissipation. Developing novel packaging technique needs to face several challenges, e.g., material selection and packaging process. Once a new package is developed, module characterization is also a challenge. These issues must be handled more carefully in the SiC MOSFET power module packaging design.

A. Fast Switching Speed

A comprehensive comparison between Si IGBT and SiC MOSFET with the same power rating was performed in [67]. The selective devices are from Infineon's third-generation Si IGBT IKW15N120H3 and Cree's SiC MOSFET C2M0080120D. The quantitative *dv/dt* and *di/dt* values of the two devices are shown in Table IV. As seen in Table IV, SiC MOSFET switches much faster than Si IGBT. Due to fast switching speed capability, switching characteristics of SiC MOSFET are more susceptible to parasitic elements,

TABLE III
COMPARISON AMONG THE EXISTING PACKAGING SCHEMES FOR SiC POWER MODULE

Packaging scheme	Feature
Miniaturized double side cooling [49]	• Double-sided cooling with flip-chip and clip bonding; • Withstand high temperature over 220 °C; • 2 times enhancement in thermal dissipation performance is achieved.
POL [50]-[51]	• Wire-bonds are replaced with flexible substrate.
LTCC based double-sided cooling [52]	• Double-sided cooling; • LTCC interposer is used as dielectric and chip carrier; • Parasitic inductance of 3.3 nH is achieved.
6-in-1 [53]	• Double-sided cooling; • Magnetic cancellation effect is used; • Parasitic inductance of 7.5 nH is obtained.
PCoB [54]	• Double-sided air-cooling; • As a CTE buffer between die and substrate, Mo spacers are used to reduce thermo-mechanical stress; • 0.5 ºC/W thermal resistance and 8 nH power loop parasitic inductance are achieved.
Press-pack package based on LTCC interposer [55]	• Double-sided cooling based on LTCC based microchannel; • A miniature and flexible "fuzz buttons" in a low-profile LTCC interposer is used; • The total parasitic inductance is 4.3 nH at a frequency of 100 kHz.
Chip scale, flip-chip package [56]-[59]	• Flip-chip solder ball array is used to make connections to the anode; • A Cu connector is used to contact the bottom cathode; • A 24% reduction in on-state resistance is observed.
Cu pin connection [60]-[61]	• Wire-bonds are replaced with Cu pin; • Si_3N_4 based DBC substrate is used; • A 50% reduction in thermal resistance of overall structure is obtained.
SKiN [62]-[63]	• Sintering of power chips to a DBC; • A top-side sintering of power chips to an FPC; • Sintering of the DBC to a pin-fin heat sink; • A total commutation parasitic inductance is less than 1.4 nH.
DBC and PCB hybrid structure [64]	• Simple packaging process; • Much more complicated routing can be achieved; • Ultra-low loop inductances can be realized.
DBC and FPC hybrid structure [65]	• Cancellation of magnetic coupling effect is strong; • Parasitic inductance can be significantly minimized to only 0.79 nH by using thin FPC and proper layout design.

TABLE IV
SWITCHING SPEED EVALUATION OF SiC MOSFET AND IGBT [67]

Feature	Turn-on		Turn-off	
	SiC MOSFET	IGBT	SiC MOSFET	IGBT
dv/dt (kV/μs)	40	16	27	8
di/dt (kA/μs)	1.1	0.5	0.3	0.06

i.e., parasitic inductances of interconnections and parasitic capacitances [68].

In the phase-leg configuration, crosstalk, which refers to the spurious triggering of the low-side SiC MOSFET during the turn-on transition of the high-side SiC MOSFET and vice versa, is one of the failure mechanisms of power module. Due to high *dv/dt* at turn-on transient of one MOSFET, parasitic capacitance of the other MOSFET easily causes a gate voltage spike that could result in spurious turn-on if the induced gate voltage exceeds the threshold voltage of SiC MOSFET. The undesired power losses are then generated in both high- and low-side MOSFETs, leading to an increase in their junction temperature and decrease in efficiency [69]. SiC MOSFET is more vulnerable to false triggering due to its low threshold voltage compared with Si counterpart [69], [70]. For instance, threshold voltage of IGBT 5SMY 12K1280 from ABB is 5–7 V [71], while for SiC MOSFET CPM2-1200-0025B from CREE, the value is only 2.6 V [72].

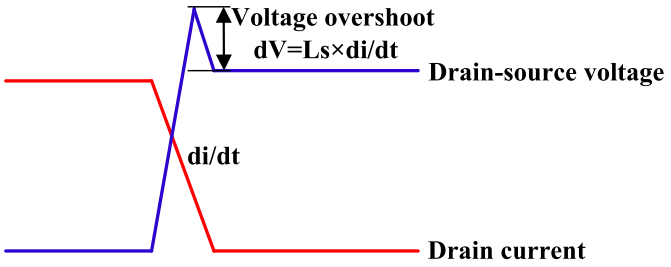

Fig. 37. Illustration of voltage overshoot caused by parasitic inductance.

The high *di/dt* at turn-off transient easily leads to voltage overshoot, generates circulating energy loss, and also causes EMI and compatibility problems due to the parasitic inductances [73], [74]. Fig. 37 shows the voltage overshoot caused by parasitic inductance. In order to avoid the large overshoot, much smaller parasitic inductance is required for fully utilizing the fast switching characteristics of SiC MOSFET [75]–[77].

B. Heat Dissipation

The switching frequency of Si IGBT-based converters is normally limited to 20 kHz, but the switching frequency of SiC MOSFETs can reach 100 kHz in a hard-switching converter [78]. With soft switching, the switching frequency can be even higher [79]. However, increasing switching frequency is also increasingly inflicted with higher switching loss that can considerably compromise efficiency [80]. In addition, with the small form factor, power-loss density of SiC MOSFET will be larger in the high frequency. As a consequence, thermal management of SiC power module is more challenging, especially in high frequency. Conventional single-sided cooling schemes are not capable of meeting heat dissipation of SiC power module in such applications. Novel double-sided or multisided liquid or two-phase flow boiling cooling has great potentials to solve its heat dissipation issue while maintaining the chip junction temperature at a low temperature.

C. Material Selection

Limited by available packaging materials, junction temperatures of SiC power modules are subjected to ∼175 °C, even though SiC devices are, in theory, capable of operating at high temperature up to 600 °C [3], [81]. Most packaging materials adopted in the Si-based power modules, e.g., die attach and encapsulant, cannot survive temperatures over 175 °C for a

long time, prohibiting application of the SiC power modules in a high-temperature environment. High-temperature die-attach alternatives, such as organic die attach, high-temperature lead-free solders, and sintering of micro- and nano-Ag powders, seem to be potential candidates [3]. These high-temperature die-attach alternatives, however, need higher processing temperature, which could easily cause larger residue stress and strain in the power module. For encapsulant, it has not only thermal stability but also dielectric breakdown strength issues in the SiC power modules.

With the same breakdown voltage, commercially available SiC MOSFET bare die has smaller chip area and thinner thickness compared with Si counterparts, and thus, package materials in a SiC power module will sustain higher electric field strength than that in a Si power module [18].

Besides, SiC power modules are often used in harsh environments. Under high ambient temperature and operational temperature, CTE mismatch among the package materials could induce excessive warpage, stress, and strain, leading to SiC die crack, interface delamination, and so on.

Therefore, package materials with high-temperature stability, high dielectric strength, and CTE matching with SiC should be selected for SiC power module.

D. Packaging Process

In pursuit of low parasitic inductances and high-efficiency cooling of SiC power module, novel wirebondless packages or topology structures are proposed. However, developing novel packaging techniques will face some process challenges. New failure mode could occur during the packaging process.

At present, commercially available SiC power devices are designed for Al wirebonding. The front-side pads metallization of these devices are Al, which is not compatible with wirebondless packaging techniques and an additional metallization layer is required on the front-side source and gate pads [36], [49]. Therefore, the remetallization of Al pad on the power devices is a key process for the development of wirebondless packages. Wafer- or chip-level sputtering process is usually performed to deposit a layer or multilayer metallization layer on the original Al pads using physical vapor deposition (PVD) equipment. However, for SiC power MOSFET, the cost and risk of pad remetallization at wafer level are very high. It is difficult to realize the pad remetallization at chip level due to a relatively small die size. Besides, sputtering condition must be well controlled; otherwise, pad remetallization quality is not well, and it could result in worse interconnection between the pads and outer layers and lead to the final failure. Therefore, remetallization of Al pad on the SiC devices is a challenge.

Bonding process is also a challenge. In order to improve the thermal dissipation performance of SiC power module, soldering or sintering material is usually adopted. However, their bonding conditions are difficult to control, especially for multidie bonding. If not well controlled, many voids at the interface could be generated, leading to poor thermal dissipation performance.

Furthermore, some special package structures are designed, it is difficult to achieve through conventional packaging processes. Some new packaging process and equipments are needed, which increases the cost of the package.

Besides, some new package materials may be used, which indicates that new process condition needs to be explored and thus increases the cost of the package. Interface delamination or stress concentration could occur due to CTE mismatch between the new materials and the others.

Therefore, new package development will face many new process challenges.

E. Module Characterization

In general, measurement instrument is developed and equipped with some fixtures for conventional discrete devices, e.g., TO247 and TO220 packages. However, once a novel power module package is developed, in order to thoroughly characterize the performance of the module, custom clamps must be designed and fabricated. How to design clamps and accurately evaluate the performance via custom clamps are also challenges for the characterization of new power module package.

VI. Conclusion

In order to address parasitic inductances, heat dissipation, and reliability issues that are inherent with Al wires used in a conventional packaging scheme, many power module packaging schemes with low parasitic inductance and high-efficiency cooling, e.g., planar packaging, 3-D packaging, and PCB embedded packaging, have been developed. As a potential semiconductor material in high operating temperature, high blocking voltage, and high switching frequency applications, SiC material properties and SiC device potentials are introduced in this article. In order to comprehensively investigate the packaging techniques for power module, prior to review of packaging techniques for SiC power module, review of packaging schemes for Si-based power modules, which are representative and widely used power devices, is first performed. These packaging schemes are the foundation of packaging schemes of SiC power module. Then, low inductive and high-efficiency cooling interconnection technologies for SiC power module are thoroughly overviewed. Although some similar packaging schemes for Si-based power module have also been explored, requirements of parasitic inductance and heat dissipation for SiC power module package are demanding. Finally, the challenges of packaging techniques for SiC power module are summarized. With the advent of new SiC devices, the features of SiC MOSFETs pose substantial challenges to packaging of SiC power module, e.g., fast switching speed and heat dissipation. The development of novel packaging technique needs to overcome new challenges, e.g., material selection and packaging process. Once a new package is developed, module characterization is also a challenge. These issues must be addressed more carefully in the SiC MOSFET power module packaging design.

References

[1] J. Fabre, P. Ladoux, and M. Piton, "Characterization and implementation of dual-SiC MOSFET modules for future use in traction converters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4079–4090, Aug. 2015.

[2] J. Fabre and P. Ladoux, "Parallel connection of 1200-V/100-A SiC-MOSFET half-bridge modules," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 1669–1676, Mar./Apr. 2016.

[3] J. Hornberger, A. B. Lostetter, K. J. Olejniczak, T. McNutt, S. M. Lal, and A. Mantooth, "Silicon-carbide (SiC) semiconductor power electronics for extreme high-temperature environments," in *Proc. IEEE Aerosp. Conf.*, Big Sky, MT, USA, vol. 4, Mar. 2004, pp. 2538–2555.

[4] R. Khazaka, L. Mendizabal, D. Henry, and R. Hanna, "Survey of high-temperature reliability of power electronics packaging components," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2456–2464, May 2015.

[5] C. Chen, Z. Huang, L. Chen, Y. Tan, Y. Kang, and F. Luo, "Flexible PCB-based 3-D integrated SiC half-bridge power module with three-sided cooling using ultralow inductive hybrid packaging structure," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5579–5593, Jun. 2019.

[6] B. Mouawad *et al.*, "Direct copper bonding for power interconnects: Design, manufacturing and test," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 5, no. 1, pp. 143–150, Jan. 2015.

[7] B. Mouawad *et al.*, "Application of the spark plasma sintering technique to low-temperature copper bonding," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 2, no. 4, pp. 553–560, Apr. 2012.

[8] A. Hamidi and D. Cottet, "Parasitics in power electronics packaging," in *Proc. Int. Symp. Microelectron., (IMAPS)*. Long Beach, CA, USA, Nov. 2004, pp. 1–6.

[9] W. Zhang *et al.*, "A new package of high-voltage cascode gallium nitride device for megahertz operation," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1344–1353, Feb. 2015.

[10] J. W. Palmour *et al.*, "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," in *Proc. IEEE Int. Symp. Power Semiconductor Device IC's (ISPSD)*, Waikoloa, HI, USA, Jun. 2014, pp. 79–82.

[11] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, "Performance evaluation of high-power SiC MOSFET modules in comparison to Si IGBT modules," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181–1196, Feb. 2019.

[12] O. Sivkov and M. Novak, "Implementation of SiC inverter for high frequency, medium voltage applications," in *Proc. Int. Conf. Mechatronics Mechatronika*, Brno, Czech Republic, Dec. 2014, pp. 477–483.

[13] M. Mudholkar, S. Ahmed, M. N. Ericson, S. S. Frank, C. L. Britton, and H. A. Mantooth, "Datasheet driven silicon carbide power MOSFET model," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2220–2228, May 2014.

[14] A. R. Hefner, R. Singh, J.-S. Lai, D. W. Berning, S. Bouche, and C. Chapuy, "SiC power diodes provide breakthrough performance for a wide range of applications," *IEEE Trans. Power Electron.*, vol. 16, no. 2, pp. 273–280, Mar. 2001.

[15] B.J. Baliga, *Advanced Power MOSFET Concepts*, Boston, MA, USA: Springer, 2010.

[16] T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and S. H. Ryu, "Silicon carbide power MOSFET model and parameter extraction sequence," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 353–363, Mar. 2007.

[17] S. Hazra, S. Madhusoodhanan, G. Karimi Moghaddam, K. Hatua, and S. Bhattacharya, "Design considerations and performance evaluation of 1200-V 100-A SiC MOSFET-based two-level voltage source converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4257–4268, Sep./Oct. 2016.

[18] C. Chen, F. Luo, and Y. Kang, "A review of SiC power module packaging: Layout, material system and integration," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 170–186, Sep. 2017.

[19] CREE. *Application Considerations for Silicon Carbide MOSFETs*. Accessed: Jan. 2011. [Online]. Available: https://www.wolfspeed.com

[20] J. A. del Alamo and J. Joh, "GaN HEMT reliability," *Microelectron. Rel.*, vol. 49, no. 9, pp. 1200–1206, Sep. 2009.

[21] K. Weidner, M. Kaspar, and N. Seliger, "Planar interconnect technology for power module system integration," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst. (CIPS)*, Nuremberg, Germany, Mar. 2012, pp. 1–5.

[22] T. Ueda, N. Yoshimatsu, N. Kimoto, D. Nakajima, M. Kikuchi, and T. Shinohara, "Simple, compact, robust and high-performance power module T-PM (transfer-molded power module)," in *Proc. IEEE Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, Hiroshima, Japan, Jun. 2010, pp. 47–50.

[23] Z. X. Liang, P. Q. Ning, F. Wang, and L. Marlino, "A phase-leg power module packaged with optimized planar interconnections and integrated double-sided cooling," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 443–450, Sep. 2014.

[24] H.-R. Chang, J. Bu, G. Kong, and R. Labayen, "300A 650V 70 um thin IGBTs with double-sided cooling," in *Proc. IEEE 23rd Int. Symp. Power Semiconductor Devices ICs*, San Diego, CA, USA, May 2011, pp. 320–323.

[25] Q. Zhu, A. Forsyth, R. Todd, and L. Mills, "Thermal characterisation of a copper-clip-bonded IGBT module with double-sided cooling," in *Proc. IEEE Int. Workshop Therm. Investigations ICs Syst. (THERMINIC)*, Amsterdam, The Netherlands, Sep. 2017, pp. 1–6.

[26] C. L. Han, "Design and development of planar double-sided cooling IGBT module," Ph.D. dissertation, Dept. Inst. Elect. Eng., Univ. Chin. Acad. Sci., Beijing, China, 2015.

[27] Y. Wang *et al.*, "Mitigation of challenges in automotive power module packaging by dual sided cooling," in *Proc. 18th Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Karlsruhe, Germany, Sep. 2016, pp. 1–8.

[28] Y. Zhang, T. Hammam, I. Belov, T. Sjögren, M. Bakowski, and H.-P. Nee, "Thermomechanical analysis and characterization of a Press-pack structure for SiC power module packaging applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 7, pp. 1089–1100, Jul. 2017.

[29] IXYS. *Press-Pack IGBT, Towards the Next Generation of Super Switch*. Accessed: Jun. 24, 2014. [Online]. Available: https://fhi.nl/app/uploads/sites/38/2014/01/KWx-IXYS-UK-IGBT-june14.pdf

[30] R. Simpson, A. Plumpton, M. Varley, C. Tonner, P. Taylor, and X. Dai, "Press-pack IGBTs for HVDC and FACTs," *CSEE J. Power Energy Syst.*, vol. 3, no. 3, pp. 302–310, Sep. 2017.

[31] Z. Liang, J. D. V. Wyk, and F. C. Lee, "Embedded power: A 3-D MCM integration technology for IPEM packaging application," *IEEE Trans. Adv. Packag.*, vol. 29, no. 3, pp. 504–512, Aug. 2006.

[32] A. Ostmann *et al.*, "Integration of passive and active components into build-up layers," in *Proc. IEEE Electron. Packag. Technol. Conf.*, Singapore, Dec. 2002, pp. 223–228.

[33] R. Aschenbrenner, "System-in-package solutions with embedded active and passive components," in *Proc. Int. Conf. Electron. Packag. Technol. High Density Packag.*, Shanghai, China, Jul. 2008, pp. 1–2.

[34] L. Boettcher, D. Manessis, A. Ostmann, S. Karaszkiewicz, and H. Reichl, "Embedding of chips for system in package realization—Technology and applications," in *Proc. 3rd Int. Microsyst., Packag., Assemb. Circuits Technol. Conf.*, Taipei, Taiwan, Oct. 2008, pp. 383–386.

[35] A. Ostmann, L. Boettcher, D. Manessis, S. Karaszkiewicz, and K.-D. Lang, "Power modules with embedded components," in *Proc. Eur. Microelectron. Packag. Conf. (EMPC)*, Grenoble, France, Jan. 2013, pp. 1–4.

[36] L. Boettcher, S. Karaszkiewicz, D. Manessis, and A. Ostmann, "Development of embedded power electronics modules," in *Proc. 4th Electron. Syst.-Integr. Technol. Conf.*, Amsterdam, The Netherlands, Sep. 2012, pp. 1–6.

[37] Y. Pascal, A. Abdedaim, D. Labrousse, M. Petit, S. Lefebvre, and F. Costa, "Using laminated metal foam as the top-side contact of a PCB-embedded power die," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1453–1456, Oct. 2017.

[38] A. Munding, A. Kessler, T. Scharf, B. Plikat, and K. Pressel, "Laminate chip embedding technology—Impact of material choice and processing for very thin die packaging," in *Proc. IEEE 67th Electron. Compon. Technol. Conf. (ECTC)*, Orlando, FL, USA, Jun. 2017, pp. 711–718.

[39] D. J. Kearney, S. Kicin, E. Bianda, and A. Krivda, "PCB embedded semiconductors for low-voltage power electronic applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 3, pp. 387–395, Mar. 2017.

[40] T.-C. Chang, C.-C. Lee, C.-P. Hsieh, S.-C. Hung, and R.-S. Cheng, "Electrical characteristics and reliability performance of IGBT power device packaging by chip embedding technology," *Microelectron. Rel.*, vol. 55, pp. 2582–2588, Dec. 2015.

[41] E. Parker, B. Narveson, A. Alderman, and L. Burgyan, "Embedding active and passive components in PCBs and inorganic substrates for power electronics," in *Proc. IEEE Int. Workshop Integr. Power Packag.*, Chicago, IL, USA, May 2015, pp. 107–110.

[42] R. Reiner *et al.*, "PCB-embedding for GaN-on-Si power devices and ICs," in *Proc. 10th Int. Conf. Integr. Power Electron. Syst.*, Stuttgart, Germany, Mar. 2018, pp. 1–6.

[43] GaN System. *A Basis for Extremely Small GaN Power Transistors*. Accessed: Nov. 22, 2016. [Online]. Available: https://gansystems.com/newsroom/article/basis-extremely-small-gan-power-transistors/

[44] J.-L. Marchesini, P.-O. Jeannin, Y. Avenas, J. Delaine, C. Buttay, and R. Riva, "Implementation and switching behavior of a PCB-DBC IGBT module based on the power chip-on-chip 3-D concept," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 362–370, Jan./Feb. 2017.

[45] F. Hou *et al.*, "High power-density 3D integrated power supply module based on panel-level PCB embedded technology," in *Proc. IEEE Electron Comp. Technol. Conf.*, San Diego, CA, USA, Jun. 2018, pp. 1365–1370.
[46] K. Vladimirova *et al.*, "Solderless leadframe assisted wafer-level packaging technology for power electronics," in *Proc. IEEE IEEE Electron Comp. Technol. Conf.*, San Diego, CA, USA, Aug. 2018, pp. 1251–1257.
[47] L. Ménager, M. Soueidan, B. Allard, V. Bley, and B. Schlegel, "A lab-scale alternative interconnection solution of semiconductor dice compatible with power modules 3-D integration," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1667–1670, Jul. 2010.
[48] S. Li, L. M. Tolbert, F. Wang, and F. Z. Peng, "Stray inductance reduction of commutation loop in the P-cell and N-cell-based IGBT phase leg module," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3616–3624, Jul. 2014.
[49] D. R. M. Woo, H. H. Yuan, J. A. J. Li, L. J. Bum, and Z. Hengyun, "Miniaturized double side cooling packaging for high power 3 phase SiC inverter module with junction temperature over 220°C," in *Proc. IEEE 66th Electron. Compon. Technol. Conf. (ECTC)*, Las Vegas, NV, USA, Jun. 2016, pp. 1190–1196.
[50] L. Stevanovic, "Packaging challenges and solutions for silicon carbide power electronics," presented at the ECTC Panel Session: Power Electron.—A Booming Market, 2012.
[51] L. Yin, C. Kapusta, A. Gowda, and K. Nagarkar, "A wire-bondless packaging platform for silicon carbide power semiconductor devices," *J. Electron. Packag.*, vol. 140, no. 3, Sep. 2018, Art. no. 031009.
[52] H. Zhang, S. S. Ang, H. A. Mantooth, and S. Krishnamurthy, "A high temperature, double-sided cooling SiC power electronics module," in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, Sep. 2013, pp. 2877–2883.
[53] H. Ishino, T. Watanabe, K. Sugiura, and K. Tsuruta, "6-in-1 Silicon carbide power module for high performance of power electronics systems," in *Proc. IEEE Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Waikoloa, HI, USA, Jun. 2014, pp. 446–449.
[54] Y. Xu, I. Husain, H. West, W. Yu, and D. Hopkins, "Development of an ultra-high density power chip on bus (PCoB) module," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Milwaukee, WI, USA, Sep. 2016, pp. 1–7.
[55] N. Zhu, H. A. Mantooth, D. Xu, M. Chen, and M. D. Glover, "A solution to press-pack packaging of SiC MOSFETS," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8224–8234, Oct. 2017.
[56] S. Seal, M. D. Glover, A. K. Wallace, and H. A. Mantooth, "Flip-chip bonded silicon carbide MOSFETs as a low parasitic alternative to wire-bonding," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl., (WiPDA)* Fayetteville, AR, USA, Nov. 2016, pp. 194–199.
[57] S. Seal, A. K. Wallace, J. Zumbro, and H. A. Mantooth, "Thermo-mechanical reliability analysis of flip-chip bonded silicon carbide Schottky diodes," in *Proc. IEEE Int. Workshop Integrated Power Packaging (IWIPP)*, Delft, The Netherlands, Apr. 2017, pp. 1–5.
[58] H. A. Mantooth and S. S. Ang, "Packaging architectures for silicon carbide power electronic modules," in *Proc. Int. Power Electron. Conf.*, Niigata, Japan, May 2018, pp. 153–156.
[59] S. Seal, M. D. Glover, and H. A. Mantooth, "3-D wire bondless switching cell using flip-chip-bonded silicon carbide power devices," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8553–8564, Oct. 2018.
[60] M. Horio, Y. Iizuka, and Y. Ikeda, "Packaging technologies for SiC power modules," *Fuji Electr. Rev.*, vol. 58, no. 2, pp. 75–78, 2012.
[61] Y. Ikeda, Y. Iizuka, Y. Hinata, M. Horio, M. Hori, and Y. Takahashi, "Investigation on wirebond-less power module structure with high-density packaging and high reliability," in *Proc. IEEE 23rd Int. Symp. Power Semiconductor Devices ICs*, San Diego, CA, USA, May 2011, pp. 272–275.
[62] T. Stockmeier, P. Beckedahl, C. Göbl, and T. Malzer, "SKiN: Double side sintering technology for new packages," in *Proc. IEEE 23rd Int. Symp. Power Semiconductor Devices ICs*, San Diego, CA, USA, May 2011, pp. 324–327.
[63] P. Beckedahl, S. Buetow, A. Maul, M. Roeblitz, and M. Spang, "400 A, 1200 V SiC power module with 1nH commutation inductance," in *Proc. 9th Int. Conf. Integr. Power Electron. Syst. CIPS*, Nuremberg, Germany, Mar. 2016, pp. 1–6.
[64] Z. Chen, Y. Yao, D. Boroyevich, K. Ngo, and W. Zhang, "An ultra-fast SiC phase-leg module in modified hybrid packaging structure," in *Proc. IEEE Energy Convers. Congr. Expo.*, Pittsburgh, PA, USA, Sep. 2014, pp. 2880–2886.
[65] Z. Huang *et al.*, "A novel low inductive 3D SiC power module based on hybrid packaging and integration method," in *Proc. IEEE Energy Convers. Congr. Expo.*, Cincinnati, OH, USA, Oct. 2017, pp. 3995–4002.
[66] S. Toyoshima, S. Hatsukawa, N. Hirakata, T. Tsuno, and Y. Mikamura, "Compact SiC power module for high speed switching," SEI Investments Company, Oaks, PA, USA, Tech. Rev ., 2015, no. 80, pp. 81–84.
[67] A. Anthon, Z. Zhang, and M. A. E. Andersen, "Comparison of a state of the art Si IGBT and next generation fast switching devices in a 4 kW boost converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Montreal, QC, Canada, Sep. 2015, pp. 3003–3011.
[68] L. Wu, L. Xiao, J. Zhao, and G. Chen, "Physical analysis and modeling of the nonlinear miller capacitance for SiC MOSFET," in *Proc. 43rd Ann. Conf. IEEE Ind. Electron. Soc.*, Beijing, China, Nov. 2017, pp. 1411–1416.
[69] T. Wu, "CDV/DT induced turn-on in synchronous buck regulators," Int. Rectifier, Tech. Rep., 2007.
[70] H. Zaman, X. Wu, X. Zheng, S. Khan, and H. Ali, "Suppression of switching crosstalk and voltage oscillations in a SiC MOSFET based half-bridge converter," *Energies*, vol. 11, no. 11, p. 3111, Nov. 2018.
[71] ABB. *IGBT-Die 5SMY 12K1280*. [Online]. Available: https://new.abb.com/semiconductors/insulated-gate-bipolar-transistors-(igbt)-and-diode-dies
[72] CREE. *CPM2-1200-0025B, Rev. C*. Accessed: Jan. 2016. [Online]. Available: https://www.wolfspeed.com/power/products/sic-mosfets/cpm2-1200-0025b
[73] S. Yin, P. Tu. P. Wang, K. J. Tseng, C. Qi, X. Hu, M. Zagrodnik, and R. Simanjorang, "An accurate subcircuit model of SiC half-bridge module for switching-loss optimization," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 3840–3848, Jul./Aug. 2017.
[74] Y. Ren *et al.*, "Voltage suppression in wire-bond-based multichip phase-leg SiC MOSFET module using adjacent decoupling concept," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8235–8246, Oct. 2017.
[75] H. Kono, K. Takao, T. Suzuki, and T. Shinohe, "High-speed and low switching loss operation of 1700 V 60 A SiC MOSFETs installed in low parasitic inductance module," in *Proc. IEEE Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Waikoloa, HI, USA, Jun. 2014, pp. 289–292.
[76] K. Takao, T. Shinohe, T. Yamamoto, K. Hasegawa, and M. Ishida, "1200 V-360 A SiC power module with phase leg clustering concept for low parasitic inductance and high speed switch," in *Proc. Int. Conf. Integr. Power Electron. Syst.*, Nuremberg, Germany, Feb. 2014, pp. 1–7.
[77] K. Takao and S. Kyogoku, "Ultra low inductance power module for fast switching SiC power devices," in *Proc. IEEE Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Hong Kong, May 2015, pp. 313–316.
[78] Q. Yan, X. Yuan, Y. Geng, A. Charalambous, and X. Wu, "Performance evaluation of split output converters with SiC MOSFETs and SiC Schottky diodes," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 406–422, Jan. 2017.
[79] M. R. Ahmed, G. Calderon-Lopez, F. Bryan, R. Todd, and A. J. Forsyth, "Soft-switching SiC interleaved boost converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Charlotte, NC, USA, Mar. 2015, pp. 941–947.
[80] J. Wang, H. S. H. Chung, and R. T. H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.
[81] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si—Evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC Power Semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011.

Fengze Hou is currently pursuing the Ph.D. degree with the Department of Microelectronics, Delft University of Technology, Delft, The Netherlands.

Since July 2012, he has been an Assistant Researcher with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China. He is also a Senior Engineer with the National Center for Advanced Packaging, Wuxi, China. His current interests include thermal management, reliability, system integration, and SiC power module packaging.

Wenbo Wang received the B.Sc. degree in electrical engineering and automation and the M.Sc. degree in power electronics and electrical drives from Northwestern Polytechnical University, Xi'an, China, in 2008 and 2010, respectively, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2017.

He is currently with the Shenzhen Institute of Wide Bandgap Semiconductors (Wins), Shenzhen, China. His current research interests include wide-bandgap semiconductors, high-frequency magnetics, and high-frequency power converters.

Liqiang Cao received the B.Sc. degree from the University of Science and Technology of China, Hefei, China, and the M.Sc. and Ph.D. degrees from the Chalmers University of Technology, Gothenburg, Sweden.

From 2000 to 2005, he was with IVF—The Swedish Institute of Production Engineering Research and the Sino-Swedish Microsystem Integration Technology (SMIT) Center, Sweden, as a Research Fellow. He joined Intel in October 2005 as a Senior Scientist and a Program Manager. Since February 2009, he has been a Professor with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China. He is currently the General Manager of the National Center for Advanced Packaging, Wuxi, China. His research interests focus on the manufacturing process for system-in-package and FEM modeling for advanced packaging.

Jun Li received the B.Sc. degree in electronics science and technology and the Ph.D. degree in electromagnetic field and microwave technology from Southwest Jiaotong University, Chengdu, China, in 2004 and 2010, respectively.

From 2010 to August 2012, she completed her post-doctoral research at the Institute of Microelectronics, Chinese Academy of Sciences (IMECAS), Beijing, China, where she was an Assistant Researcher from August 2012 to 2014 and has been an Associate Professor since 2014. She is currently the Associate Director of the System Packaging and Integration Research Center, IMECAS. Her interests include the design and simulation of system-in-package, simulation methods of advanced packaging, DFx codesign, signal integrity, power integrity, IPD design, thermal management of advanced packaging, and high-power cooling technology.

Meiying Su received the Ph.D. degree in circuits and systems from the Dalian University of Technology, Dalian, China.

In 2012, she was an Assistant Researcher with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, where she has been an Associate Professor since 2015. Her interests include thermal management and thermomechanical reliability analysis of 2.5-D/3-D packaging and fan-out packaging.

Tingyu Lin received the Ph.D. degree in microelectronics from the National University of Singapore (NUS), Singapore, in 1997.

He has more than 20-year experiences in design, process, assembly, reliability, and equipment development in electronics packaging. He was a Motorola (Google) certified Six Sigma Black Belt in 2012. Since 2013, he has been the Technical Director of the National Center for Advanced Packaging (NCAP), Wuxi, China. Until now, he has been engaged in more than 100 product design and process development in mobile module, IC component, and consumer electronics. He has published 150 articles and filed more than 80 patents.

Dr. Lin received many excellent paper awards and gave keynote talks in several conferences. He led two international ASTM sputtering material standards (F3166/F3192) for TSV development and received the Motorola Innovation Award in 2008.

Guoqi Zhang (M'03–F'14) received the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 1993.

He was with NXP Semiconductors, Eindhoven, The Netherlands, as the Senior Director of Technology Strategy, until 2009, and was a Philips Research Fellow until May 2013. He is currently a Chair Professor of micro/nanoelectronics system integration and reliability with the Delft University of Technology. He has authored/coauthored more than 400 scientific publications. His research interest covers multilevel heterogeneous system integration and packaging, wide-bandgap semiconductors sensors and components, multiphysics and multiscale modeling of micro/nanoelectronics, and digital twin for mission critical multifunctional electronics components and systems.

Dr. Zhang serves as the Deputy Director of the European Center for Micro- and Nanoreliability (EUCEMAN), the Co-Chair of the Advisory Board of International Solid-State Lighting Alliance (ISA), and the Secretary General of the International Technology Roadmap of Wide Bandgap Semiconductors (ITRW).

Braham Ferreira (M'88–SM'01–F'05) received the Ph.D. degree in electrical engineering from Rand Afrikaans University, Johannesburg, South Africa.

In 1981, he was with the Institute of Power Electronics and Electric Drives, Technical University of Aachen, Aachen, Germany. He was a System Engineer with ESD Pty (Ltd.) from 1982 to 1985. From 1986 to 1997, he was with the Department of Electrical Engineering, Rand Afrikaans University, where he held the Carl and Emily Fuchs Chair of power electronics in later years. From 1998 to 2018, he held the Chair of power electronics and electrical machines with the Delft University of Technology, Delft, The Netherlands, where he served as the Head of the department from 2006 to 2010 and was the Director of the Delft-Beijing Institute of Intelligent Science and Technology from 2017 to 2018. He is currently a Professor of power electronics with the University of Twente, Enschede, The Netherlands. He has authored or coauthored 100 journal and transactions articles and 300 conference articles. He holds 15 patents.

Dr. Ferreira received 15 prize paper awards. He was a recipient of the IEEE IAS Gerald Kliman Innovator Award and the IAS Outstanding Achievement Award. He is the Chair of the IEEE International Technology Roadmap of Wide Bandgap Semiconductors (ITRW). He served as the President of the IEEE Power Electronics Society from 2015 to 2016.