RF Capacitance-Voltage Characterization of MOSFETs with high leakage dielectrics

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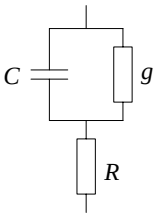
***Abstract*— We present a MOS Capacitance-Voltage measurement methodology that, contrary to present methods, is highly robust against gate leakage current densities up to 1000 A/cm^2. The methodology features specially designed RF test structures and RF measurement frequencies. It allows MOS parameter extraction in the full range of accumulation, depletion and inversion.**

***Index Terms*—MOSFETs, MOS capacitors, capacitance, capacitance measurement, RF, leakage currents, tunneling**

I. Introduction

As CMOS device dimensions are scaled below 100 nm, the concurrent gate dielectric thinning leads to progressively higher gate leakage currents. Tunnel current densities around 100 A/cm^2 are foreseen for the near future in some CMOS logic applications [1]. Although this may be acceptable from a functional point of view, such leakage currents complicate fundamental MOS characterization techniques like charge pumping [2], time-dependent dielectric breakdown tests [3] and capacitance-voltage (*C-V*) measurements [4-8]. Gate leakage affects the measurement of the capacitance-voltage characteristic as well as its interpretation. This can be understood conceptually by considering a simple three-element equivalent circuit for the leaky MOS capacitor as sketched in Fig. 1. The capacitance C is connected in parallel to a (strongly bias-dependent) differential conductance $g \equiv \mathrm{d}I/\mathrm{d}V$ arising from gate current. An external resistance R, originating e.g. from gate resistance, is also inevitable. The equations (1)–(4) in Fig. 1 give the analytic expressions for the impedance Z, the quality factor Q, and the optimum measurement frequency f_{opt} at which the quality factor reaches its maximum value Q_{opt}. Measurement at f_{opt} will lead to the most accurate value for C. A capacitance measurement is only straightforward when the capacitance is large enough (typically at least 1 pF), and when the quality factor is larger than 10. In case of a quality factor below unity, it is hardly possible to obtain a good estimate of the capacitance.



$$Z = \frac{1}{j\omega C + g} + R \tag{1}$$

$$Q \equiv -\frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} = \frac{\omega C}{g + R(\omega^2 C^2 + g^2)} \tag{2}$$

$$f_{\mathrm{opt}} = \frac{1}{2\pi RC}\sqrt{gR(1+gR)} \tag{3}$$

$$Q_{\mathrm{opt}} = \frac{1}{2\sqrt{gR(1+gR)}} \tag{4}$$

Fig. 1. Three-element equivalent circuit approximation of a leaky MOS capacitor, with equations for its impedance Z, the related quality factor $Q(\omega)$, and the maximum achievable quality factor Q_{opt}, found at frequency f_{opt}.

To obtain $Q_{\mathrm{opt}} \gg 1$, it follows from (4) that R should satisfy

$$gR \ll \frac{\sqrt{2}-1}{2} \approx 0.2 \tag{5}$$

This equation shows that the higher the gate leakage (and hence g), the lower the external resistance R must be. This can be achieved by a careful design of the test structure: abundant, nearby well contacts and a small gate area. (For a sufficiently high total capacitance, several devices *with separate well contacts* can be connected in parallel, as in [9].) The *minimum* frequency for $Q \geq 1$ can then be expressed as

$$f_{\mathrm{min}} = \frac{1-\sqrt{1-4gR(1+gR)}}{4\pi RC} \approx \frac{g}{2\pi C} \tag{6}$$

For a 10×10 μm^2 MOS capacitor with 10 A/cm^2 gate leakage, typical values are C = 2 pF, $g \approx 50\times10^{-6}\ \Omega^{-1}$, and R = 10–100 Ω leading to f_{min} = 4 MHz.

Note that f_{min} is independent of gate area and external resistance. Therefore it cannot be reduced by design improvements. As a direct consequence, high leakage dielectrics demand high measurement frequencies, driving us into the gigahertz range.

II. Device fabrication and characterization

The experimental study of *C-V* measurements at gigahertz frequencies (RF-CV measurements) is carried out using transistors designed for two-port RF measurements in ground-signal-ground configuration. They consist of many gates connected in parallel, with a layout resulting in very low gate resistance and low well resistance (see e.g. [9]). Sub-micron channel lengths are used to achieve a low channel resistance.

Devices were fabricated in a standard 6-metal 0.12 μm CMOS flow, and in a single-metal 0.18 μm CMOS research process. S-parameter measurements in the range 0.1–48 GHz were carried out on-wafer using a HP 8510C network analyzer. The gate was connected to Port 1, drain connected to Port 2. The gate was biased, the other terminals grounded. The measurements were accompanied by SOLT calibration and open-short de-embedding [10].

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III. Validation of RF-CV measurements

Capacitance-voltage measurements between 0.5 and 10 GHz are shown in Fig. 2 (left). Here, $C_{\rm gg} \equiv {\rm Im}(Y_{11})/\omega$, which is only a good approximation of the MOS capacitance C when the external resistance R is negligible. At the lowest frequencies, the

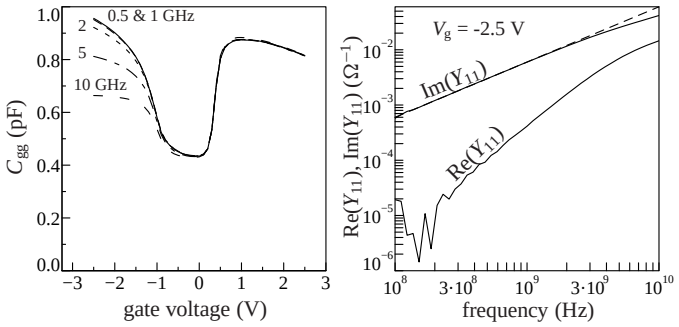


Fig. 2. Left: capacitance-voltage curve of a W/L = 384 μm/0.18 μm NMOS RF transistor as measured at various frequencies, after de-embedding. Right: real and imaginary parts of Y_{11} as a function of frequency at $V_{\rm g}$ = -2.5 V. The dashed line shows the trend of a capacitor without series resistance.

shape of the curve is as expected, with the accumulation behavior of an ultra-thin dielectric and inversion capacitance decreasing due to gate depletion. The depletion region around $V_{\rm g}$ = 0 V shows only a moderate decrease in capacitance because this is a sub-micron channel device with significant gate-drain overlap capacitance.

At frequencies above 1 GHz, we observe a drop in the capacitance at accumulation bias. It is accompanied by a downward bend of the real part of Y_{11}: see Fig. 2 (right). This is not due to a drop in the MOS capacitance, but rather the signature of a significant external series resistance. The origin is the well resistance $R_{\rm well}$, which results in a limited response time of bulk holes; see Fig. 3. In this figure, we have explicitly separated

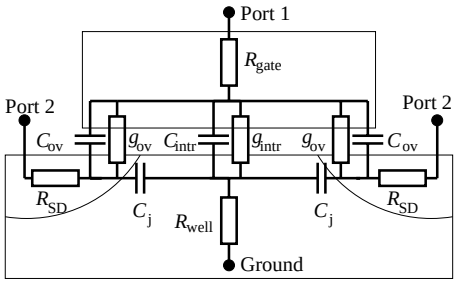


Fig. 3. Cross section of a capacitor (or transistor), with an approximated equivalent circuit in accumulation. All components in this diagram are bias dependent except $R_{\rm gate}$, $R_{\rm SD}$ and $R_{\rm well}$.

the overlap regions, with capacitance $C_{\rm ov}$ and conductance $g_{\rm ov}$, from the intrinsic or "channel" region with capacitance $C_{\rm intr}$ and conductance $g_{\rm intr}$. In accumulation and depletion, charging and discharging of $C_{\rm intr}$ requires holes to move from the "channel" region to the ground connection through $R_{\rm well}$. This transport is limited by the characteristic delay time $\tau = R_{\rm well}C_{\rm intr}$, which implies that the measurement frequency f is restricted to

$$f \ll \frac{1}{2\pi R_{\rm well} C_{\rm intr}} \qquad (7)$$

For the transistor under study, $\tau \approx 20$ ps. As a result the depletion and accumulation capacitances of $C_{\rm intr}$ are attenuated at frequencies above 1 GHz. Therefore, in this paper we present further analysis of data obtained at 1 GHz.

To find the intrinsic capacitance $C_{\rm intr}$ we measured the Y-parameters of two devices with equal design except for the gate lengths, being 130 and 180 nm. From the difference of the obtained $C_{\rm gg}$ curves, we can establish the $C_{\rm intr}$ of a 50 nm channel segment. The capacitance of this segment is shown in Fig. 4. A *C-V* model can now be fitted to these data to ob-

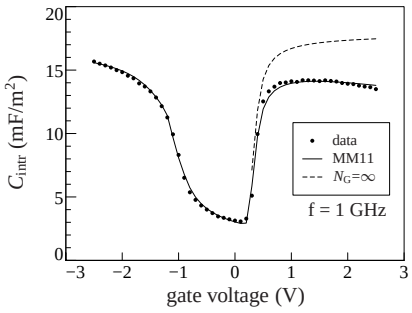


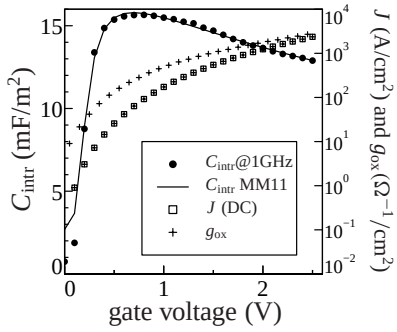
Fig. 4. Area-normalized capacitance of a 50 nm wide channel segment as computed from the difference of a 130 nm and a 180 nm gate length RF transistor. A fit of MOS Model 11 (MM11) to the data is also shown (see text). The dashed line symbolizes the (modeled) inversion capacitance in case of infinitely high gate doping.

tain the required MOS parameters. As an example we fitted MOS Model 11 [11] over the full curve, also shown in the figure. Fit values were: -1.07 V flatband voltage, 1.9 nm oxide thickness, 2.6×10^{20} cm^{-3} gate doping, and 1.7×10^{18} cm^{-3} substrate doping (using no other fit parameters). These values are as expected for this 0.12 μm CMOS process.

IV. RF-CV and gate leakage

The RF-CV measurement method can cope with a large gate leakage current. We fabricated RF transistors with high-leakage dielectrics in a research process flow (based on 0.18 μm CMOS) using a different design of RF structures. These devices have a considerably higher τ, preventing the correct measurement of accumulation and depletion capacitance in the channel. In inversion however, τ does not play a role while the gate leakage current is at its highest. The external resistance in inversion (being the sum of gate and source/drain resistance) is just below 1 Ω, which adequately solves the measurement problems discussed in e.g. [12]. Fig. 5 shows the measured inversion capacitance. $C_{\rm intr}$ was obtained from the capacitance difference between a 1 μm and a 0.2 μm gate length device. (For this approach to be valid, the threshold voltage difference between these devices must be limited.) The MOS Model 11 fit yields an oxide thickness and gate doping level independent of frequency in the range 0.2–2 GHz (see the table in Fig. 5) and fits poorly outside that region (due to a low quality factor).

Given the fact that power and functionality requirements restrict the gate leakage in CMOS circuits to typically < 1000 A/cm^2, the successful extraction of $C_{\rm intr}$ at gate currents exceeding this value shows that the presented methodology is well suited for the characterization of any dielectric that satisfies reasonable leakage specifications.



MM11 fit results		
f GHz	t_{ox} nm	N_G 10^{20}/cm^3
0.10	(1.24)	(0.80)
0.21	1.33	0.90
0.48	1.35	0.94
1.0	1.35	0.95
2.1	1.33	0.94
4.8	(1.42)	(1.15)

Fig. 5. Inversion capacitance and gate leakage current density of a high-leakage dielectric. The inversion capacitance is correctly measured even when the gate current density exceeds 1 kA/cm^2, as confirmed by the excellent fit with MOS Model 11. The fit values are listed in the table for various frequencies.

V. Conclusions

This paper presents the RF-CV methodology, which allows the measurement and analysis of capacitance-voltage curves even in the presence of gate leakage exceeding 1000 A/cm^2. On the basis of theoretical and experimental findings, design guidelines are formulated for RF capacitors. When these guidelines are followed, the appropriate Capacitance-Voltage characteristics are obtained around 1 GHz. These can be used for the extraction of MOS parameters such as (equivalent) oxide thickness, substrate doping concentration, and gate depletion. Since power and functionality requirements restrict the gate leakage in CMOS circuits to typically $<$ 1000 A/cm^2, the presented methodology is well suited for the characterization of *any* dielectric foreseen in future CMOS technologies.

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