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RF Characterization and Analytical Modelling of Through Silicon Vias and Coplanar Waveguides for 3D Integration

Yann P. R. Lamy, K. B. Jinesh, Fred Roozeboom, Dirk J. Gravesteijn, and Wim F. A. Besling

Abstract—High-aspect ratio (12.5) through silicon vias (TSV) made in a silicon interposer have been electrically characterized in the direct current (dc) and microwave regimes for 3D interconnect applications. The vias were micro-machined in silicon, insulated, and filled with copper employing a bottom-up copper electroplating technique in a “via-first” approach. DC via resistance measurements show good agreement with the theoretical expected value ($\sim 16 \text{ m}\Omega$). Radio-frequency (RF) measurements up to 50 GHz have been performed on coplanar waveguides located on the back-side of the wafers and connected to the front-side with TSVs. The *S*-parameters indicate clearly the beneficial impact of double sided ground planes of the RF signals. The via resistance extracted from impedance measurements is in good agreement with dc values, while the inductance (53 pH) and capacitance (2.4 pF) of the TSV are much lower than conventional wire bonding, which makes the use of TSV very promising for 3D integration. An advanced analytical model is proposed for the interconnect system with vias and lines and shows very good agreement with the experimental data with a limited number of fitting parameters. This work gives a proof of concept for high aspect ratio TSV manufacturing and new insights to improve 3D interconnect modeling for systems-in-package applications in the microwave regime.

Index Terms—Radio-frequency (RF) characterisation, RF modeling, Si interposer, three-dimensional interconnects, through silicon via, through-wafer interconnect, TSV, vias.

I. INTRODUCTION

THROUGH-SILICON-VIAs (TSVs) are of increasing interest for 3D integrated circuit technology as they appear to be attractive candidates to mitigate issues such as *RC* delay, thermal heating, and power consumption of conventional 2D integrated circuits (ICs). Moreover, TSVs enable heterogeneous integration into advanced system-in-package products which enable novel “More than Moore” applications. In the near future, several new multifunctional components [e.g., sensors and actuators, MEMS, passives for dc–dc converters, radio-frequency (RF)] should be combined in a compact packages [1], [2]. Lots of architectures have been proposed for these devices

[3], [4] but whatever the integration technique (i.e., via last, via first. . .) the electrical behavior of the 3D interconnect remains a key point as it has to transmit a wide range of different signals varying from analog to digital and RF. According to these requirements, it is mandatory to evaluate static TSV electrical behavior and as function of frequency. However, only a few papers in literature describe the RF electrical behavior of TSVs with front and back-side interconnects [5]–[8]. In addition, the RF data are not always linked to the dc behavior and other via properties. The RF characterization is either done on one-port reflective RF structures ([5], [6]), or on low aspect ratio (~ 5) vias ([7], [8]). In terms of modelling, the existing papers on TSV simulations are using complicated numerical techniques like finite element methods, with no clear links to the processing and the real measurements [7], [8]. This limits the use of the simulations significantly. In addition, the impact of grounding in coplanar lines coupled with TSVs has not been investigated in details so far.

In this work, we combine a fabrication method for high aspect ratio TSVs in a silicon interposer with in-depth dc and RF characterizations and modelling. The vias are filled with copper by means of copper electroplating in a “via-first”-like integration approach. The bottom-up plating approach ([5], [6]) has the main advantage to circumvent the lining/seeding limitation problems for high-aspect ratio vias because of the very poor step coverage standard deposition tool [9], [10]. The TSVs are coupled to standard coplanar waveguides (CPW) with different line lengths on the back-side of the wafer to allow in-depth RF analysis. This work demonstrates not only the realization of a silicon interposer but also allows realistic data extraction from RF measurements up to 50 GHz. From these results, an advanced electrical model for TSVs has been developed, which is very useful to interpret electrical data and to optimize layout and 3D integration for all kinds of system-in package applications in the microwave regime such as interconnecting active dies with passives and MEMS components [5], [11].

II. WAFER LAYOUT AND FABRICATION TECHNOLOGY

For complete electrical characterization, dc and RF device modules have been designed on the same die. The process flow is described in Fig. 1. Fabrication started from one-side polished 6-in wafers. We have chosen low resistivity ($\sim 0.01 \Omega\cdot\text{cm}$) wafers since very often a Si interposer has high doping levels for the devices. We mimic here a worse case scenario. The 20- μm -diameter vias were etched in a STS DRIE etcher with inductively coupled plasma, using a typical Bosch etch process to

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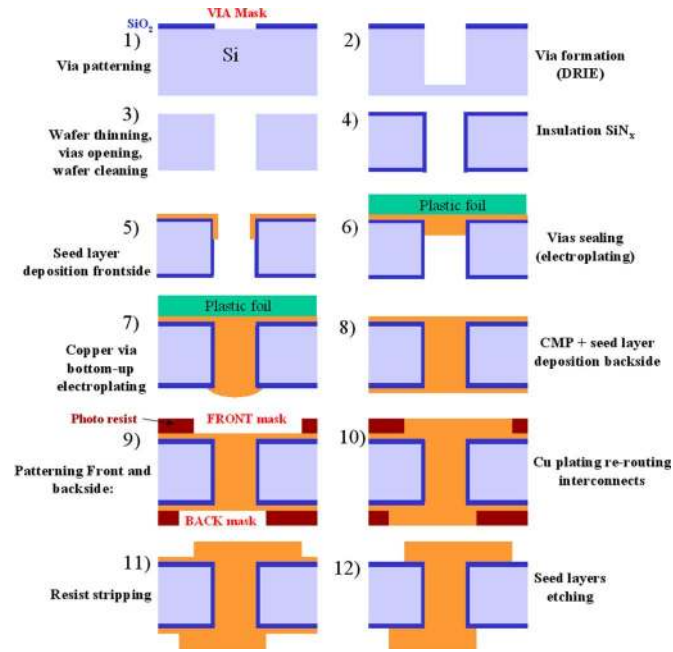


Fig. 1. Fabrication process flow for TSV interposer employing bottom-up electroplating.

achieve vertical sidewalls [2], [12]. A $2.5\text{-}\mu\text{m}$ PECVD SiO_2 layer was used as hard mask. The wafer thickness was thinned down to $250\ \mu\text{m}$, leading to vias with an aspect ratio (AR) of 12.5. The via insulation is formed with a $500\ \text{nm}$ SiN_x liner deposited with low pressure chemical vapor deposition to avoid Cu diffusion into the silicon. A 200-nm PVD Ti/Cu thin film has been deposited on the front-side as seed layer for the Cu sealing process. The bottom-up via dc electroplating have been carried out similar to techniques used by other groups [5], [6], [10], [12]. Prior to Cu plating, a plastic foil has been applied on the front-side to prevent the overgrowth of Cu and to enhance the sealing of vias. After filling a $\sim 4\text{-}\mu\text{m}$ -thick interconnect on the front and back-side of the wafer has been deposited with Cu electroplating through a negative photoresist. This subsequent Cu plating compensates for the possible nonuniform via fill after the primary bottom-up plating, or small recessions that occur on the front-side due to the via sealing. This reinforces the electrical contact between the metal layer and the vias, and level off the discrepancies between vias in terms of filling.

Fig. 2 shows scanning electron microscope (SEM) and optical pictures of the electroplated TSVs with front and back-side interconnects. They show vias uniformly filled with copper in two different areas. The top part shows uniform sealing without voids. Despite a small recession at the bottom, there is a good connection of the via with the bottom-side interconnects.

III. DC ELECTRICAL MEASUREMENTS

The sheet resistances $R_{\text{sheet}} = R_{\text{meas}} \times \pi / \ln(2)$ of the plated copper of front and back-side interconnects are extracted from Van der Pauw structures [14]. The resistivity of the plated copper on the front and back-side ($\rho = 2.0\ \mu\Omega \cdot \text{cm}$) is close to the bulk resistivity of copper ($\rho = 1.8\ \mu\Omega \cdot \text{cm}$). The small

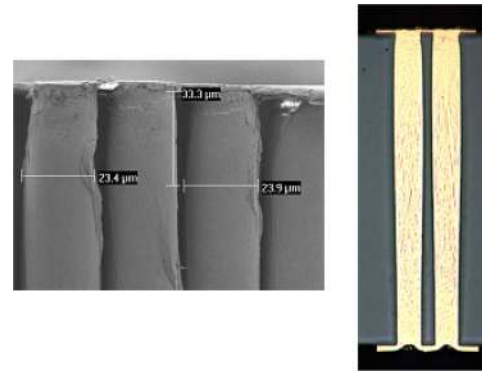


Fig. 2. SEM image of Cu plated vias (left) and optical microscope image of polished cross section of filled via (right).



Fig. 3. Schematic drawing and final front and back-side metal patterning for Kelvin structure.

difference could be due to the fact that no anneal has been performed and therefore the grain size is somewhat smaller and less well controlled than after annealing. Individual TSV resistance data were obtained from Kelvin structures using four point probe measurements [14], [15]. A schematic drawing and pictures of the Kelvin structures are shown in Fig. 3. The front-to-back electrical connection is made by four TSVs in parallel to contact the back-side electrical pads. With this geometry, only the central single via is probed, excluding the front and back interconnect resistance contributions. The median measured resistance of 250 individual vias is $15.3\ \text{m}\Omega$. This corresponds well to the expected via resistance of $R_{\text{via}} = 15.9\ \text{m}\Omega$ for a $20\text{-}\mu\text{m}$ nominal diameter and $250\text{-}\mu\text{m}$ -deep via, assuming a Cu resistivity of $\rho = 2.0\ \mu\Omega \cdot \text{cm}$ (identical to the resistivity of the plated copper on the field).

Via chains with 2, 10, and 100 vias have been characterized electrically. The cumulative resistance versus the number of measured vias is plotted for chains with 2 vias, 10 vias, and 100 vias in Fig. 4. A perfect linear behavior is observed. The electrical lines connecting the vias are identical in all via chains ($40\ \mu\text{m}$ wide, $50\ \mu\text{m}$ long). The corresponding resistances of the front and back-side interconnect are $R_{\text{line}} = 6.8\ \text{m}\Omega$. This resistance is not negligible compared to resistance of a single via and contributes significantly to the total resistance of the chain. The resistance extracted from the slope of the line ($23.7\ \text{m}\Omega$) corresponds to the sum of the average resistance of one via and the average resistance of the top and bottom lines. In doing so, one can derive an average via resistance in the chain of $16.9\ \text{m}\Omega$. This is fully consistent with the median resistance of Kelvin structures ($15.3\ \text{m}\Omega$). The resistance offset of the line corresponds to additional resistances from the admission line at the beginning

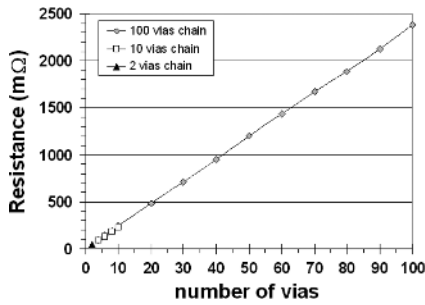


Fig. 4. Resistance versus number of vias for 2-, 10-, and 100-via chains with measurements at intermediate positions.

and the end of the line. It remains in the order of magnitude of an average line resistance.

IV. RF MEASUREMENTS

A. RF-Module Description and Measurements

The RF module is comprised of RF copper lines with different lengths ($40\ \mu\text{m}$, $95\ \mu\text{m}$, $170\ \mu\text{m}$, and $320\ \mu\text{m}$) in order to separate the electrical contribution of the line from the via RF behavior and to be able to extract the own resistance, inductance, and capacitance of the vias. The lines are $30\ \mu\text{m}$ wide and located on the back-side of the wafer. They are connected by two TSVs to the front-side from which the RF measurement is performed. Two designs have been used for these RF lines. The first set of lines has ground planes on the front-side only, while the second set of lines have both front-side and back-side ground planes, connected to each other by several identical TSVs with a diameter of $20\ \mu\text{m}$. In the latter case, the RF lines are also surrounded by ground planes at the back-side. The spacing between them and the transmission line is $29\ \mu\text{m}$. These two configurations are illustrated in Fig. 5. Top and back-side optical pictures of the micromachined coplanar waveguide+line of $95\ \mu\text{m}$ in the double-sided ground planes configuration are shown in Fig. 6. These two sets allow assessing the influence of ground planes on the back-side at RF frequencies. The RF measurements have been carried out on a dedicated RF probe station with a 2-port vector network analyzer with Cascade's dual infinity probes on a frequency range extending from 100 MHz to 50 GHz. Special attention was paid to the calibration of the probes with a LRRM calibration protocol with a $50\text{-}\Omega$ calibration kit. All RF measurements have been de-embedded with the appropriate open-short corrections. It is, therefore, possible to compare the electrical results and extract information from the S -parameters.

B. S-Parameters Analysis

For the single and double ground plane configurations the signals are symmetrical ($S_{11} = S_{22}$ and $S_{12} = S_{21}$) since there is no nonreciprocal component. For both configurations, the S -parameters S_{11} and S_{21} have been plotted in Fig. 7 for three different line lengths ($40\ \mu\text{m}$, $170\ \mu\text{m}$, and $320\ \mu\text{m}$).

One can observe that these lines exhibit a low reflection ($S_{11} \sim -20\ \text{dB}$) and high transmission in the low frequency range (100 MHz–1 GHz). This is the expected RF behavior in this frequency region and proves that the TSVs are functional within the evaluated CPW structure. The transmission S_{21}

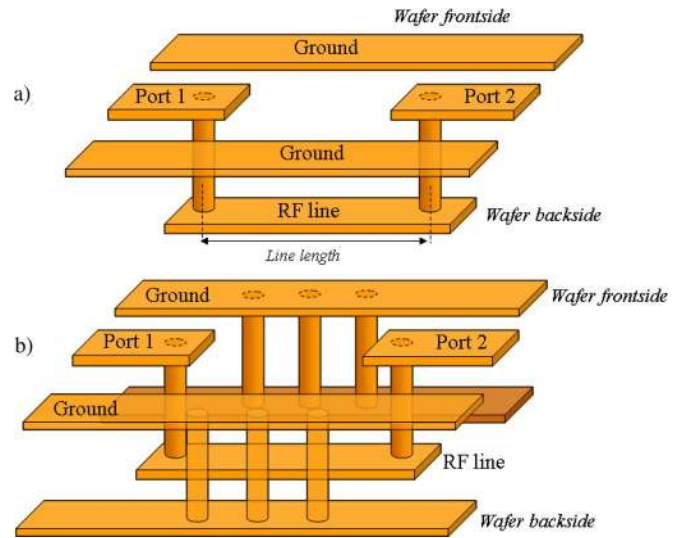


Fig. 5. Sketch of RF copper lines with TSVs (a) with ground planes at front-side only; (b) with ground planes at both the front and back-side.

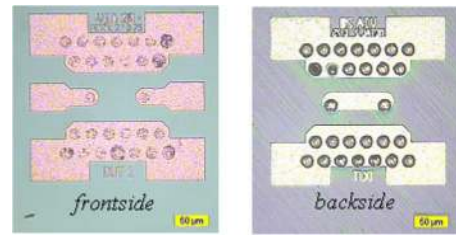


Fig. 6. Optical microscope images of a $95\text{-}\mu\text{m}$ -long RF lines with TSVs and front and back-side ground planes connected with TSVs. Left: front-side view. Right: back-side view.

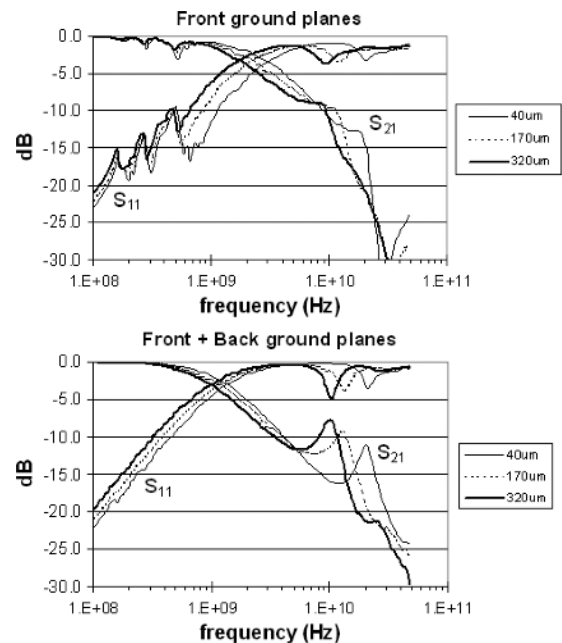


Fig. 7. S -parameters for different line lengths ($40\ \mu\text{m}$, $170\ \mu\text{m}$, and $320\ \mu\text{m}$) with ground plane on front-side only and ground plane on front-side + back-side.

exhibits very low insertion losses at 100 MHz ($-0.15\ \text{dB}$ for single ground planes, and $-0.04\ \text{dB}$ for double ground planes)

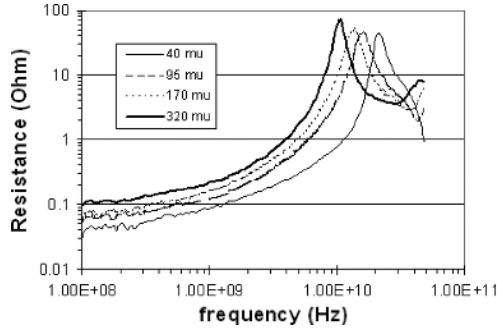


Fig. 8. Resistance R (Ohm) for 40- μm , 95- μm , 170- μm , and 320- μm line lengths with ground planes on both front and back-side.

and starts decreasing beyond 1 GHz. The reflection increases continuously with frequency for the double ground plane configuration. Compared to the double-sided ground plane configuration, the presence of ripples is observed in the single sided ground planes case. These ripples appear reproducibly at identical frequencies for different line lengths, indicating that the ripples are design related. Such ripple can result from a parasitic coupling with the low resistive, floating substrate. In the double-sided ground planes case, the RF lines are surrounded with ground planes, which ensure a quasi transverse electromagnetic mode (TEM) propagation. Clear resonance peaks of the lines are observed above 10 GHz, whereas the resonance peaks are hardly distinguishable in the case of single plane grounding. These results clearly show the possibility to use double ground planes with TSVs connecting both sides in order to get clean signals with low losses. Being able to reduce the parasitic coupling is the first step towards 3D integration and Si interposer applications. The findings extend on the CPW results obtained in [6] which reports on T-resonators only. For the following electrical parameter discussion, we limit ourselves to the CPW double sided ground planes configuration.

C. Resistance

The total resistance of the vias and the line is derived from the real part of differential impedance defined as $Z_{\text{diff}} = Z_0 * (z_{11} - z_{12} - z_{21} + z_{22})$, where Z_0 is the 50 Ω characteristic impedance, and z_{ij} the normalized impedance matrix elements extracted from the S -parameters. The resistance as function of frequency is plotted in Fig. 8 for different line lengths. As expected, the extracted resistance at 100 MHz increases with the Cu line length, as is described in Table I and is consistent with the low loss transmission signal observed on the S_{21} parameters. When the frequency increases, the RF-measured resistance increases due to the skin effect. The skin depth $\delta = (\rho/\pi f \mu_0)^{1/2}$ in Cu at 100 MHz is approximately 7 μm , implying that the skin effect already affects the effective resistance of 20- μm vias + line. This could well explain the small difference between the dc and 100 MHz resistance values. Above 10 GHz, the measured resistance deviates from the Eddy current behavior due to the intrinsic RF resonance of the CPW lines themselves due to the several R , L , and C components in parallel and series (see later in the modelling, Section IV-F and in [6]). This is clearly observed in Fig. 8, where the energy dissipation at the resonance

TABLE I
COMPARISON OF THE LINE + VIAS RESISTANCE BETWEEN THE DC CALCULATED VALUE AND THE MEASURED RESISTANCE AT 100 MHz FOR GROUNDED LINES

Line length (μm)	40	95	170	320
R extracted from DC (m Ω)	37	45	55	75
R extracted at 100 MHz (m Ω)	39	53	63	95

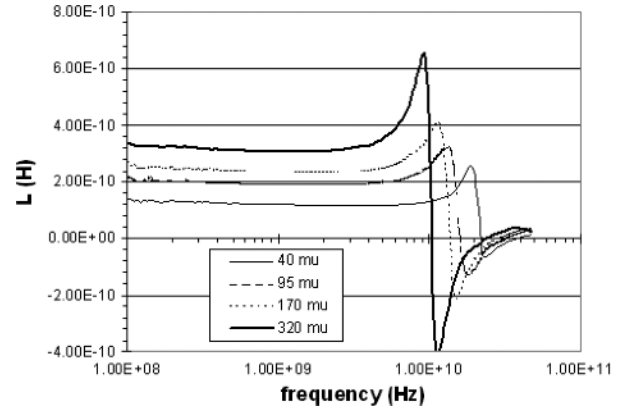


Fig. 9. Inductance L (H) for 40- μm , 95- μm , 170- μm , and 320- μm length lines with both front-side and back-sides ground planes.

translates in a high resistive contribution to the total impedance. The longest lines show the smallest resonance frequency, following a LC -resonance mechanism.

D. Inductance

The series inductance written as $L = \text{Im}(Z_{\text{diff}})/(2\pi f)$ of the line + vias is extracted from the imaginary part of the differential impedance and plotted in Fig. 9 for the different line lengths. The inductance linearly increases from 0.13 to 0.33 nH for 40- μm to 320- μm -long lines, with an inductance per meter of 7.1×10^{-7} H/m for the line.

This value is fully consistent with standard values for CPWs found in literature for similar dimensions [5], [7], [16]. The extracted inductance of one via is $L_{\text{via}} = 53$ pH at frequencies below 100 MHz. The main contribution to the total inductance depends on the length of the line. This inductance value is proportionally two times lower than inductance obtained for moderate aspect ratio vias described in [6] and [7], and 500–1000 times lower than wire bonding, making TSV very attractive for 3D integration. The resonance peaks fall at the resonance peaks already described in the resistance curves. The inductance decreases slightly from 100 MHz to ~ 3 GHz due to the skin effect and is empirically modelled by a skin effect power law as in [6].

E. Capacitance

The total capacitance is extracted from the common mode admittance, $\text{Im}(Y_{\text{com}})$, defined as $Y_{\text{com}} = y_{11} + y_{12} + y_{21} + y_{22}$, where y_{ij} are the normalized admittance matrix elements extracted from the S -parameters. The capacitance $C = \text{Im}(Y_{\text{com}})/(2\pi f)$ is plotted as a function of frequency in

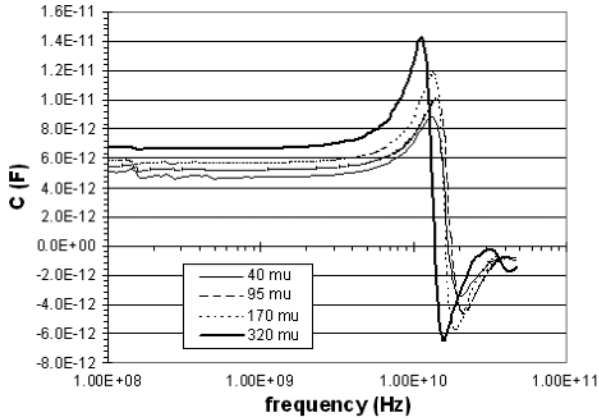


Fig. 10. Capacitance C (F) for 40- μm , 95- μm , 170- μm , and 320- μm length lines with both front-side and back-side ground planes.

Fig. 10 for the different line lengths. The curves indicate that the via capacitance is dominating the total capacitance for the used line lengths. We extract an average capacitance per via of 2.4 pF, and a capacitance density of 4.6 pF/mm for the lines. This can be compared with the theoretical capacitance value based on the following calculations. The total area of the via outer surface is $A_{\text{via}} = 20 \mu\text{m} \times \pi \times 250 \mu\text{m}$, and the dielectric constant of the SiN liner is $\epsilon_r \sim 7.5$ and its thickness is $0.5 \mu\text{m}$ and therefore: $C_{\text{via,theo}} = \epsilon_0 \epsilon_r A_{\text{via}} / d_{\text{diel}} = 2.1 \text{ pF}$. The measured value is higher than the theoretical one but can be explained by a nonideal bowed shape of the vias due to intrinsic limitation of the DRIE etching technique [18] and/or a slightly thinner insulation layer (SiN) in the middle of the via [5].

The nonnegligible capacitance value leads to a strong via coupling with the substrate at higher frequencies. For instance, the total capacitance of the 54 grounded vias of the 320 μm double-grounded lines end up in a total capacitance of $54 \times 2.4 = 130 \text{ pF}$. As the substrate becomes strongly coupled to ground, the occurrence of parasitic resonances and/or ripples is prevented in these devices. If a lower capacitance is required, a silicon oxide insulation could easily replace the SiNx liner, reducing the capacitance by a factor of ~ 1.8 .

F. Modelling

There is great interest trying to build an equivalent electrical model for the vias + line system that describes the full set of results with different dimensions in the microwave regime. A predictive analytical model would be very helpful to achieve a better understanding of 3D integration. Moreover, it would allow circuit optimization and make effective designs in the microwave regime. Obviously, a basic model with RLC series is not sufficient to match the measured resonance frequencies, the capacitance and inductance levels independently, as has already been observed by others [19], [20]. In contrast a numerical simulation is very often to opaque and does not give a simple explanation for a certain behavior [7], [8]. Here, we propose an advanced analytical model for the lines+vias system, which is presented in Fig. 11.

It involves the inductance L_v , the capacitance C_v and the resistance R_v of the via and the inductance L_l , the capacitance C_l and resistance R_l of the line. The losses in the substrate are

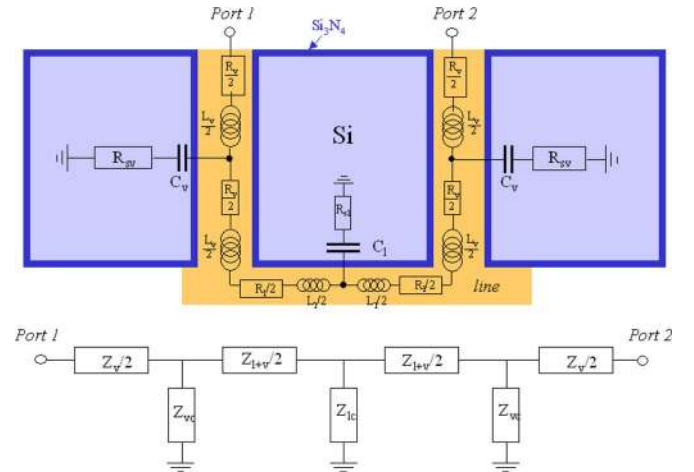


Fig. 11. Equivalent model for the vias + line circuit in RF measurements in a seven impedances electrical scheme.

taken into account as well by two resistances in series of the capacitances, R_{sv} and R_{sl} , of the via and the line respectively. We assume here that the Si substrate is grounded at high frequency by means of the TSV ground planes. After two successive Π - T transformations of the electrical scheme, it is possible to derive analytical expressions for R , L , and C for the vias+line system. There are eight parameters in this model: four for the via (R_v , L_v , R_{sv} , and C_v) and four for the line (R_l , L_l , R_{sl} , and C_l). Four of them (R_l , R_v , C_v , and C_l) are known from the design layout and confirmed by dc measurements of the line: L_v is not known *a priori* but must be constant whatever the line length, and L_l should vary proportionally with the line length. The skin effect is taken into account in the vias and interconnects resistances R_v and R_l . Thus, the only two fitting parameters are R_{sv} and R_{sl} , which only depend on the damping of the system. One expects them to be in the same order of magnitude. The measured data for R , L , and C with their corresponding modeled curves are plotted in Fig. 12 and Fig. 13 for the 40 μm and 320- μm grounded lines. The via parameters R_l , R_v , C_v , and C_l derived from the geometrical layout and confirmed by the dc measurements have been used as input parameters. The model is fitting the R , L , and C curves with a good accuracy below 5%, especially at the lower frequency. The predicted resonance frequencies and the width of the resonance peaks are in very good agreement with the measurements. Using the same parameters for the 320- μm case, the modeled capacitance is slightly lower than the measured value (9%) which could be related due to a possible underestimation of the via capacitance for the longest lines (see Section IV-E). The inductance L_l of the 320- μm line leads to an 8 times higher inductance than the 40- μm line and shows that also this parameter is in perfect agreement with the model. We derive a linear inductance of $5 \times 10^{-7} \text{ H/m}$ for the line that is consistent with the already discussed linear inductance. Similarly, the line capacitance C_l is ~ 8 times higher for the 320 μm than the 40- μm line, which fits perfectly the scaling. All modeling parameters are summarized in Table II. Interestingly, this model predicts some additional resonance after the main resonance peak around 10 GHz since second peaks and peak shoulders are observed in the model curves. The L and C

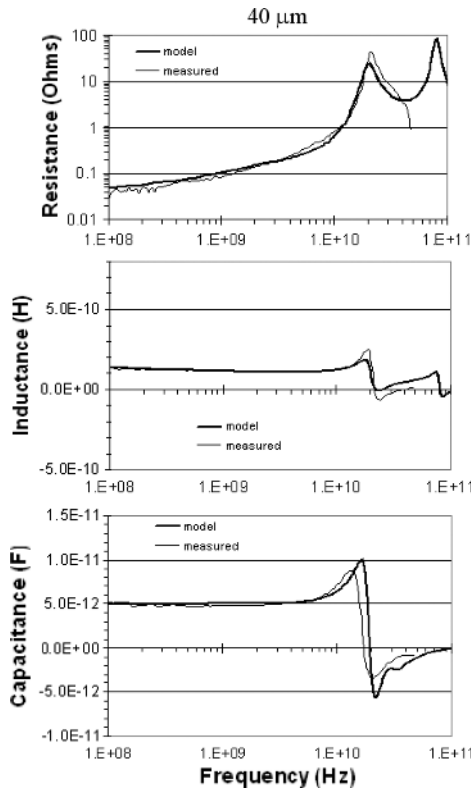


Fig. 12. R , L , and C data curves versus fitted curves from the model for 40- μm grounded lines.

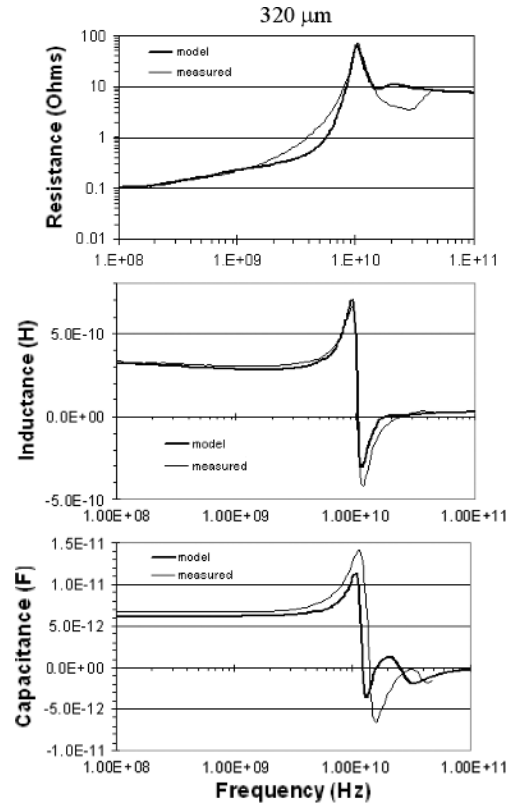


Fig. 13. R , L , and C data curves versus fitted curves from the model for 320- μm grounded lines.

measured curves suggest indeed the possibility of second resonances with a sharp slope of the curve, but the damping seems too high to have a clear picture of it. These possible extra resonance peaks must be investigated in more details by measuring at higher frequencies (e.g., 100 GHz) on a higher resistive substrate. Although many other models are possible, this refined model gives promising results with a minimum of fitting parameters since the only fitting parameters are the substrate losses resistances R_{sv} and R_{sl} , which are close to each other (0.8–6 Ω). These values are relatively low and can be linked to the low intrinsic resistivity of the used wafer ($\sim 0.01 \Omega \cdot \text{cm}$). This explains why the resonance peaks are relatively broad, and why secondary peaks are hardly observed. These results show that even with low resistivity silicon substrates as can be found in actual devices, the TSV behavior is well understood and can be modelled in the RF regime within good specifications.

V. CONCLUSION

In this work, we have used a “via-first” approach for making a RF silicon interposer. The through silicon vias were manufactured with micro-machining techniques and bottom-up electroplating. The dc resistance values match the theoretical expected values for TSVs with an aspect ratio of 12.5 and 250 μm length. The electrical dc behavior has been confirmed in RF measurements where the resistance, the inductance and the capacitance values have been extracted. The need of front-side and back-side ground planes has been demonstrated because it

TABLE II
MODEL PARAMETERS USED FOR MODELLING THE 40- μm AND 320- μm GROUNDED LINES. ONLY THE DAMPING PARAMETERS R_{sv} AND R_{sl} HAVE BEEN USED FOR THE FIT. THE OTHERS PARAMETERS ARE THE THEORETICAL VALUES EXPECTED FROM DESIGN

Line lengths :		40 μm	320 μm
vias	R_v (Ω)	0.015	
	C_v (pF)	2.4	
	L_v (pH)	50	
	R_{sv} (Ω)	0.8	1
line	R_l (Ω)	0.005	0.4
	C_l (pF)	0.16	1.28
	L_l (pH)	20	160
	R_{sl} (Ω)	0.8	6

prevents the occurrence of parasitic coupling RF signals. Functional CPWs on the back-side of the wafer have been achieved that was probed on the front-side of a low resistive silicon substrate. The low via capacitance (2.4 pF) and low inductance (53 pH) confirm the great potential of TSV for 3D packaging compared to wire bonding. An advanced electrical model has been successfully proposed and fits with good accuracy the total R , L , and C curves of the vias + line system for two different line length as function of frequency. The resonance frequency can be predicted using only the dimensions of the system. The model is very powerful since it relies only on the theoretical design parameters of the system and two damping parameters whatever the line length. This model can be used as a guide for 3D integration modeling in the near future for system-in-package applications in the microwave regime.

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