

# RF-CMOS Oscillators with Switched Tuning

A. Kral, F. Behbahani, and A. A. Abidi

Electrical Engineering Department  
University of California  
Los Angeles, CA 90095-1594

Fully integrated CMOS oscillators are of great interest for use in single-chip wireless transceivers. In most oscillator circuits reported to date that operate in the 0.9 to 2 GHz frequency range, an integrated spiral inductor sets the frequency. It is generally believed that an *LC* oscillator, even when it uses a low-Q inductor, displays a lower phase noise than a ring oscillator. However, due to the absence of a good varactor compatible with CMOS technology, the integrated *LC* oscillator suffers from a very *limited tuning range*. Although this tuning range may encompass the limited frequency agility required in an RF oscillator, for instance to span the modulation bandwidth in a transmitter, it will seldom cover the much larger lot-to-lot process variations manifest as spreads of up to 20% in capacitance. Fortunately, the self-inductance of a metal spiral does not suffer spreads, because it depends on a precise number of turns and on the geometry of metal traces which is little affected by fluctuations in lithography.

This work addresses the practical problem of how to design RF CMOS oscillators with a wide enough tuning range to reliably cover process variations, *without* compromising current drain or phase noise. Prototypes were developed in the 0.6- $\mu\text{m}$  MOSIS CMOS process to oscillate at up to 1.8 GHz with a sub-3V supply. The tuning method exploits digital capabilities and MOS analog switches.

## On-Chip Components for Tuning Capacitors

A CMOS oscillator may be continuously tuned with two possible voltage-dependent capacitors: the voltage-dependent *junction capacitor* at the source or drain diffusion; or the voltage-dependent *MOS capacitor* (a MOSFET with source and drain shorted). Now in a MOS oscillator the capacitor in the resonant circuit is subject to large signal swings, on the order of the supply voltage. Thus, depending on its amplitude, the oscillation probes different

regions of the MOS capacitor's small-signal C-V characteristic, from inversion, through depletion, into accumulation (Figure 1). The average capacitance it experiences varies with the bias  $V_{GS}-V_t$ . The frequency of oscillation depends on the average capacitance, while the effect of the varying incremental capacitance across a cycle is to distort the oscillating waveform into a non-sinusoid. This distortion is usually small, and in any case unimportant in this application.

MOS capacitor tuning is used here, as opposed to junction capacitor tuning we have described in previous work [1]. The control voltage on the MOS capacitor may be swept across the full power supply with no fear of forward bias. Also, in a junction capacitor the spreading resistance in the substrate or well is set by junction size and doping, whereas in a MOS capacitor it depends on the region of operation at any instant of time. In accumulation, it is a spreading resistance in the substrate to ground; in depletion, it is this spreading resistance in series with a small capacitor; and in inversion, it is the resistance of the MOSFET channel, which is much lower than the spreading resistance, even at a modest  $V_{GS}-V_t$ .

The oscillator current drain is lowered by using as large a load impedance as is possible at the oscillation frequency. Assuming the inductor dominates the quality factor,  $Q$ , of this *LC* tuned circuit load, this is tantamount to tuning the oscillator with the largest possible inductor. However, as the inductance of a metal spiral is made larger, its self-capacitance increases as well, eventually causing the inductor to self-resonate below the target oscillation frequency, here 1.8 GHz. Therefore, spiral structures with the lowest self-capacitance per unit inductance were investigated.

## Multi-layer Inductors

The three levels of metal available in this process make it possible to fabricate a useful multi-layer spiral inductor [2, 3], whose inductance per unit area, owing to solenoid-like properties, rises almost quadratically with the number of layers. Although there is substantial capacitance between the turns in

the closest layers of such a spiral (Figure 3), the capacitance to substrate experiences the largest signal voltage. Without resorting to selective removal of the substrate underlying the inductor [4], three-layer inductors of about 10 nH may be realized for use at 2 GHz.

This inductor suffers mainly from the loss due to the resistance of the metal windings, but also due to substrate losses caused by displacement currents flowing in the substrate spreading resistance, and due to eddy currents induced in the heavily doped substrate under the 6- $\mu\text{m}$  thick epi layer. A laminated grounded polysilicon shield plate is placed under all the inductors to prevent the displacement currents from flowing into the substrate [5]. A simple four-element model (Figure 2) is found to accurately fit the complex impedance of standalone test inductors measured with a PicoProbe<sup>®</sup> across 0.8 to 5 GHz. The quality factor,  $Q$ , of any inductor at a certain frequency may be deduced from the model. For instance, at 1.5 GHz the  $Q$  of the 13.1 nH inductor is 2.9.

Random voltage fluctuations on the control terminal of a VCO modulate its frequency and induce phase noise [6]. The larger the VCO modulation index  $K_V(\text{Hz}/\text{V})$ , the higher the induced phase noise. This gives rise to a dichotomy, because as mentioned in the Introduction a large  $K_V$  is beneficial to encompass process spreads; however, it will also raise the phase noise. This leads to the concept of switch-selected tuning elements in a VCO.

## Switch-Selected Tuning & Results

### Principle

The frequency of the RF VCO in a wireless transceiver is either set by a synthesizer PLL to some fixed value (as in the receiver, and often in the transmitter), or it is directly modulated by the baseband data across a small fractional range (sometimes in a transmitter). Thus, one way to resolve the conflicting requirements described above is to switch in tuning elements from an array such that a staggered but overlapping series of VCO characteristics is obtained, each with low  $K_V$  but together covering the desired range (Figure 3). A mixed analog-digital PLL must tune this VCO, first by digitally selecting the appropriate tuning element, and then fine-tuning the frequency with the analog output of a phase-frequency detector.

The overlap regions are sufficiently wide to accommodate the modulation bandwidth, if this VCO is to be used in a transmitter. Thus during continuous modulation the tuning element will never have to be switched. Also, the overlap region must

encompass statistical fluctuations across an array of tuning elements fabricated on-chip (which are much lower than process spreads).

### Switched Tuning Capacitors

An  $LC$  oscillator may be tuned by connecting some combination of MOS capacitors selected from a weighted array across a fixed inductor. Each capacitor may be tuned continuously with an analog voltage, and together the array defines the desired piecewise V-f characteristic (Figure 3). The challenge here is to build a satisfactory RF switch which will select the capacitors. The switch resistance must be sufficiently low to not degrade the capacitor  $Q$ . This implies a FET with a large W/L ratio whose large junction capacitance will now parasitically load the capacitor array when the FET is turned OFF, and compress the available spread in capacitance.

In this prototype, the RF switch consists of an array of doughnut-shaped sub-FETs (Figure 4), whose gate encloses the drain junction. The drain junction capacitance is 20% lower than in a conventional interdigitated FET, but the source capacitance is larger. However, this is unimportant in the intended use because the source is grounded (Figure 4). The switch is used to connect a fixed linear capacitor (poly on thin oxide over N+ diffusion) in parallel with a tunable MOS capacitor. The measured tuning range is 1.34 GHz  $\pm$ 6% (Figure 5), which verifies that the (unswitched) MOSFET drain capacitance is not so large that it swamps out the discrete capacitor being connected. The measured phase noise remains almost the same when the RF switch is ON or OFF, which shows that its resistance does not degrade resonator  $Q$ . In the transition region when the switch is partly ON, it severely lowers the capacitor  $Q$  and the phase noise is 12 dB worse. Of course, the switch will never be used in this way. The current drain rises slightly at the lower frequency.

Both the ON resistance of the MOSFET switch and its drain junction capacitance will change with the drain voltage. Over the rail-to-rail oscillation amplitude, the *average* resistance is 80  $\Omega$  and the *average* drain capacitance is 40 fF.

This prototype shows the feasibility of tuning an RF oscillator with an array of switched capacitors.

### Switched Tuning Inductors

While a series MOSFET is able to select a capacitor without degrading resonator  $Q$ , when used in series with an inductor it adds a much larger relative loss. However, one of an array of *independent oscillators* may be selected with a MOSFET switch connected to a common-mode point outside the oscillator loop

(Figure 6). The inductors tuning each oscillator are sized differently. The outputs combine in buffer FETs with a common drain, one of which is turned ON by the selected oscillator. These FETs are of small size so as not to excessively load the resonant circuit in the oscillator core. A larger buffer follows to provide adequate drive to the subsequent circuits. Each oscillator is continuously tuned by a MOS varactor.

The measured frequency tuning characteristics (Figure 7) shows a frequency range from 1.4 to 1.85 GHz with the required overlaps between the switched segments. The measured phase noise at 100 kHz offset is constant within 3 dB across the entire range, while the current drain of the oscillator core rises from 7.2 to 8.5 mA at the high frequencies. A representative phase noise plot (Figure 8) shows a slope of about 30 dB/decade up to an offset of 80 kHz, ascribed to upconverted flicker noise in the MOSFETs. At higher offsets, the slope changes to 20 dB/decade, attributable to white noise.

## Conclusions and Discussion

Using two switched tuning methods, RF CMOS oscillators are shown to obtain a wide tuning characteristic consisting of continuously tuned segments. This is a practical way to accommodate the large shifts in the frequency of fully integrated oscillators caused by lot-to-lot process spreads. The use of multi-layer inductors is shown, and also MOS capacitors as varactors for continuous tuning. With this method, either an array of weighted capacitors may be switched in parallel with a *single* oscillator core, or one of an array of *multiple* oscillator cores may be selected, each tuned by inductors of various sizes.

In the RF context, the quality of a particular oscillator may be gauged by its tuning range, the oscillation frequency ( $f_{osc}$ ), and the normalized

phase noise. From fundamental considerations, for a resonator with a given  $Q$ , phase noise is inversely proportional to: offset frequency ( $\Delta f$ );  $f_{osc}$ ; and the current drain,  $I$ . Table 1 compares the results obtained from the prototypes described here with the best published results for RF-CMOS integrated oscillators [7, 8], after normalization to a 100 kHz offset from 1.8 GHz, per mA current drain.

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- [2] M. W. Geen, G. J. Green, R. G. Arnold, J. A. Jenkins, and R. H. Jansen, "Miniature Multilayer Spiral Inductors for GaAs MMICs," in *GaAs IC Symp.*, San Diego, CA, pp. 303-305, 1989.
- [3] R. B. Merrill, T. W. Lee, H. You, R. Rasmussen, and L. A. Moberly, "Optimization of High Q Integrated Inductors for Multi-Level Metal CMOS," in *Int'l Electron Devices Mtg*, Washington, DC, pp. 983-986, 1995.
- [4] J. Y.-C. Chang, A. A. Abidi, and M. Gaitan, "Large Suspended Inductors on Silicon and their use in a 2- $\mu$ m CMOS RF Amplifier," *IEEE Electron Device Letters*, vol. 14, no. 5, pp. 246-248, 1993.
- [5] C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," in *Symp. on VLSI Circuits*, Kyoto, Japan, pp. 85-86, 1997.
- [6] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. of Solid-State Circuits*, vol. 31, no. 3, pp. 331-343, 1996.
- [7] J. Craninckx, M. Steyaert, and H. Miyakawa, "A fully integrated spiral-LC CMOS VCO set with prescaler for GSM and DCS-1800 systems," in *Custom IC Conf*, Santa Clara, CA, pp. 403-406, 1997.
- [8] J. Craninckx and M. Steyaert, "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," *IEEE J. of Solid-State Circuits*, vol. 32, no. 5, pp. 736-744, 1997.

| Source    | Tuning Range | Technology               | Current Drain (mA) | Frequency (GHz) | Phase Noise (dBc/Hz) | @Offset (kHz) | Scaled to 100 kHz offset from 1.8 GHz (dBc/Hz) | Then scaled to 1 mA (dBc/Hz) |
|-----------|--------------|--------------------------|--------------------|-----------------|----------------------|---------------|--|------------------------------|
| [7]       | 20%          | 0.4 m (high- $\rho$ sub) | 11                 | 1.8             | 113                  | 200           | 107  | 96.6                         |
| [8]       | 14%          | 0.7 m                    | 4                  | 1.8             | 116                  | 600           | 100.4  | 94.4                         |
| This work | 26%          | 0.6 m                    | 8.5                | 1.84            | 101                  | 100           | 101.6  | 92.3                         |
|           |              |                          | 7                  | 1.53            | 104                  | 100           | 103.5  | 95                           |

Table 1

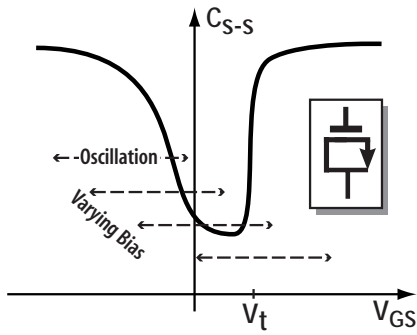


Figure 1: MOS capacitor presents an average capacitance to a large signal that varies with bias.

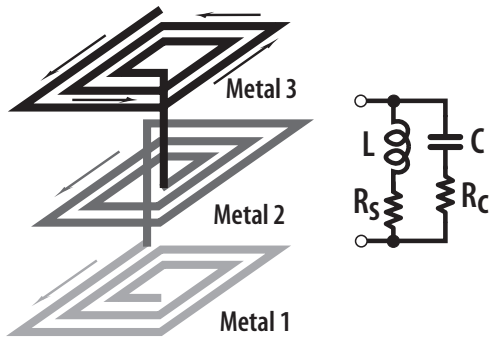


Figure 2: Multi-layer spiral inductor and two-terminal circuit model. Examples of model parameters: {13.1nH,  $R_s=37\Omega$ , 203fF,  $14\Omega$ } or {8.7nH,  $R_s=28\Omega$ , 171fF,  $28\Omega$ }.

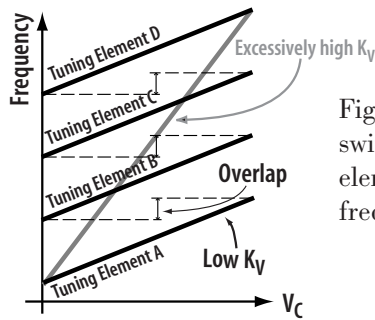


Figure 3: Principle of switched tuning element to cover a wide frequency range.

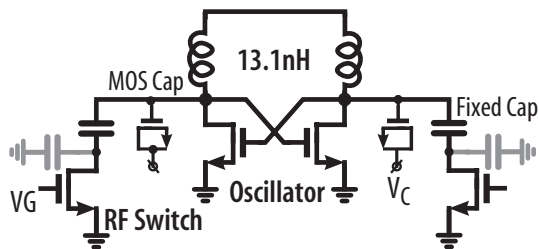


Figure 4: Oscillator tuned with switched capacitor; layout of RF switch FET

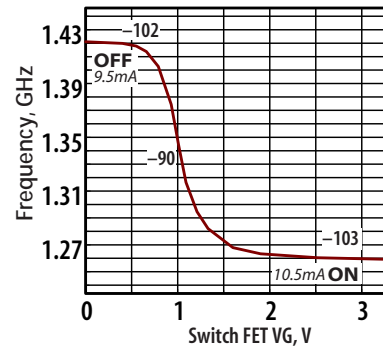


Figure 5: Measured tuning range with fixed switched capacitor. Three measured values of SSB phase noise in dBc/Hz at 100 kHz offset are given, as well as the supply current.

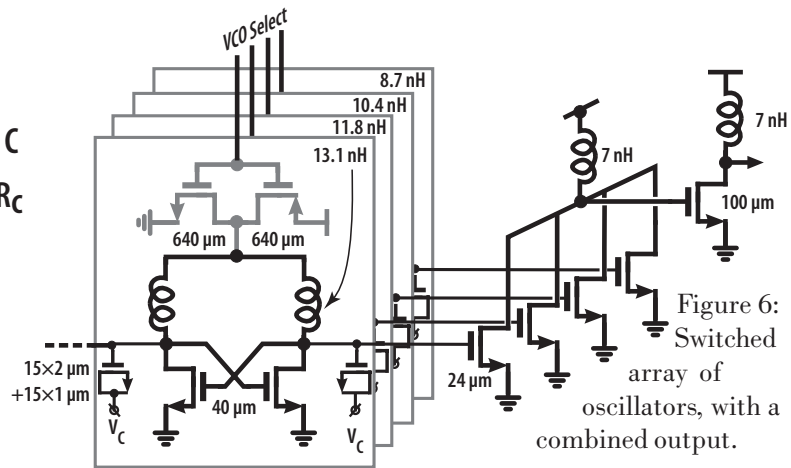


Figure 6: Switched array of oscillators, with a combined output.

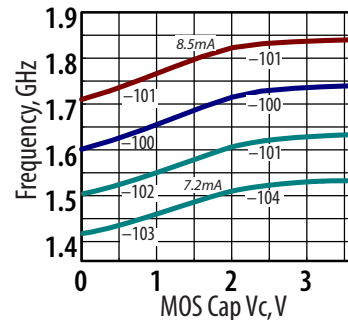


Figure 7: Measured frequency-tuning characteristics of array. Continuous tuning is with MOS capacitor, discrete steps by selecting oscillators with different inductors. Phase noise at 100 kHz offset shown.

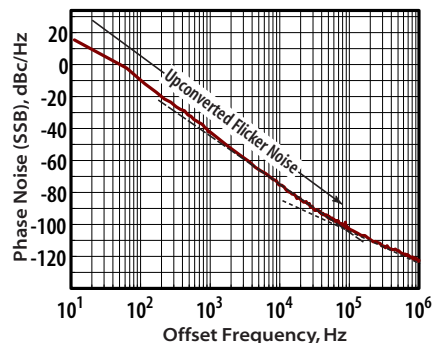


Figure 8: Typical measured actual phase noise plot.