Role of Ga Vacancy on a Multilayer GaTe Phototransistor

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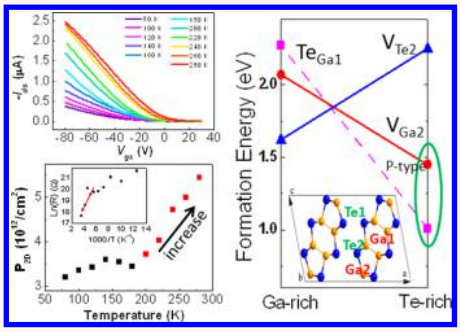
ABSTRACT We report a high-performance field-effect transistor (FET) and phototransistor based on back-gated multilayer GaTe nanosheets. Through both electrical transport measurements at variable temperatures and first-principles calculations, we find Ga ion vacancy is the critical factor that causes high off-state current, low on/off ratio, and large hysteresis of GaTe FET at room temperature. By suppressing thermally activated Ga vacancy defects at liquid nitrogen temperature, a GaTe nanosheet FET with on/off ratio of $\sim 10^5$, off-state current of $\sim 10^{-12}$ A, and negligible gate hysteresis is successfully demonstrated. Furthermore, a GaTe phototransistor with high photogain above 2000 and high responsivity over 800 AW^{-1} is achieved, as well. Our findings are of scientific importance to understand the physical nature of intrinsic GaTe transistor performance degradation and also technical significance to unlock the hurdle for practical applications of GaTe transistors in the future.



KEYWORDS: gallium telluride · transistor · two-dimensional · layered materials · vacancy

As an emerging class of new material, two-dimensional (2D) layered materials have attracted considerable interest in the past decade since graphene was discovered in 2004.[1−3] In contrast to graphene, the presence of an inherent band gap allows 2D semiconductors to be highly promising building blocks for high-performance electronic and optoelectronic applications.[4−6] Moreover, compared to traditional semiconductor materials, such as Si and III−V group materials, 2D layered semiconducting materials exhibit three important features: (1) their ultrathin thickness (atomic level) is beneficial for efficient electrostatic gating and high degree of vertical integration for field-effect transistor (FET); (2) the intrinsic surface free of dangling bonds effectively reduces the surface charge trapping states and roughness scattering, thus obtaining high channel mobility; (3) owing to the nature of 2D structures, by employing current thin film micromanufacturing techniques, they are relatively easily fabricated into complex devices. As a representative, MoS_2 is the most widely investigated 2D layered semiconducting material. Single-layer MoS_2 FET has demonstrated excellent performance, for instance, relatively high channel mobility ($\sim$200 $cm^2\ V^{-1}\ s^{-1}$) and high on/off switch ratio (10^8).[7] Recently, Kis *et al.* has improved the field-effect mobility to exceed 1000 $cm^2\ V^{-1}\ s^{-1}$.[8]

Encouraged by the achievements in MoS_2, various other 2D layered semiconductors such as the family of III−VI compounds (GaS, GaSe, and InSe) have been studied.[9−11] Gallium telluride (GaTe) is another important 2D layered III−VI semiconductor with a direct band gap around 1.7 eV at room temperature in bulk form.[12,13] However, the properties and applications of GaTe are not well-known. This is most likely due to its complicated crystal structure and possible high defect density.[12−14] Strikingly different with the hexagonal structure of GaS and GaSe, GaTe crystallizes into the more complicated and less symmetric monoclinic structure with the space group C_{2h}^3, as shown in Figure 1a. Especially, there are two kinds of Ga−Ga bonds in one single layer: two-thirds are perpendicular to the layer and one-third lie in the layer. As a result, there is only a two-fold rotational symmetry along the *b* axis and no rotational symmetry perpendicular to the (20−1) layer plane (Figure 1b). To date, most discovered 2D layered materials, such as graphene, MoS_2, WS_2, WSe_2, GaS, GaSe, and so on, almost have relatively high

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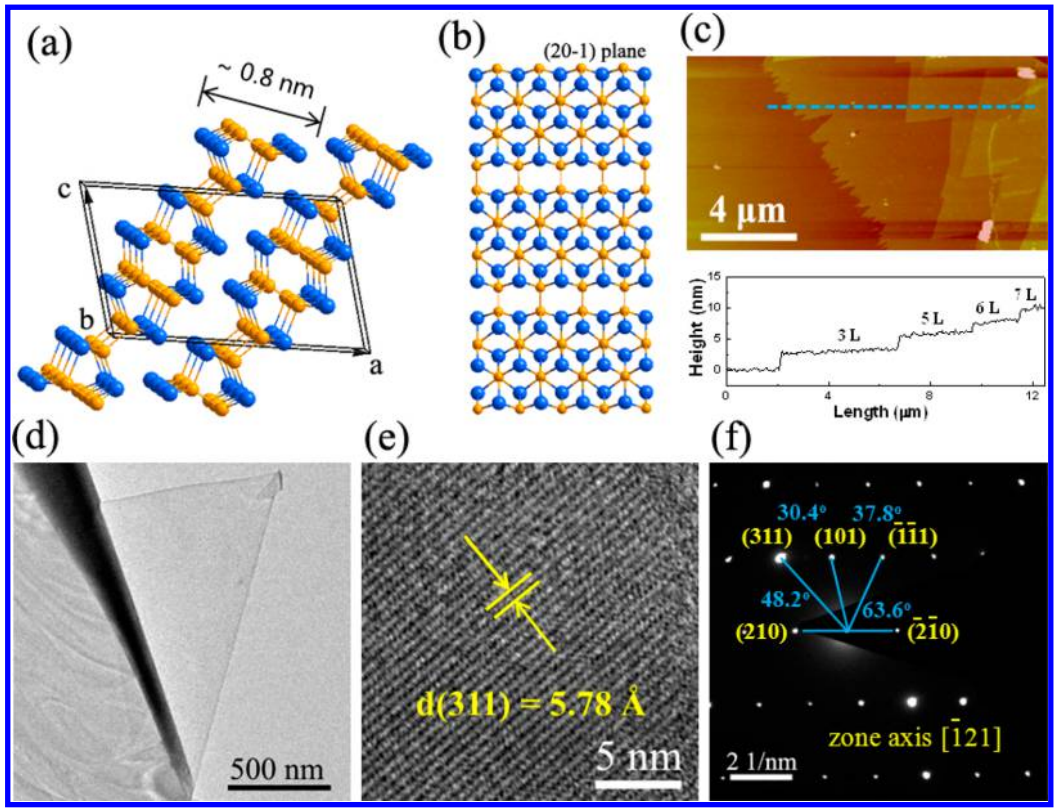

Figure 1. Schemes and characterizations of layered GaTe nanosheets. (a) Scheme of GaTe crystal structure. Blue balls, Te; yellow balls, Ga. (b) Top view along the direction perpendicular to the (20−1) layer plane. (c) AFM image of as-prepared GaTe NSs *via* a tape-exfoliation method (top) and corresponding profile (bottom). (d) TEM, (e) HRTEM, and (f) SAED images of a typical few-layer GaTe NS.

crystal symmetry along the vertical direction.[9,10,15−17] Very few reports are available about high anisotropic 2D layered materials. These anisotropic crystallography characteristics of single-layer GaTe may open up new opportunities for fundamental research and technical applications associated with anisotropic physical properties. At this point, it is significantly important to start the research on GaTe.

For most metal chalcogenide semiconductors, cation vacancies play a crucial role in their electrical properties.[12,18,19] Largely attributed to various defects in bulk GaTe, undoped GaTe exhibits a p-type electrical characteristic.[20] These defects should have strong influences on GaTe FET properties. For example, high off-state current and poor on/off ratio were observed in WS_2 nanotube FETs at room temperature.[21] Similar results were also obtained in some other chalcogenide compounds including WSe_2, As_2S_3, and so on.[22,23] However, how these defects affect the FET performance is not systematically studied, and the physical mechanism is still unclear. Understanding the origin of FET performance deterioration will help us find a way to restore, even enhance, the device performance based on these materials. Here, we report a high-performance FET and phototransistor based on back-gated multilayer GaTe fabricated by mechanically exfoliation method. Through electrical transport measurements at variable temperatures, we find Ga ion vacancy is the critical factor that causes the high off-state current, low on/off ratio of GaTe FET, and large hysteresis at room temperature. First-principles calculations based on GaTe crystal defect states agree very well with our experiments. Compared with ambient conditions, properties of the device at 77 K and 4×10^{-4} mbar vacuum are much improved. By suppressing thermally activated Ga vacancy defects at liquid nitrogen temperature, a FET with on/off ratio of $\sim 10^5$, off-state current of $\sim 10^{-12}$ A, and negligible gate hysteresis is successfully demonstrated. Furthermore, a GaTe phototransistor with high photogain above 2000, high responsivity over 800 AW^{-1}, and fast response of ~0.3 s is achieved, as well. These improved properties indicate that the two-dimensional GaTe nanosheet is a new promising material for high-performance FETs and phototransistors.

RESULTS AND DISCUSSION

High-quality GaTe NSs with different thickness can be easily obtained by repeatedly peeling the bulk using Scotch tape. As shown in Figure 1c, one typical AFM image and the corresponding line profile explicitly reveal the thickness of GaTe sheets' steplike increases from 3 to 7 layers. One single-layer GaTe has around 0.8 nm thickness, and we believe it certainly can be

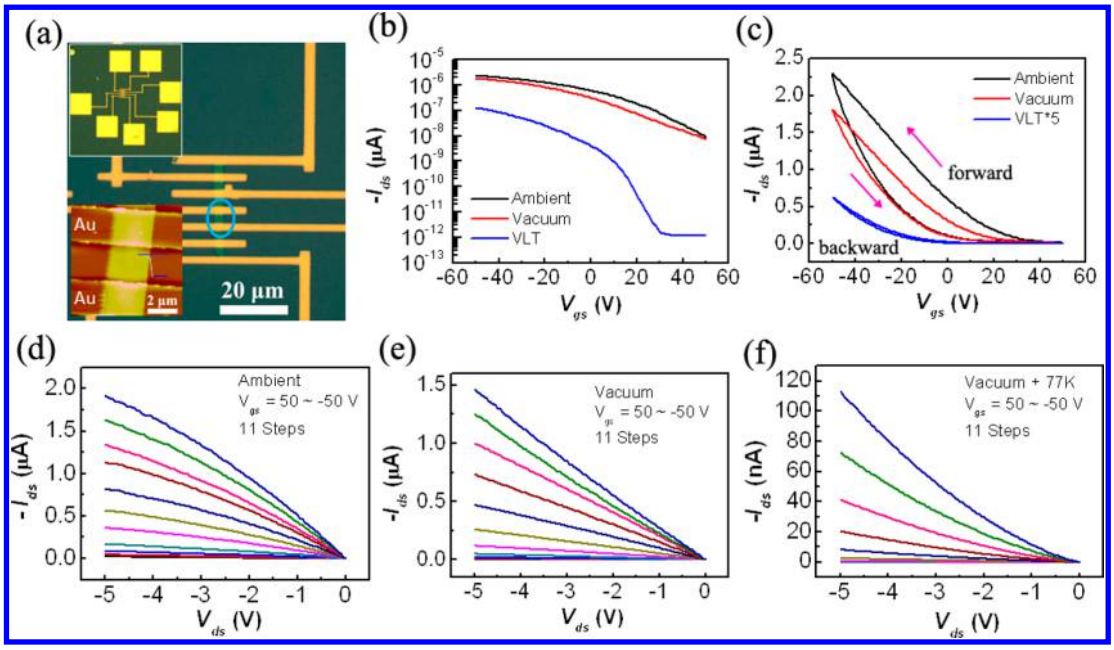

Figure 2. Electrical properties of GaTe-based FET. (a) Optical micrograph of a representative GaTe NS FET device. Top inset: zoomed-out optical image of this device. Bottom inset: AFM image according to the area marked by a blue circle. (b) Transfer curves, (c) hysteresis behavior, and (d−f) output characteristics of the same GaTe transistor measured in ambient, vacuum, and VLT (vacuum and low temperature: 4.2 × 10^{-4} mbar and 77 K) conditions. Note: For (b,c), V_{ds} = −5 V. Note: the drain current under VLT was magnified 5× in panel (c).

fabricated using the Scotch-tape method. However, the optical contrast of GaTe NSs below 3 layers is too weak to be distinguished from the 300 nm thick SiO_2 substrate using traditional optical microscopy, even under 1000-fold magnification (Figure S1, Supporting Information). Figure 1d,e shows the TEM and HRTEM images of a typical thin GaTe NS deposited directly on the TEM copper grid by mechanical exfoliation method. The (311) plane with the lattice constant of about 5.78 Å can be clearly observed in Figure 1e. The corresponding selected area electron diffraction (SAED) pattern (Figure 1f) indicates that the GaTe NS formed is single crystalline. Furthermore, a series of planes and relevant angles between each other shown in Figure 1f confirm that the layered GaTe belongs to a monoclinic crystal system (JCPDS 65-2208). This can be further confirmed by X-ray diffraction (XRD) patterns (Figure S2, Supporting Information). Raman spectra were employed to verify the quality of GaTe NSs. A Raman spectrum measured on a 30 nm thick GaTe sheet is consistent with previous reports on single GaTe crystals (Figure S3, Supporting Information).[24,25] All characterizations above clarify that the GaTe NSs prepared by the tape-peeling method contain high crystal quality, good optical properties, and layer number controllability.

A back-gated multilayer GaTe FET was fabricated on a highly p-doped silicon substrate with a 300 nm thick SiO_2 layer, schematically shown in Figure 2a. The linearity of $I-V$ curves indicates the ohmic contacts between GaTe sheets and Cr/Au electrodes (Figure S4, Supporting Information). The electrical properties of GaTe are strongly affected by environmental conditions including vacuum and temperature. Here, for convenience, we refer to the condition of 4 × 10^{-4} mbar pressure as "vacuum". The condition of both vacuum and 77 K is assigned as "VLT" (vacuum + low temperature). In order to rule out the possible artifacts from gate hysteresis, all $I-V$ curves were collected on the same measurement cycle scanning from positive to negative bias. Figure 2b shows that the multilayer GaTe NS demonstrates a significant p-type behavior in all three different conditions: ambient, vacuum, and VLT. It was found that, in ambient conditions, GaTe FET exhibits relatively poor properties: high off-state current of ~1 × 10^{-8} A and consequent low on/off ratio of ~230. In order to improve the properties, the device was held for 4 h in vacuum to remove the surface adsorbates. Nevertheless, nothing but slight decrease of the drain current happened, which originates from the removal of the surface p-dopant adsorbates.[26,27] Once the device was cooled to 77 K, a remarkable property enhancement was observed. The off-state current approaches ~1 × 10^{-12} A and lowers ~4 orders of magnitude. On/off ratio reaches ~10^5 and is enhanced more than 400 times. In addition, the AFM image in Figure 2a indicates that the GaTe ribbon has uniform thickness around 33 nm, as well as the channel length and width are approximately 1.9 and 1.8 μm, respectively. Based on above device configuration, the hole field-effect mobility can be estimated to ~0.10 cm^2 V^{-1} s^{-1} using a standard method, which is comparable to those of back-gated MoS_2 FETs without dielectric screening and ultrathin GaS and GaSe transistors.[10,28]

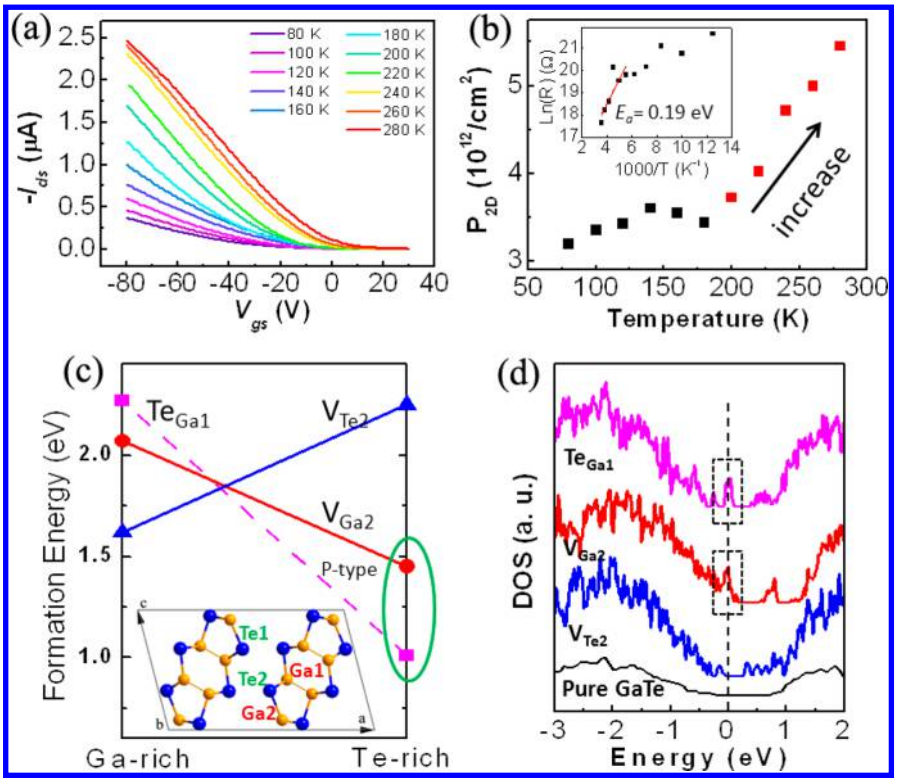

Figure 3. Temperature-dependent transistor characteristics and first-principles calculations. (a) $I_{ds}-V_{gs}$ curves of the GaTe NS FET recorded at various temperatures ranging from 80 to 280 K. $V_{ds} = -5$ V. (b) Charge concentration p_{2D} as a function of temperature at $V_{gs} = -80$ V. Inset: Arrhenius plot of the two-probe resistance of the same device. (c) Formation energy of three types of detects in GaTe crystal: Te and Ga vacancies (V_{Te2} and V_{Ga2}) and Te-on-Ga antisite (Te_{Ga1}) as a function of Te chemical potential. Note that a total of six defect sites are tested in terms of Ga and Te positions (inset) according to the crystal symmetry, and the three cases with low formation energies are shown. For antisite, the dashed line is a guide for the eyes, and the actual curve connecting the end points is not necessarily linear. (d) DOS for perfect GaTe and three defective structures. The black dashed rectangles highlight the position of the hole states in the band gap of GaTe. Zero is the Fermi level.

The hysteresis is defined as the threshold voltage (V_{th}) shift between the forward and reverse V_g sweeping. It may strongly influence the reliability of GaTe FETs and thus was carefully investigated. To eliminate this effect from gate bias sweeping rate, the data in Figure 2c were collected at a fixed V_g scanning rate of 1 V/s (Figure S5, Supporting Information). From ambient, vacuum, to VLT conditions, the hysteresis step-by-step decreased from 45.0, 28.5, to 1.9 V. The first stage improvement largely originates from removal of surface trapping states by vacuum.[29] The second stage enhancement is likely due to the suppression of thermally activated defects. It will be further discussed later. Output characteristics of the same GaTe transistor measured in ambient, vacuum, and VLT were shown in Figure 2d–f. Interestingly, the drain current tends to slightly saturate when the source–drain voltage scans from 0 to 5 V in ambient, which should be related the surface adsorbate scattering. This phenomenon exists not only in relatively thick GaTe nanosheets (~30 nm) but also in thin layers. Similar results were obtained in a ~8.5 nm thick GaTe transistor (Figure S6, Supporting Information).

To obtain a better insight into the mechanism of how temperature affects the FET performance, variable temperature measurements as well as the theoretical simulation were carried out. Figure 3a shows that, as the temperature increases, the V_{th} of the device moves to the positive direction, which suggests that more channel charges were generated. Further, the 2D charge density (p_{2D}) can be deduced using a parallel-plate capacitor model following this equation:[30] $p_{2D} = C_{ox}\Delta V_{bg}/e$, where $C_{ox} = \varepsilon_0\varepsilon_r/d_{ox}$, $\varepsilon_0 = 8.85 \times 10^{-12}$ Fm^{-1}, ε_r is 3.9, and d_{ox} is 300 nm for SiO_2, e is the electron charge 1.6×10^{-19} C, $\Delta V_{bg} = 80 - V_{th}$. The relationship of p_{2D} *versus* temperature was plotted in Figure 3b. Under the temperature range from 80 to 200 K, the charge density changes very little, whereas above 200 K, it sharply increases. The transfer curves at various temperatures, decreasing from 280 to 80 K at a step of 20 K, were also systematically measured, and similar results were obtained (Figure S7, Supporting Information). These results indicate that one defect state above the valence band maximum of GaTe sheets is thermally activated at $T > 200$ K. In the temperature range from 200 to 280 K, the relationship of the resistance *versus* temperature can be described with Arrhenius plot: $\ln(R_T) = \ln(R_0) + E_a/2kT$, where R_T is the resistance at T K, R_0 is the resistance at $T = \infty$, E_a is the thermal activation energy, and k is the Boltzmann

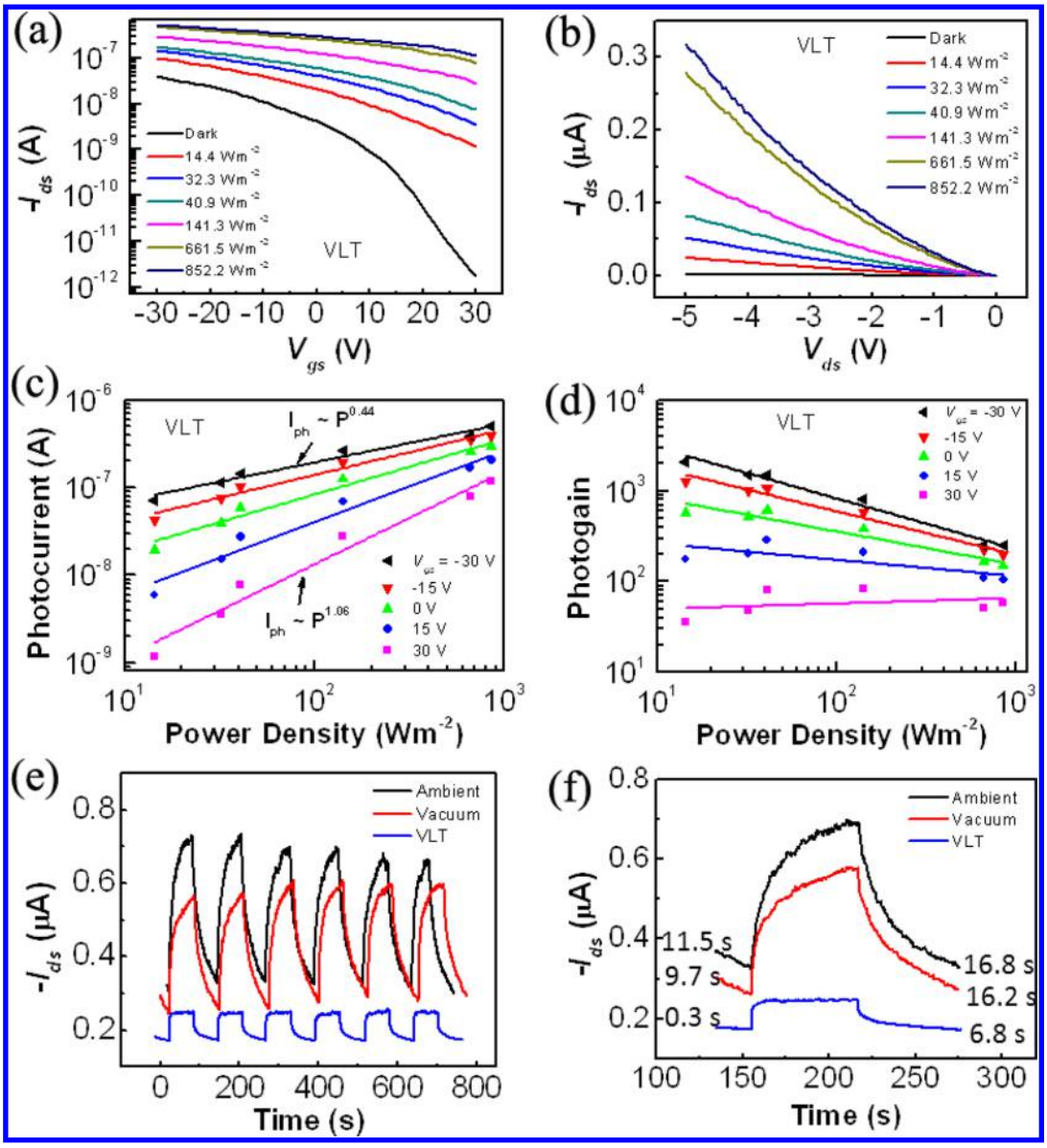

Figure 4. Characteristics of a GaTe phototransistor. (a) Transfer curves of the GaTe NS phototransistor measured at different light intensity in VLT. $V_{ds} = -5$ V. (b) Output characteristics of the phototransistor for various light power density without gate bias applied. (c,d) Laser power dependence of the photocurrent and photogain, respectively. $V_{ds} = -5$ V. (e) Photoswitching characteristics and (f) one time-resolved photoresponse cycle of the same transistor measured with a 473 nm laser on and off under ambient, vacuum, and VLT conditions. $V_{gs} = 0$ V, laser power density = 141.3 W m^{-2}.

constant. The data shown in the inset of Figure 3b suggest that the charge transport is thermally activated and the activation energy is 0.19 eV, which is consistent with that of gallium vacancy level.[12] To eliminate the possible effects from GaTe crystal structural change at $T > 200$ K, Raman spectra at various temperatures ranging from 80 to 290 K were systematically measured (Figure S8, Supporting Information). Almost all Raman peaks do not show a clear shift, and no new Raman peaks occur with the temperature increase. These results suggest that no structural change happens in the temperature range from 80 to 290 K.

First-principles calculations are carried out to uncover the origin for defect-induced p-type electrical characteristics. Figure 3c shows the calculated formation energy for three low-energy native defects as a function of the Te chemical potential μ_{Te}: a low μ_{Te} describes the Ga-rich growth conditions, whereas a high μ_{Te} describes the Te-rich growth condition. Figure 3d illustrates their corresponding electronic structures. It reveals that Ga vacancy (V_{Ga}) and the Te-on-Ga antisite (Te_{Ga}) are acceptors, while Te vacancy (V_{Te}) is a donor. This implies the Te-rich growth condition of the samples. Although the Te_{Ga} has the generally lowest formation energy under the condition, it behaves like a deep-level acceptor (see Figure 3d), most likely corresponding to the experimentally observed defect state with an activation

energy of 0.6 eV.[12] Hence, the thermally activated p-type defects above 200 K in our samples are largely assigned to the Ga ion vacancies, V_{Ga2}. Combining the theoretical and experimental results, we conclude that Ga ion vacancy is the critical factor that causes the high off-state current, poor on/off ratio of GaTe FET, and large hysteresis at room temperature. These original findings will be very beneficial for the fabrication of high crystal quality GaTe and hence high-performance GaTe NS FETs.

With thermally activated Ga vacancy suppression at liquid nitrogen temperature, a GaTe phototransistor was investigated by exploring the characteristics of photocurrent, photogain, and photoswitching. A 473 nm laser (with higher photon energy than the band gap) is employed to perform photoresponse experiments. Figure 4a displays the $I_{ds}-V_{gs}$ curves, and Figure 4b is the $I_{ds}-V_{ds}$ plots of the GaTe phototrasistor measured under different illumination laser power density in VLT. When the incident light intensity increases from 14.4 to 852.2 W m^{-2}, the photocurrent ($I_{ph} = I_{illumination} - I_{dark}$) monotonically increases. Meanwhile, the photocurrent and photogain exhibit strong dependence on the gate bias, as shown in Figure 3c,d. Figure 3c indicates that the photocurrent at a positive gate bias of 30 V is linearly proportional to the incident light power density: $I_{ph} \sim P^{\beta}$, where $\beta = 1$. The linear relationship suggests that the photocurrent is solely determined by the amounts of absorbed photon. As the gate voltage shifts from 30 to −30 V, the value of β decreases from 1.06 to 0.44. The loss of photocurrent could be due to recombination of the photogenerated free carriers and charge trapping by the defects and charge impurity in GaTe.[26,31] Photogain (G) can be calculated by the formula: $G = (I_{ph}/q)/(PS/h\nu) = h\nu R_{\lambda}/q$,[32] where I_{ph} is the photocurrent, q is the electron charge, P is the incident light intensity, S the effective illuminated area, h is Planck's constant, ν is the light frequency, and R_{λ} is responsivity. We find that G is higher than 2000 and R_{λ} is over 800 AW^{-1} under VLT at $P = 14.4$ W m^{-2}, $V_{gs} = -30$ V, and $V_{ds} = -5$ V, which are comparable to those of the MoS_2 phototransisor.[26] To study the stability and photoresponse speed of the device, the time photoresponse with the laser switching on and off was performed, as shown in Figure 4e,f. Compared with ambient and vacuum conditions, photoswitching behavior of GaTe NS phototransistors under VLT is much more stable and lower noise. As the external condition changes from ambient, vacuum, to VLT, the rising time decreased from 11.5, 9.7, to 0.3 s and decay time reduced from 16.8, 16.2, to 6.8 s, as shown in Figure 4f. All of these improvements are ascribed to the removal of surface adsorbates and the suppression of Ga ion vacancies.

How exactly do Ga vacancies affect the performance of GaTe transistors at room temperature? Based on solid physics theory, vacancy density is strongly dependent on the temperature and has significant impact on the electrical characteristics. In general, low temperature generates low vacancy density, thus low charge density. High off-state current and low on/off ratio of GaTe transistors at room temperature should come from relatively high defect densities. For hysteresis, when gate bias sweeps from positive to negative direction, the trapping states based on Ga vacancies capture many carriers; when gate bias sweeps conversely, partial carriers will be slowly moved back into the channel from the trap centers, which generates large hysteresis. Similar to hysteresis effect, the stability and response time of GaTe phototransitors are also affected by various traps in the GaTe NSs. Once GaTe NSs are illuminated by the light, photogenerated carriers may first fill the trap states and then reach the maximum, which degrades the response speed. Consequently, when the light is turned off, partial carriers will be released slowly from the trapping states, which prolongs the reset time and deteriorates the stability, as well.

CONCLUSION

In conclusion, through electrical transport measurements at variable temperatures and theoretical calculations, we find Ga ion vacancy is the critical factor that causes the high off-state current, low on/off ratio, and large hysteresis of GaTe FETs at room temperature. By suppressing thermally activated Ga vacancy defects at liquid nitrogen temperature, the performance of GaTe transistors is much improved: (1) the off-state current approaches $\sim 1 \times 10^{-12}$ A and lowers ~4 orders of magnitude; (2) on/off ratio reaches $\sim 10^5$ and is enhanced more than 400 times; (3) the hysteresis largely decreases from 45.0 to 1.9 V. Furthermore, by suppressing thermally activated Ga vacancy defects at liquid nitrogen temperature, a GaTe phototransistor with high photogain above 2000, high responsivity over 800 AW^{-1}, and fast response of ~0.3 s is successfully demonstrated. Our studies find the intrinsic hurdle that degrades the room temperature performance of GaTe transistors and the results are significantly important to help us find a way to restore, even enhance, GaTe transistor performance.

METHODS

GaTe multilayer flakes were mechanically exfoliated from bulk GaTe (99.99%, Alfa Aesar) and transferred to a heavily doped p-type silicon substrate with a 300 nm thick thermal oxidation layer. The thickness was examined by atomic force microscopy (AFM, Veeco Multimode), and microstructures were characterized by high-resolution transmission electron microscopy (HRTEM, FEI F20). The electrical contact patterns were

defined by standard e-beam lithography. Cr/Au (8 nm/60 nm) electrodes were deposited using a thermal evaporation machine. The electrical transport measurements were carried out on a probe station (Lakeshore, TTP4) equipped with a vacuum pump, a flow cryostat, and a semiconductor characterization system (Keithley 4200). The phototransistor properties were measured using a 473 nm laser (RGBLase). The first-principles calculation method for this study can be found in Supporting Information.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Optical image of layered GaTe is shown in Figure S1. XRD data and Raman spectrum are presented in Figure S2 and Figure S3. Linear I_d-V_d curves for GaTe FET are provided in Figure S4. The hysteresis dependence on gate bias sweeping rate is shown in Figure S5. The electrical properties of a thinner GaTe device is shown in Figure S6. Figure S7: transfer curves of a GaTe device at various temperatures decreasing from 280 to 80 K. Variable temperature Raman spectra are shown in Figure S8. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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