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Role of Threshold Voltage Shift in Highly Accelerated Power Cycling Tests for SiC MOSFET Modules

Haoze Luo, *Member IEEE*, Francesco Iannuzzo, *Senior Member IEEE*, and Marcello Turnaturi

***Abstract* –In silicon carbide (SiC) power MOSFETs, threshold voltage instability under high-temperature conditions has potential reliability threats to long-term operation. In this paper, the threshold voltage shifts caused by the instability mechanisms in accelerated power cycling tests for SiC MOSFETs are investigated. In conventional power cycling tests, the positive threshold voltage shift can cause successive on-state resistance increases, which can sequentially increase junction temperature variations gradually under fixed test conditions. In order to distinguish the increased die voltage drop from the bond wire resistance degradation, an independent measurement method is used during the power cycling tests. As the number of cycle increases, SiC die degradation can be observed independently of bond wire increases during the tests. It is studied that the SiC die degradation is associated with the threshold voltage instability mechanisms. Unlike the bond wire lift-off failure, the die degradation and the related die resistance increase can stop the power cycling test in earlier than expected. Additionally, a new test protocol considering die degradation is proposed for power cycling test. By means of power device analyzer, the failure mechanism and degradation performance of SiC MOSFETs before and after the power cycling test are compared and discussed. Finally, experimental results confirm the role of threshold voltage shifting and identify different failure mechanisms.**

***Index Terms* –Silicon carbide, power MOSFET, power cycling test, threshold voltage instability, bond wire, online monitoring methods.**

I. INTRODUCTION

Silicon carbide (SiC) materials are regarded as the most promising alternative to Silicon (Si) for the future power conversion system. As the material and fabrication techniques continue to develop, the commercially available SiC-MOSFET modules can cover the rating voltages from 400 V to 1700 V since 2015 [1]. Although the thin and small die size as well as the high frequency can improve the overall power density of converter, these features also bring more intense thermal fatigue to both the dies and packages [2].

So far, the tolerable maximum junction temperature (T_j) for most of the commercial SiC MOSFET modules is no more than 200 °C, which is far lower than the theoretical value around 500 °C [3]. Many researches have shown that the high-temperature environment can cause the threshold voltage (V_{th}) instabilities in SiC power MOSFETs [4]–[6]. The significant positive/negative V_{th} shifts can happen under specific working conditions because of the instability mechanisms. Due to the properties of interface SiC/SiO2, the threshold voltage shift in SiC MOSFET is more serious than that of Si-based MOSFETs [7]. The notorious V_{th} instabilities in SiC-MOSFETs can be regarded as one of the main obstacles to the long-term high-temperature applications. During the long-term operation, the gradually increased on-state resistance (R_{on}) caused by the positive V_{th} shift under elevated temperature can decrease the efficiency and deteriorate reliability of SiC MOSFETs.

In practice, the gate reliability tests for V_{th} stability are usually conducted with high-temperature gate bias (HTGB) and high-temperature reverse bias (HTRB) tests before the delivery [8]. The specific positive gate voltage is applied to the gate side under high-temperature environment alone (such as 175 °C) for 1000 hours' storage without drain current [9]. During these "static" gate bias tests, the positive gate bias can cause a positive V_{th} shift. On the contrary, the negative gate bias can result in the downward V_{th} shifting. Usually, the successive V_{th} shift after the "static" gate bias test is a few hundred millivolts, which is within the normal tolerance for the well-designed gate oxide layer. However, the standard "static" gate bias tests do not reflect the practical operation conditions of SiC MOSFETs. In practice, the running SiC MOSFETs usually work under pulsed current with the positive gate bias and high junction temperature (T_j) during the on-state conditions. Recently, studies have shown that the gate-bias stressing at high-temperature and drain current conditions can lead to much larger V_{th} shift than high-temperature conditions alone [7], [10]. Furthermore, according to the preliminary experiments, the general trend for V_{th} shift is positive under the normal working conditions, even the symmetrical back-and-forth bias stress like +15V/-15V is applied to the gate side [6].

Nowadays, the temperature-dependent reliability issues for power modules have attracted extensive attention from industries and academics [11]–[14]. Usually, the power cycling test is an effective way to investigate the packaging reliability under highly thermal acceleration conditions. The objective of power cycling test campaign is to evaluate different material-related failure mechanisms [15] and further estimate the relevant lifetime of modules [16], [17]. In case of highly accelerated thermal cycling test, V_{th} of SiC die can gradually shift if a continuous gate voltage bias is applied to the gate for an extended period [10]. However, the countermeasures and the consequent effects in SiC power cycling test have not been addressed yet.

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The objective of this paper is to evaluate and validate the V_{th} shift effects on the lifetime of SiC modules in the accelerated power cycling test. This paper clearly reveals the role of V_{th} shift effects in the power cycling tests. By introducing the independent measurement method, both the die on-state voltage and the package voltage drop are measured separately during the tests. With the increase number of cycles, the changes of die on-state voltage caused by V_{th} shift can be monitored. Then the propagation and acceleration process induced by die degradation and the corresponding effects on bond wire degradation are investigated separately. By means of power device analyzer, the failure mechanisms for SiC-MOSFET modules behind the power cycling tests can be investigated and identified. Finally, a new test protocol for SiC MOSFET modules in accelerated power cycling test is proposed.

The remainder of the paper is organized as follows. In Section II, the charge trapping mechanism and the effects of V_{th} shift are introduced. In Section III, the conventional power cycling test setup for SiC-MOSFET modules and the related problem statements are presented. The experimental results and discussion are shown in Section IV and Section V, separately. Finally, it is the conclusion.

II. Effects of Vth Shift in SiC MOSFET

A. Mechanisms of V_{th} shift

Owing to the process technologies, the thermally grown oxide contains four categories of positive charges: mobile charge (m), fixed oxide charge (F), trapped oxide charge (T), and interface state charge (I) [5]. The consequently charge trapping effect during operation is depicted in Fig.1. Moreover, the time-dependent threshold voltage V_{th} can be expressed as:

$$\begin{cases} Q_{ox} = Q_T + Q_m + Q_I + Q_F \\ V_{th} = V_{thi} - \dfrac{Q_{ox}}{C_{ox}} \end{cases} \quad (1).$$

Where V_{thi} is the initial threshold voltage, C_{ox} is the specific capacitance of the gate oxide layer.

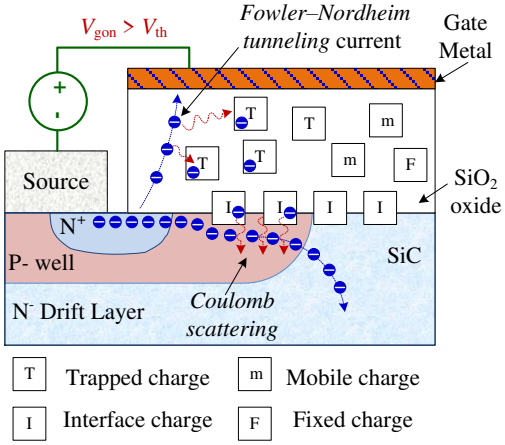

Fig.1. Multi charges in oxide growth layer silicon surfaces.

Theoretically, the large positive V_{th} shift under driven and high-temperature conditions can be attributed to two aspects. Firstly, the direct tunneling of electrons into the interfacial oxide traps near SiC/SiO2 interface [18], [19]. Besides, in case of the thin gate oxide layer (e.g. less than 50 nm), a Fowler–Nordheim tunneling current can inject additional electrons into SiO2 layer and then cause further V_{th} shift [20]. Secondly, significant V_{th} shift under high temperature and gate bias stress conditions can ascribe to the activation of additional oxide traps over operation time [6], [7].

B. Effects of V_{th} shift on die resistance

In DC power cycling test, the SiC MOSFETs are operated in the linear region with relatively low drain voltage V_{DS} and high I_{load}. Assuming the gate overdrive (V_{gs}-V_{th}) is larger than the on-state V_{DS}, the on-state V_{DS} under given current I_{load} can be expressed as [21].

$$V_{DS} = \frac{I_{load} L_{CH}}{Z \mu_{in} C_{ox}} \frac{1}{\left(V_{gs} - V_{th}\right)} \quad \text{for } |V_{DS}| << V_{gs} - V_{th} \quad (2).$$

Where L_{CH} is the length of channel, Z is the width of channel, C_{ox} is the specific capacitance of the gate oxide layer and μ_{in} is the electron mobility in the inversion layer. Among of them, L_{CH}, Z and C_{ox} can be treated as constant for a specific device, but μ_{in} is inversely proportional to temperature. In case of fixed I_{load}, V_{DS} varies with rising temperature within a given time period (t_0~t_1), so the conduction loss P_{cs} and related temperature swing ΔT_j can be expressed as

$$\Delta T_j \propto P_{cs} = L_{load} V_{DS} = I_{load} \int_{t_0}^{t_1} \frac{I_{load} L_{CH}}{Z \mu_{in} C_{ox}} \frac{1}{\left(V_{gs} - V_{th}\right)} dt \quad (3).$$

According to the V_{th} shift mechanism, the threshold voltage after the degradation is higher than the initial value V_{thi}. As a result, the die resistance R_{on} and related conduction power loss under fixed initial test conditions can increase subsequently with V_{th} increase.

C. Conventional Power cycling test without V_{th} shift

The schematic of conventional DC-based power cycling test is depicted in Fig.2 [22]–[24]. The constant load current I_{load} is generated by a high-power DC current source power supply. All the devices under test (S_{a1}, S_{a2}, … S_{an}, S_{b1}, S_{b2},… , S_{bn}) are divided into two groups and connected in series. By using the independent gate drivers (G_{a1}, G_{a2}, … G_{bn}), the inspected devices are always kept as on-state conduction by applying constant gating voltages. Meanwhile, two external switches SW_1 and SW_2 under complementary operation are used for the constant I_{load} commutation.

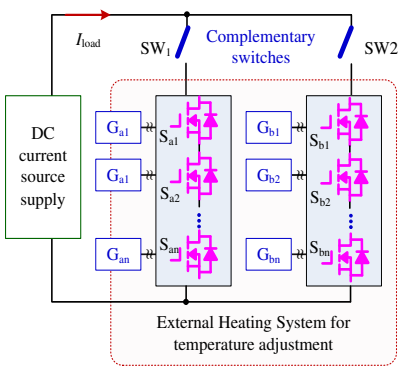

Fig.2. Schematic of conventional DC-based power cycling test platform.

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The conventional control principle for the desired ΔT_j without V_{th} shift phenomenon is depicted in Fig.3. Correspondingly, the related definitions labeled in Fig.3 are listed in Table I. As shown in Fig.3, the voltage drop on the module V_{DS} during on-state condition mainly consists of two parts, the voltage drop on die V_{cp} and the voltage drop on bond wire V_{bw}. Remarkably, the die should be regarded as a heating source and the related V_{cp} accounts for the majority of V_{DS}. It is also shown that the instantaneous power loss P_b at t_1 can be higher than P_a at t_0. Because the die voltage drop is proportional to T_j in case of fixed I_{load}, the heating power loss P_{cs} varies with T_j.

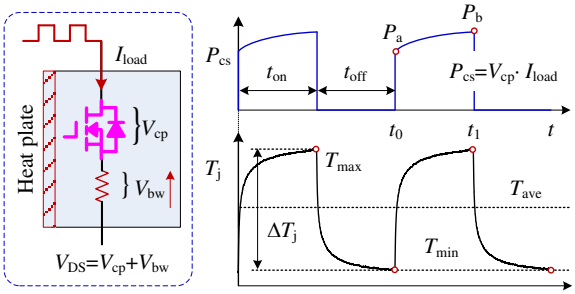

Fig.3. Control principle for DC power cycling test and temperature swing without V_{th} shift.

TABLE I. Electrical Definitions Before and After Threshold Voltage Shift

Notification	Without V_{th} shift	With V_{th} shift
Voltage drop on die	V_{cp}	V_{cpa}
Voltage drop on bond wire	V_{bw}	V_{bwa}
On-state power loss	P_{cs}	P_{csa}
Junction temperature	T_j	T_{ja}
Maximum temperature	T_{max}	T_{maxa}
Average temperature	T_{ave}	T_{avea}
Minimum T_j	T_{min}	T_{mina}
Temperature variation	ΔT_j	ΔT_{ja}

Assuming V_{th} shift does not happen during the whole cyclic test process, the average heating power P_{cs} and related ΔT_j can be kept as constant in case of fixed load current I_{load} and duty ratio:

$$\Delta T_j \propto P_{cs} = V_{cp}(V_{th}, T_j)\cdot I_{load} \quad (4).$$

Hence, despite V_{bw} increases with the number of cycles, the thermo-mechanical stress on the bond wires is constant because of the fixed heating power Pcs and related ΔT_j. Accordingly, the thermo-mechanical stress arising at the interface between the bond wire and the SiC die surface can be expressed as [25]

$$\varepsilon_t = L_{bw}(\alpha_{AL} - \alpha_{SiC})\Delta T_j \quad (5).$$

Where, L_{bw} is the length of bond wire joint, and are the coefficients of thermal expansion of aluminum material and SiC, respectively.

D. Problem Statement Considering V_{th} shift

As mentioned in (4) and (5), the desired thermo-mechanical stress in power cycling tests is determined by the conduction power loss P_{cs}. Once the die degradation happens, the related thermo-mechanical stress varies with the on-state voltage changes. The corresponding ΔT_j and propagation mechanism considering V_{cpa} changes are depicted in Fig.4. The corresponding definitions are also listed in Table I.

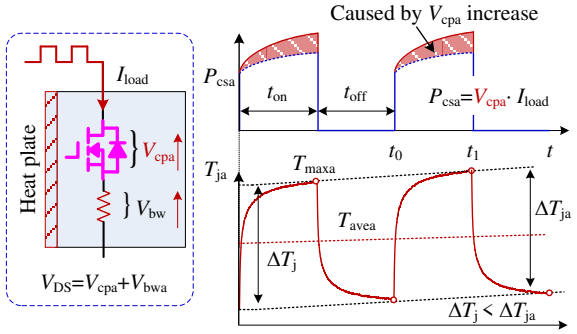

Fig.4. Temperature swing and spreading in condition of V_{th} shift onset.

Firstly, the higher P_{cpa} caused by V_{cpa} increase can raise the temperature variation ΔT_{ja}, so that the bond wires suffer from a more serious thermo-mechanical stress under the constant I_{load}. Furthermore, the maximum temperature after die degradation T_{maxa} can accelerate V_{th} shift process under the same gate bias voltage V_{gs}. Therefore, the subsequent P_{cpa} increase caused by the positive V_{th} shift can lead to the propagation on the temperature and thermo-mechanical stress. The SiC MOSFETs under test can get into a state of positive feedback loop based on SiC die and bond wires. Finally, both V_{cpa} and V_{bw} increase steadily with the number of cycles due to the occurrence of gate degradation and V_{th} shift.

Since there is no standard power cycling test procedure for SiC MOSFET modules so far, the conventional Si-based test methods are often adopted to the emerging SiC MOSFETs. In this scenario, the conventional failure criterion for Si-based MOSFETs based on 5% to 10% increase of V_{DS} or die resistance R_{on} in [26]–[29] cannot be applicable for SiC MOSFET modules. Therefore, it is necessary to measure the separate voltage drops on the bond wires and SiC MOSFET dies for the failure identification.

III. Independent Testing and Monitoring Method

A. Module under test

The studied planar SiC power MOSFETs are from VISHAY (1.2 kV/20 A). It is an H-bridge module with the conventional wire-bonded package. The module appearance with a PCB adaptor and the internal equivalent circuit are depicted in Fig.5. Accordingly, DC_{P1} and DC_{P2} are the positive bus terminals, DC_{N1} and DC_{N2} are the negative bus terminals, and OP_1 and OP_2 are the output terminals. (g_1,s_1), (g_2,s_2), (g_5,s_5), and (g_6,s_6) are the gate driver terminals for the internal four SiC dies, respectively. During the conduction period, the large DC current through the PCB board results in a considerable voltage drop across the parasitic resistance. Hence, the auxiliary measurement terminals K_{s1}, K_{s2}, K_{s5}, K_{s6}, K_{o1} and K_{o2} are introduced to exclude the parasitic voltage drop on the PCB boards. Furthermore, in order to observe the junction temperature variation, the optical fibers can be inserted into the modules through the four holes, as shown in Fig.5 (b). Referring to Fig.5 (c), R_{bw1}, R_{bw2}, R_{bw5} and R_{bw6} represent the bond wire resistances between the power source terminals and gate

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auxiliary sources. Since the power bond wires are regarded as the most vulnerable part, the solder contact resistance and copper resistance are neglected and not shown in Fig.5 (c). With the aid of external auxiliary measurement terminals, both the die voltage drops (V_{cp1}, V_{cp2}, V_{cp5} and V_{cp6}) and the bond wire voltage drops (V_{bw1}, V_{bw2}, V_{bw5}, and V_{bw6}) can be measured separately.

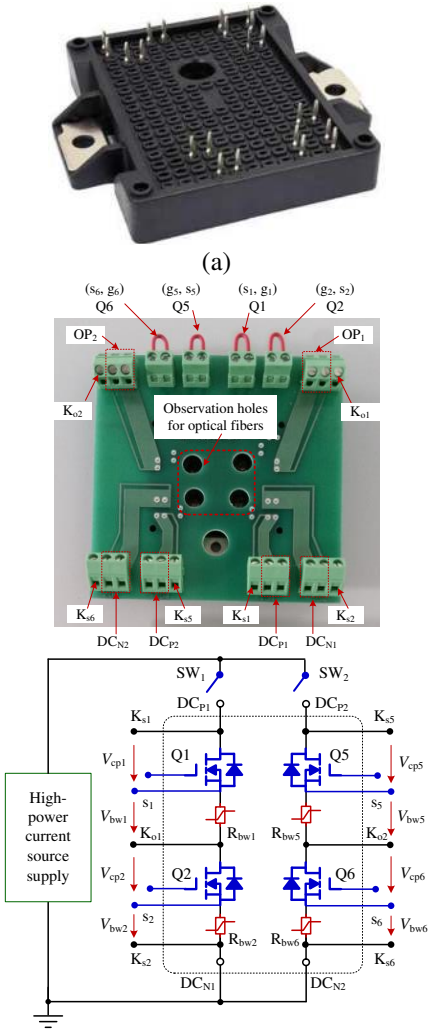

Fig.5. Schematic of power cycling test system. (a) Appearance of SiC MOSFET power module. (b) Appearance of module under test with PCB adaptor. (c) Internal equivalent test circuit.

B. Independent die and bond wire voltage measurements

To demonstrate the independent measurement principle, the equivalent measurement circuit for single SiC MOSFET is redrawn in Fig.6. For each discrete die, there exists a Kelvin source connection (K_s) between the die source and output source terminal (S). Taking advantages of auxiliary K_s, the independent measurements are performed together during the on-state conditions. Therefore, the voltage difference between Drain terminal (D) and Ks represent the die voltage drop V_{cp}. Meanwhile, in case of constant I_{load}, the bond wire voltage V_{bw} and the related parasitic resistance can be calculated. Finally, the whole device voltage drop during conduction V_{DS} mainly consists of die voltage V_{cp} and bond wire voltage V_{bw}. The measurement board can be implemented by the low-voltage the operational amplifier circuit [30].

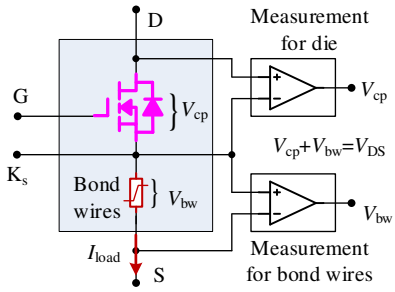

Fig.6. Schematic of independent on-state die and bond wire voltage measurement method.

C. Independent junction temperature measurement

Online T_j variation is regarded as an indicator for the thermal stress evaluation. In conventional power cycling test, T_j estimation is usually achieved by the thermal sensitive electrical parameters (TSEP) based methods [29], [31], [32]. However, only in case of the prerequisite intact die, TSEP-based methods are capable of T_j estimation by means of the initial calibration results. When the die degradation happens, the initial calibration data for the static-based TSEP methods can lead to the corresponding electrical measurement errors. Considering the potential V_{th} shift and related die resistance increase, the classical TSEP-based method is not appropriate for T_j estimation in the independent measurement method. The online T_j measurement without gel removal is achieved by the isolated optical fibers in this study. Hence, the online T_j measurement using isolated optical fiber is independent of the die degradation. The implementation of T_j measurement using optical fibers is shown in Fig.7. The part number of fiber is OTG-F-10 from Opsens with 5 ms response time [33]. In order to fix the optical fiber during operation, a displacement is used to hold the fiber vertically. With the help of graduated scale, the sensor of optical fiber can just contact the surface of die for online T_j measurement.

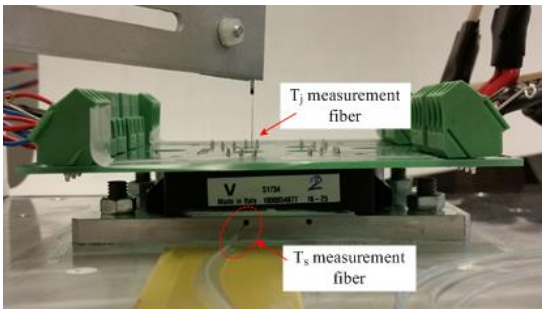

Fig.7. Implementation for online T_j measurement using optical fibers.

D. Configuration of experimental setup

According to the schematics shown in Fig.2, a conventional DC-based power cycling test platform is built, as demonstrated in Fig.8. The power cycling test system consists mainly of high-power DC supply (DELTA SM 45-140), external heating/cooling system (JULABO A40), high-precision oscilloscope (LECROY HDO6104-MS), fiber condition units (OPSENSE), isolated optical fibers (OTG-F-10), microprocessor controller (ALTERA DE2-115), isolated SiC gate drivers (CREE CRD-001) and auxiliary power sources.

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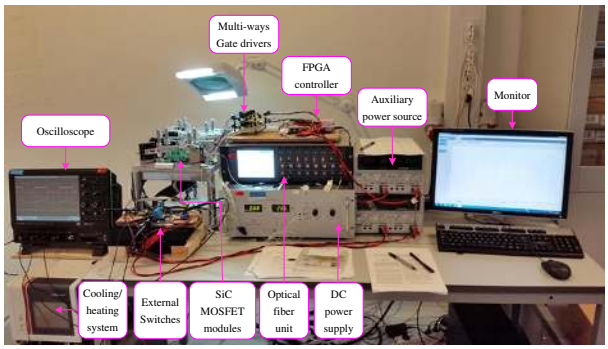

Fig.8. Appearance of power cycling test platform.

IV. Experimental Results

A. Test conditions

The power cycling test conditions for SiC-MOSFET modules are listed in Table II. Accordingly, the maximum T_j for each SiC die is around 175 °C, which is the maximum allowable T_j for the inspected SiC MOSFETs. The temperature variation ΔT_j is around 60 °C in the case of 2s on-state duration and 21.5A load current under fixed 105 °C of base plate temperature.

TABLE II. Test Conditions

Parameters	Value	Parameters	Value
Initial maximum T_j	175 °C	Base plate temperature	105 °C
Initial minimum T_j	115 °C	Constant load current	21.5 A
Delta temperature	60 °C	t_{on} / t_{off}	2s / 2s

This study is based on the power cycling test results with 24 SiC-MOSFET devices in 6 modules. During the test, four SiC devices in one same module are tested simultaneously under nearly the same test conditions. The test is stopped if the die voltage V_{cp} increases by around 15% from its initial value or the bond wire lift-off failure happens. Taking MOSFET #5 as an example, both the initial die voltage drop and bond wire voltage for Q5 and Q6 are depicted in Fig.9.

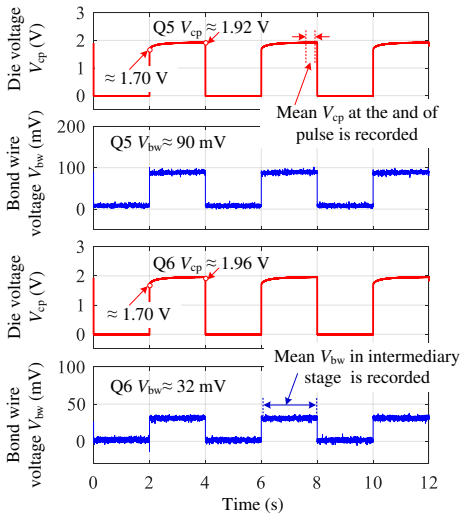

Fig.9. Initial on-state die voltage and bond wire voltage during power cycling test for MOSFET #5 module.

At the beginning of DC current pulse, the die voltages for Q5 and Q6 are about 1.70 V. Since SiC MOSFET is a unipolar device, the die resistance is sensitive to the junction temperature variation. As the increase of junction temperature, the on-state die resistance increases under the same I_{load} and V_{gs}. At the end of DC current pulse, the measured die voltages for Q5 and Q6 are around 1.92V and 1.96V, respectively. It is also worth noting that the bond wire voltage (V_{bw}) is independent of die resistance and T_j variation. Due to the low power dissipation on the bond wire, the minor self-heating effect plays a very slight role on the temperature coefficient of aluminum resistivity, the measured voltages on bond wires are flat under constant I_{load}. The initial bond wire voltages for SiC Q5 and Q6 are around 90 mV and 32 mV, respectively. Because of the internal layout design, the bond wire resistances for high-side devices (Q1 and Q5) are higher than the values of low-side SiC dies (Q2 and Q6) in one module [32].

Corresponding, the initial temperature variations for four SiC MOSFET dies without and with the independent V_{gs} regulation are depicted in Fig.10. In Fig.10 (a), the temperature variations under the same gate voltage (V_{gs}(Q1) = V_{gs}(Q2) = V_{gs}(Q5) = V_{gs}(Q6) = +20 V) are plotted. Since the tolerance deviation of static parameters can make a slight ΔT_j difference even under the same test conditions, the ΔT_j difference can be eliminated by appropriate gating voltage adjustment. Since the mean T_j and ΔT_j are regarded as two main factors account for the number of cycle to failure, the other thermal stress effect such as dT_j/dt does not need to be taken into consideration in this work.

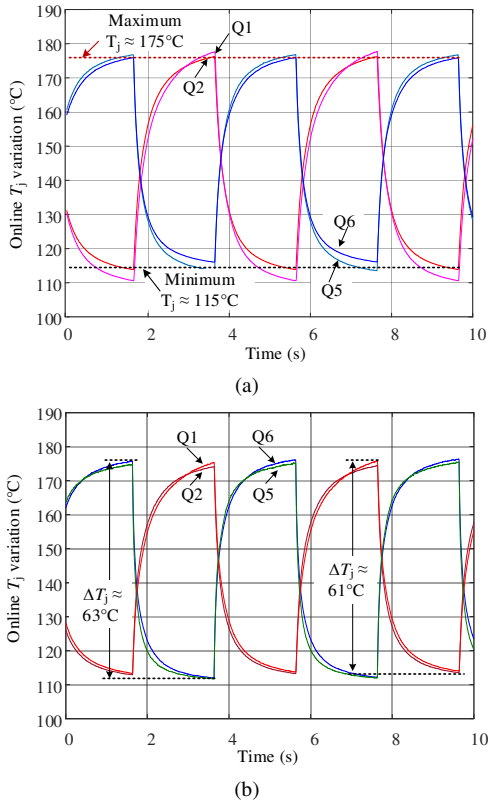

Fig.10. Initial T_j variation measurement results for MOSFET #5 module. (a) T_j variations using uniform V_{gs}=+20V. (b) T_j variations under independent V_{gs} adjustments.

As depicted in Fig.10 (b), with the independent gate voltage V_{gs} regulation for each SiC die, the measured T_j variation for each die meets the test requirement (115°C to 175°C). The

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maximum ΔT_j is around 63°C for MOSFET #5 (Q6) while the minimum ΔT_j is around 60°C for MOSFET #5 (Q2). Finally, the four SiC MOSFET dies are tested under the approximately equal ΔT_j at the beginning of the test.

B. Conventional bond wire lift-off failure

According to previous studies, the conventional bond wire lift-off failure is characterized by the abrupt die voltage increase at the end of the tests [28], [34]. In accordance with previous phenomenon, a typical bond wire lift-off failure in MOSFET #6 (Q5) is taken as an example. Both the die voltage V_{cp} and bond wire voltage V_{bw} against the number of cycles are plotted in Fig.11. Referring to Fig.11, it is worth noting that the die voltage abrupt increase is consistent with the bond wire voltage abrupt increase.

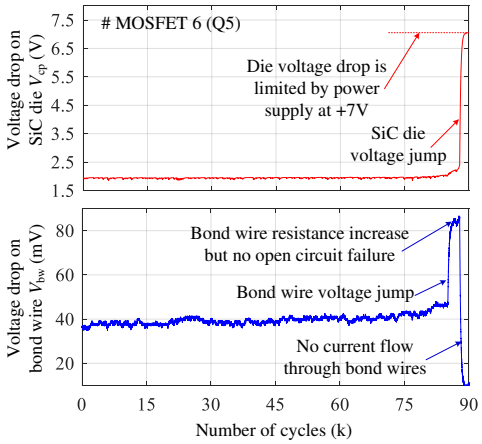

Fig.11. Open-circuit failure happens after around 88k cycles in power cycling tests.

It is also shown that the abnormal V_{bw} on bond wire happened before the abnormal V_{cp} change. This can be regarded as an evidence of the bond wire open circuit failure rather than die thermal runway failure. After the bond wire lift-off failure, there is no load current flow through the bond wires, so the measured bond wire voltage V_{bw} decreases rapidly. However, because the drain terminal (D) of MOSFET #6 (Q5) is connected to the positive output terminal of power supply, the die voltage V_{cp} is equal to the output voltage limitation of power supply (+7 V) after the open circuit failure. Remarkably, the peak value of V_{bw} after the abrupt increase is around 82 mV, which nearly doubles the initial value. Since the number of power bond wire for each SiC die is 2, the doubled V_{bw} means that one of the bond wires lift off from dies completely. Therefore, for the first abrupt increase on both V_{bw}, the open circuit failure can be identified by the separation measurement method.

C. Die degradation failures

Compared with the conventional bond wire lift-off failures, the SiC die degradation shows different aging trend within a shorter time. Because of the increasing die resistance, the related ΔT_j also expands with the number of cycles. The die voltage comparisons for MOSFET #5 (Q2) are recorded and plotted in Fig.12. In Fig.12 (a), the measured die voltage shows a significant successive increasing while the bond wire voltage increases slowly. According to the conventional failure criteria of 10% increase of V_{DS} (voltage from Drain terminal to Source terminal), it is assumed that the packaging failure occurs and the test should be stopped. However, the failure mechanism for MOSFET #5 (Q2) is mainly attributed to the die resistance increase instead of bond wire degradation. It implies that the aging rate of SiC die is much faster than the bond wire degradation under certain conditions, such as high temperature and high gate voltage bias. In Fig.12(b), the measured die and bond wire voltage comparisons before and after the test are depicted. At the end of the DC current pulse, about 170 mV increase on the die voltage compared with the initial value. However, around 15 mV increase of bond wire voltage compared with the initial value 80 mV. As a result, the die voltage increase is more noticeable in the test. Since the die resistance is proportional to the junction temperature, the die voltage difference between the beginning and end of the DC current pulse also expands. It also means that the real T_j is higher than the initial value at the end of the current pulse.

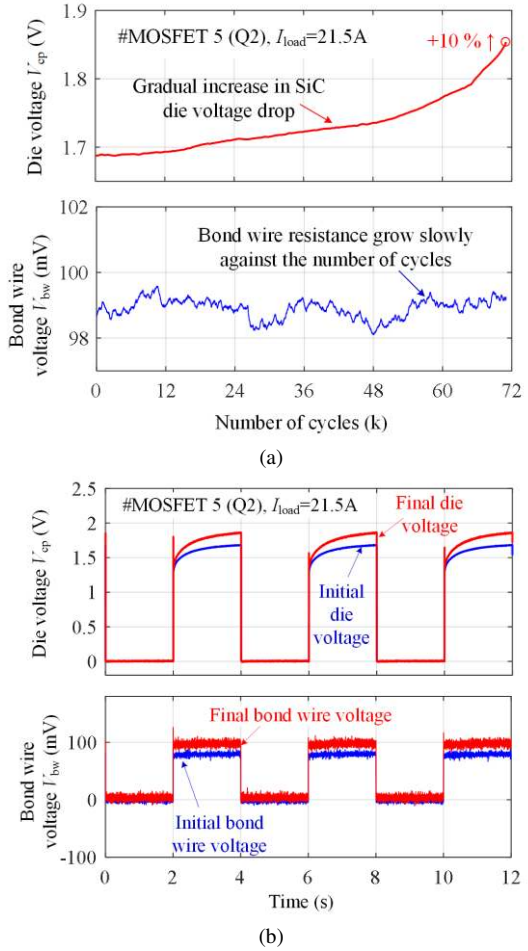

Fig.12. Die degradation in power cycling tests. (a) Aging curves for die and bond wire against number of power cycles. (b) Die voltage and bond wire voltage comparison before and after tests.

With the aid of Opsens fiber system, the changes of temperature variation against the number of cycles for MOSFET #5 (Q2) are recorded and plotted in Fig.13. At the beginning of test, the initial T_j can be kept in the range of 114 °C to 176 °C ($\Delta T_j \approx 62$ °C). After 25k cycles, the maximum T_j begins to slightly rise from 176 °C to 178 °C. Then after 56k cycles, the maximum T_j as well as ΔT_j increase obviously with the number of cycles. The measured maximum T_j is 181 °C and the related ΔT_j is 65 °C. Finally, with the acceleration of die

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degradation, the measured T_j is in the range of 118 °C to 190 °C ($\Delta T_j \approx 72$ °C) after 70k cycles. Compared with the initial T_j measurement, the maximum T_j has increased from 176 °C to 190 °C, and the corresponding ΔT_j increased 10 degrees after 70 k cycles' tests.

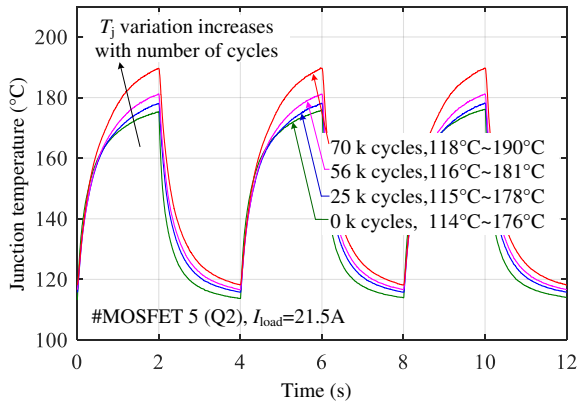

Fig.13. Junction temperature variation comparisons after different number of power cycles.

In the case of fixed testing conditions, the steadily increasing ΔT_j and the maximum T_j in the test can be mainly attributed to the increasing die resistance. Taking the advantages of independent die and bond wire measurement method, the die degradation progress against the number of power cycles can be monitored and recorded. In Fig.14 (a), 6 SiC MOSFET die aging curves with the steady die degradation are plotted. Unlike the open-circuit failures shown in Fig.11, there is no such phenomenon as an abrupt increase of die voltage after certain cycles. The on-state die voltages increase with the number of power cycles since the tests start. Therefore, there is another failure mode related to die degradation instead of bond wire degradation failure.

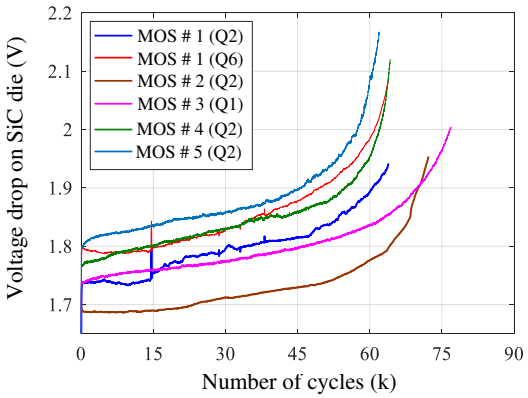

Fig.14. Power cycling test results with 6 die aging curves against the number of cycles.

V. Failure Analysis and Discussion

In order to validate the relations between die resistance increase and threshold voltage shift, the static characteristics of SiC MOSFETs before and after the tests are compared by means of the power device analyzer B1506A. All the static measurements and comparisons are carried out at 25 °C.

A. Comparison of aging electrical parameters

In Fig.15, the threshold voltage test results with different number of cycles for MOSFET #5 (Q2) are plotted. The drain current compliance for V_{th} determination is set to 1 mA. The measured initial V_{th} is around 2.79V, and then V_{th} continues to increase to 3.39V after 79k cycles and reach 3.56V at the end of test (84k cycles). The increasing V_{th} can be regarded as evidence that the increasing die resistance is related to the V_{th} shift. Furthermore, the V_{th} comparisons for the 6 SiC MOSFETs shown in Fig.14 (a) are depicted in Fig.16. The measured V_{th} after the power cycling tests are increased in varying degrees.

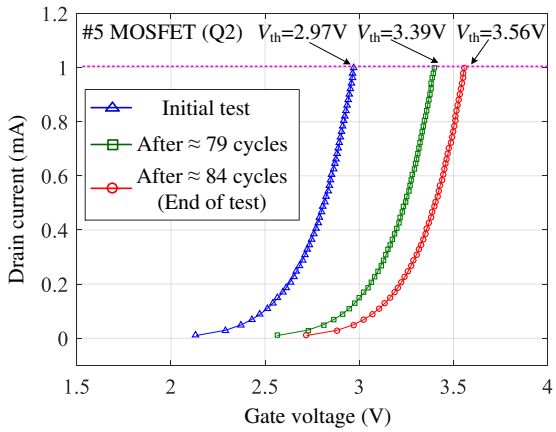

Fig.15. Threshold voltage measurement comparison for MOSFET #5 (Q2) under 25°C.

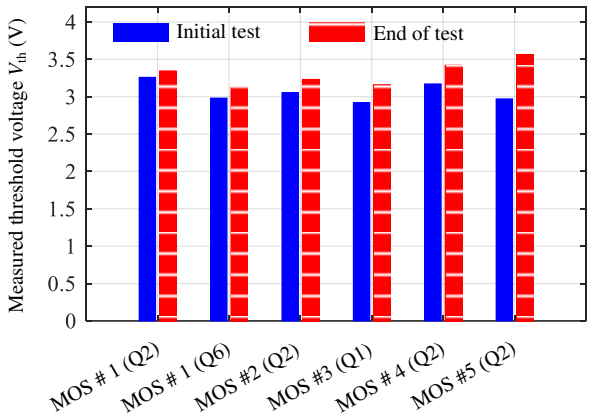

Fig.16. Threshold voltage comparison before and after power cycling test.

The threshold voltage measurement and comparison before and after the power cycling tests are listed in Table III. In the case of high-temperature cycling conditions, all the measured threshold voltages increased at varying levels after the tests. Since MOSFET #5 (Q6) and MOSFET #6 (Q5) were broken after the power cycling test, the subsequent V_{th} measurements are absent. The worst V_{th} degradation is MOSFET #5 (Q2). It is worth noting that there was no significant V_{th} shift after the power cycling tests for MOSFET #1 (Q2) at room temperature (25 °C). Many researches have studied and reported this kind of "reversibility" phenomenon [4], [35]–[37]. For the devices under gate bias at evaluated temperature, the additional oxide traps can be activated and then the V_{th} would be changed during the tests. Conversely, the oxide-trap activation would recover at room temperature without gate bias.

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Table III. Threshold voltage shift before and after power cycling test

Module Under Test	End of Test	ΔV_{th} for Q1 (V)	ΔV_{th} for Q2 (V)	ΔV_{th} for Q5 (V)	ΔV_{th} for Q6 (V)
MOSFET #1	≈78 k cycles	+ 0.1	+ 0.08	+ 0.2V	+ 0.14
MOSFET #2	≈90 k cycles	+ 0.3	+ 0.18	+ 0.17	+ 0.2
MOSFET #3	≈66 k cycles	+ 0.11	+ 0.15	+ 0.1	+ 0.11
MOSFET #4	≈70 k cycles	+ 0.07	+ 0.05	+ 0.15	+ 0.08
MOSFET #5	≈84 k cycles	+ 0.25	+ 0.59	+ 0.19	X
MOSFET #6	≈88 k cycles	+ 0.05	+ 0.05	X	+ 0.21

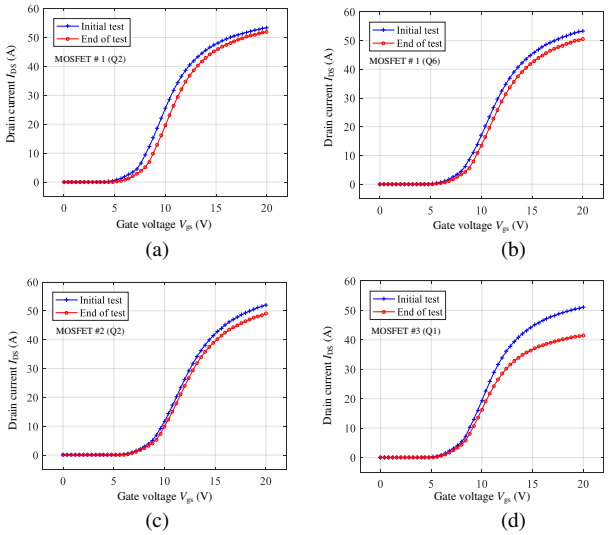
In order to further determinate the relations between the die resistance increase and positive V_{th} shift, the MOSFET transfer characteristics can be used for the die degradation investigation. The saturated MOSFET channel current is given by [21]

$$I_{DS} = \frac{Z\mu_{in}C_{OX}}{2L_{CH}}(V_{gs} - V_{th})^2 \quad (6).$$

Furthermore, in the saturated current regime of operation, the trans-conductance g_m can be expressed as

$$g_m = \frac{dI_{DS}}{dV_{gs}} = \frac{Z\mu_{in}C_{OX}}{L_{CH}}(V_{gs} - V_{th}) \quad (7).$$

Hence, in the case of fixed gate voltage V_{gs} and device parameters, the trans-conductance g_m can decrease with the increasing V_{th}. For the 6 SiC MOSFETs shown in Fig.14, the comparisons of transfer characteristic curves using device analyzer are depicted. Concerning the measurement results at the end of test, the measured I_{DS} saturation is lower than the respective initial value under V_{gs}=20 V. It is shown that MOSFET #5 (Q2) has the most serious V_{th} degradation after the test. Notably, the degradation on the transfer characteristic only proves the V_{th} shift effect on the external electrical parameters. The chip-level fatigue and the unexpected charges inside the oxide layer need Scanning Electron Microscopy (SEM) method for further investigation.



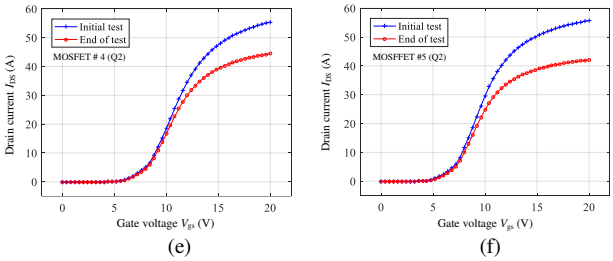


Fig.17. Transfer characteristic comparisons before and after power cycling tests at 25 °C.

B. failure mechanism of propagation and acceleration

The failure mechanisms during highly thermal test are depicted in Fig.18. At the beginning of test, the initial test conditions should be fixed according to the desired T_j variation. In the case of high-temperature operation and the immature gate oxide layer, the positive V_{th} starts to shift under high load current and positive gating voltage. The positive V_{th} shift during the test can result in the die resistance increase. Then, the increased conduction power loss caused by the die degradation can break the thermal equilibrium of the power cycling test. After that, two different types of failure mechanisms would happen.

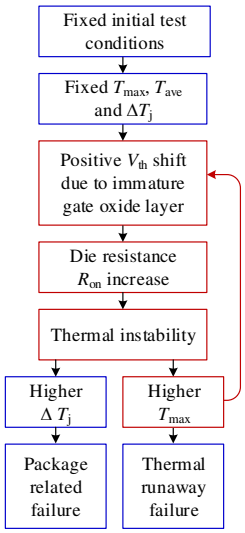


Fig.18. Two kinds of failure mechanisms during power cycling test considering V_{th} shift.

Since the increased die resistance can lead to higher ΔT_j, the package-level failure like bond wire lift-off can appear earlier than expected. On the other hand, the higher power loss caused by the die resistance increase can raise the maximum T_j. Then, the higher T_j can further accelerate the process of positive V_{th} shift. Finally, the inspected SiC MOSFET can be damaged because of the thermal runaway failure mechanism.

In summary, the first type failure mechanisms are the package related failures, such as the bond wire lift-off, solder layer delamination that can occur within a relatively short period of time. The degradation rate is proportional to the temperature swing ΔT_j. In case of the positive feedback loop, the initially fixed degradation rate would accelerate continuously. Secondly, with the propagation between the maximum T_j and positive V_{th}, the positive feedback loop leads to another die degradation mechanism. With respect to SiC MOSFETs, the

maximum operation junction temperature should be taken into consideration to avoid the underlying V_{th} shift effect. In practice, the second thermal runaway failure is the unexpected case in the power cycling test.

Regarding the aforementioned failure mechanisms in SiC modules, the maximum T_j limitation and V_{th} monitoring are of great importance to the reliability evaluation of SiC modules. The significant V_{th} shift and the related R_{on} increase can elevate the maximum T_j and accelerate the aging rate of package materials. Hence, the number of cycles to failure and the lifetime estimation method depend on both the package ruggedness and the threshold voltage stability of SiC MOSFETs. By taking advantages of the proposed independent measurement method, the voltage drops on die and bond wire can be measured and monitored during the long-term power cycling test.

In general, both the required current and power angle for three types of typical operation conditions in wind power generation are achieved by the emulator. Importantly, the internal T_j variation can be extracted during the experiments. With the help of equivalent testing method, both the T_j and T_{NTC} can be recorded and treated as a temperature protection criterion. Additionally, the safe operation area for power module considering T_j limitation can be determined in advance, and the power module and converter system can be protected by the related T_{NTC} at a low cost.

VI. Conclusion

The role of threshold voltage shift in the process of power cycling tests for SiC power MOSFETs has been studied. It is studied that the threshold voltage shift has significant impacts on the SiC die degradation during the tests. Furthermore, the die degradation caused by the threshold voltage shift can lead to a new failure mechanism instead of bond wire lift-off failure in power cycling tests. Since the conventional TSEP based T_j estimation methods can be affected by the die resistance change, the calibration could cause errors on the on-line T_j estimation. Hence, an independent T_j method using isolated optical fibers has been demonstrated in this study. Furthermore, with the advantages of auxiliary source terminal, an independent measurement method for separate die voltage and bond wire voltage has been proposed. It is validated that both the die and bond wire aging rates during the power cycling test can be monitored separately. As a result, this study enables to distinguish the die degradation failure from the bond wire lift-off failure in the power cycling tests. Finally, it has been studied that the die resistance could increase due to the successive V_{th} shift in the case of high temperature operation. The increased die resistance and corresponding elevated T_j can accelerate the process of V_{th} shift. It implies that V_{th} can be treated as a health indicator in power cycling test to identify the failure mechanisms. With the aid of device analyzer, the relations between V_{th} shift and die degradation have been validated. Furthermore, the aging transfer characteristics confirm the new die related failure mechanisms.

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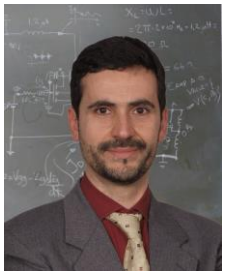

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