# Room temperature bonding of silicon and lithium niobate

M. M. R. Howlader[a] and T. Suga
*Institute for Advanced Microsystem Integration and Packaging, Research Center for Advanced Science and Technology, The University of Tokyo, 4-6-I Komaba, Meguro-ku, Tokyo 153-8904, Japan*

M. J. Kim
*Department of Electrical Engineering, University of Texas at Dallas, Richardson, Texas 75083-0688*

(Received 28 February 2005; accepted 21 June 2006; published online 19 July 2006)

The feasibility of wafer-level bonding was examined for silicon (Si)/lithium niobate ($LiNbO_3$) wafers by using a modified surface activated bonding process at room temperature. A low energy argon ion source of 80 eV energy with 3 A current was used, which was capable of sputter cleaning and depositing Fe nanolayers on the surfaces. Visual inspection showed that almost all of the 4 in. $Si/LiNbO_3$ wafers were bonded. The measured bond strengths were as high as 37 MPa but were inhomogeneous. This is due to the lack of uniform application of force over the surfaces (which are not parallel to the jigs) and the pulling angles during the pulling test. A 5 nm thick amorphous layer was observed across the $Si/LiNbO_3$ interface. Electron energy loss spectroscopy analysis confirmed the presence of Fe in the interfacial amorphous layer. This Fe-containing interfacial layer appears to be responsible for the high bonding strength observed between $Si/LiNbO_3$ at room temperature. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2229262]

Bulk micromachining has several advantages over surface micromachining such as tenfold lower electro-optic coefficients[1] and spontaneous ferroelectric polarization[2] in sputtered polycrystalline lithium niobate ($LiNbO_3$) films compared with those in bulk single crystalline $LiNbO_3$ wafers. In addition, increased light scattering and larger optical losses in waveguides caused by the grain boundaries in polycrystalline film,[3] in contrast to single crystalline $LiNbO_3$, reduce their utility in applications. Bonding of silicon (Si) and $LiNbO_3$ allows for ease of micromachining and high quality electrically sensitive thin films, as well as mechanically rigid diaphragms. For this reason, Si combined with $LiNbO_3$ is desirable for microelectromechanical systems (MEMS) devices such as pressure sensors, microfluidic devices, etc., and optical communication devices such as waveguides and optical data storage systems. To the best of our knowledge, no work has been reported on the wafer-level bonding of Si and $LiNbO_3$ at room temperature. Due to the van der Waals forces,[4] the chemically cleaned Si and $LiNbO_3$ wafers bond together after contact at room temperature. However, the bonding strength is very low. Therefore, the bonded interface cannot be used for practical applications. The coefficient of thermal expansion (CTE) mismatch between Si and $LiNbO_3$ is in the range of 188%–454% at room temperature. The CTE mismatch depends on the orientation of $LiNbO_3$. These CTE levels do not allow direct wafer bonding at high temperatures due to thermal stresses across the interface. The calculation for CTE mismatch was based on the reported literature CTE values of $2.6\times10^{-6}$/K and $[7.5(c\ \text{axis})-14.4(a\ \text{axis})]\times10^{-6}$/K for Si and $LiNbO_3$ respectively, at 25 °C.[5] The bonded wafers can fracture at temperatures higher than 150 °C. However, wafer thinning as well as long annealing cycle approaches have been reported to accommodate large CTE differences, but at the expense of high fabrication costs for devices.

Bonding at low temperatures of two or more smooth material surfaces with a high CTE mismatch was recently demonstrated using a room temperature surface activated bonding (SAB) process. This technique enables bonding of metals to metals, to semiconductors, and to ceramic insulators with low load or no load at room temperature. It is regarded as an enabling technology for room temperature wafer bonding of diverse wafers and can be used in the fabrication of micromachined devices such as pressure sensors and microvalves for fluid controls. In this process, smooth mating surfaces (rms $<2$ nm) were cleaned with either an argon fast atom beam (Ar-FAB), a low energy ion beam, or a radio frequency (rf) plasma in ultrahigh vacuum (UHV), which resulted in activated surfaces. This was followed by intimate contact of the wafers, which produced covalent solid-state bonding as a result of adhesion forces between surface atoms. The contact load applied during bonding was negligibly small for smooth surfaces.

Energetic ion sources were utilized for activating mating wafers prior to contact in the SAB process. Such energetic sources can change surface behavior and result in inhomogeneous polarization and charging states, which are controlled by the chemical and structural nature of the targets. Bonding failure of ionic wafers may be the result of the properties of the modified surfaces. To avoid such effects, the SAB process was modified so that the samples were sputtered using a modified hollow cathode ion source, capable of depositing 1–2 nm thick Fe layers and sputter cleaning the surfaces. In the modified SAB process, the ionic wafers were treated for a relatively longer time than that of the activation of wafers [30–60 s (Ref. 6) time require for Si surface activation] used in the parent SAB method, because prolonged treatment with the modified ion source can compensate surface polarization. Concurrent sputter cleaning and deposition of Fe were essential to control the nanolayers and the adverse effects of surface polarization. Therefore, Fe nanolayers are considered to be nanoadhesion layers. Another reason for using Fe as a source for nanoadhesion layers is the easy fabrication of the Fe ring and the important role of Fe as a dopant in in-

[a]Present address: Engineering Physics Department and Electrical and Computer Engineering Department, McMaster University, 1280 Main Street West, Hamilton, ON L8S 4L7, Canada; electronic mails: matiar@su.rcast.u-tokyo.ac.jp and mrhowlader@ece.mcmaster.ca

 

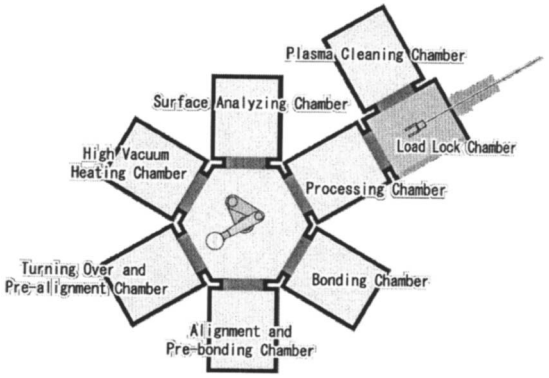


FIG. 1. Schematic diagram of a robot controlled 8 in. wafer-level SAB tool.

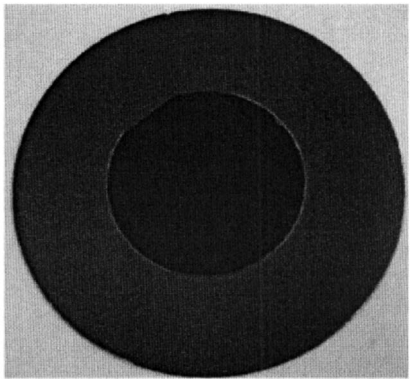

FIG. 2. Infrared transmission image of $Si/LiNbO_3$ bonded by the modified SAB process at room temperature.

creasing the refractive index in $LiNbO_3$ for light-wave applications.[7] Recently the modified SAB process was demonstrated with 8 in. Si and 5 in. glass wafers at room temperature.[8] This letter reports on the activation process and bonding mechanism of $Si/LiNbO_3$ at room temperature.

Mirror-polished single crystalline *c*-cut 4 in. $LiNbO_3$ and (100) 8 in. Si wafers were used for the bonding experiments. The thicknesses of the $LiNbO_3$ and Si wafers were 400 and 730 $\mu$m, respectively. Figure 1 shows the schematic diagram of a wafer-scale SAB tool used for the experiments. The SAB tool consists of eight chambers. The vacuum pressure is in the range of $10^{-8}$–$10^{-9}$ Torr for all chambers (Fig. 1). The tool accommodates 8 in. diameter wafers. We have developed a wafer carrier, which uses an 8 in. Si wafer to carry a 4 in. wafer. To develop a wafer carrier for $LiNbO_3$, four small pieces of Si, thinner than the $LiNbO_3$ being used, were placed in a rectangular convergent on the center of an 8 in. Si wafer with a distance slightly greater than the diameter of the $LiNbO_3$ wafer and bonded by the fusion bonding method. This tray cannot be used as a top carrier because the wafer is simply placed on the tray and it can be dropped when flipped over the wafer with the tray. Therefore, we placed the upper $LiNbO_3$ wafer on the top carrier with silver paste at the center of the 8 in. Si wafer to bond between the two $LiNbO_3$ wafers. The Si and $LiNbO_3$ wafers were loaded into the load-lock chamber and kept there until the vacuum pressure reached $10^{-7}$ Torr. The wafers were sputtered separately in the processing chamber by a low energy argon ion beam with a voltage of 80 V and a current of 3 A. This process simultaneously sputter cleans the samples and sputters Fe for deposition onto the samples. To produce the Fe deposition source, the hollow cathode surface was covered by a Fe ring. The accelerated radial ions in the discharged plasma may sputter Fe from the Fe ring surface and deposit Fe onto the sample surfaces during cleaning. The sputtering time for Si and $LiNbO_3$ was 10 and 20 min, respectively. $LiNbO_3$ was first cleaned for 18 min then cooled in the vacuum chamber of the tool, and finally cleaned for 2 min. The reason for cooling the $LiNbO_3$ wafer was to compensate the temperature increase to 200 °C, which occurs within 5 min of the start of the sputter cleaning. This temperature change was measured by a thermocouple placed on the back side of the wafer. The bonding between Si and $LiNbO_3$ without cooling $LiNbO_3$ resulted in fractures in the bonded samples because of the CTE mismatch at 200 °C. The Si wafer was transferred to the turning-over and prealignment chamber, turned over, and transferred to the alignment and prebonding chamber. The $LiNbO_3$ wafer was directly transferred to the alignment and prebonding chamber after sputtering. Bonding was performed in the alignment and prebonding chamber under a load of 50 kgf.

Figure 2 shows the infrared transmission image of $Si/LiNbO_3$ interface bonded at room temperature under 50 kgf. The entire area of $LiNbO_3$ was bonded completely. The SAB processed $Si/LiNbO_3$ interface had no macro- or microvoids, in contrast to that of the rf plasma or other direct wafer bonded interfaces. The void-free bonded interface can improve the performance of systems to be built by producing electrically and optically useful interfaces. Furthermore, we have recently integrated Si/Si wafers by the SAB, hydrophilic, hydrophobic, and radio frequency (rf) plasma processes at room temperature followed by annealing at identical conditions. The interfaces investigated by infrared transmission imaging showed that the numbers and sizes of voids/bubbles across the interface (which was due to the formation of hydrogen gas) were increased with an increase of annealing temperature in all processes except in the SAB process.[9]

Figure 3 shows the tensile strength distribution for a 4 in. bonded $LiNbO_3$ wafer bonded with an 8 in. Si wafer at room temperature. The bond strength was measured by a tensile pulling tester (AGS-1 kNG), which was made by Shimadzu Corporation. The bonded wafers were cut into $10 \times 10$ mm$^2$ pieces and attached to metal bars (jigs) with glue for the tensile pulling test. The tensile tester attempts to separate the bonded wafers by pulling metal bars adhered to

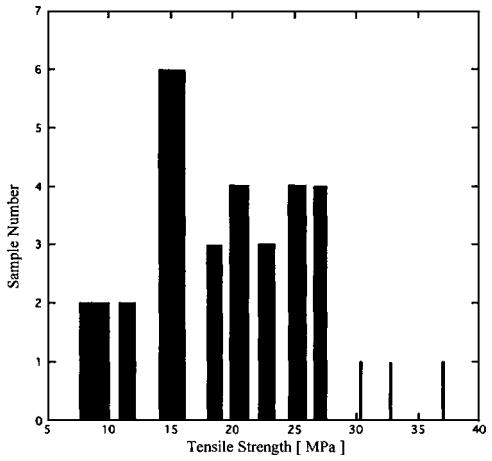


FIG. 3. Tensile strength distribution of 4 in. $LiNbO_3/8$ in. Si wafers bonded at room temperature. Diced samples of size $10 \times 10$ mm$^2$ were randomly picked for tensile tests.

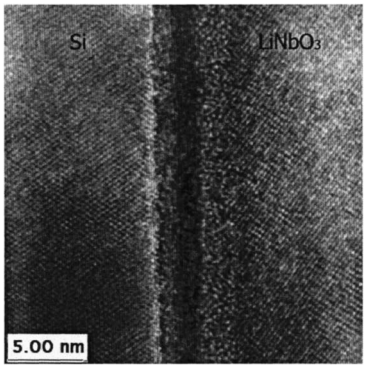


FIG. 4. HRTEM image of $Si/LiNbO_3$ bonded by the modified SAB process at room temperature. An amorphous layer with a dark crystalline Fe layer is observed across the interface. The observed lattice fringes are not as sharp as they can be because the crystal tilt for HRTEM imaging was optimized to mediate slight rotational misorientation of the bonded $Si/LiNbO_3$ pair.

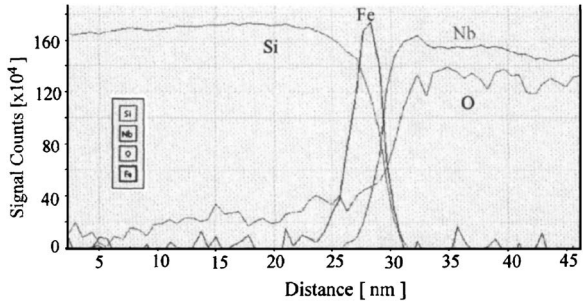


FIG. 5. Compositional distribution across the $Si/LiNbO_3$ interface by the EELS analysis. The upper left and upper right (red) lines show Si and Nb, respectively. The center of the interface is near the crossing of these two curves. The Fe curve is across the center, which looks like a Gaussian curve. The left and right sides from the center represent Si and $LiNbO_3$ wafers, respectively. The horizontal and vertical axes represent the distance across the interface (in nm) and the signal counts $\times 10^4$, respectively. The spatial resolution of the analysis shown is about 1 nm.

the bonded wafers from two opposite directions perpendicular to the bonded surfaces. The tensile pulling speed was 1 mm/min, and a computer controlled the pulling speed and the data acquisition. The results represent the bonding strength of 31 pieces of samples randomly taken from the bonded wafers after dicing. The tensile strength varied in the range of 8–37.5 MPa. Two samples fractured at the glue, i.e., where the jigs were attached and showed a tensile strength below 10 MPa. The other samples were fractured not from the glue and the bonded interface but from bulk materials of Si and $LiNbO_3$. The majority of the samples showed excellent bonding strength. In fact, the quantitative measurement of tensile strength is very difficult to obtain but can be partly improved by using mesa structures on wafers. A recent work on chip-scale $Si/LiNbO_3$ bonding showed the temperature limit of $Si/LiNbO_3$ to be 100 °C.[5] However, the worst bonding strength value of this study (i.e., 8.9 MPa) is identical to the best value of that study (i.e., 9 MPa). The activation source used in that study for chip-size $Si/LiNbO_3$ bonding was 1 keV Ar-FAB. The effect of chipping at the glue bonded interface of $LiNbO_3$ with other materials limits the fabrication of miniaturized waveguide devices. In order to investigate these chipping effects in this study, the bonded $Si/LiNbO_3$ wafers were diced into hundreds of chip-size pieces by using an automated dicing saw operated at the standard cutting speed for semiconductors. The diced interface was so smooth that we could not detect the bonded interface of $Si/LiNbO_3$.

Figure 4 shows the high-resolution transmission electron microscope (HRTEM) image of $Si/LiNbO_3$ bonded at room temperature. The observed lattice fringes are as sharp as they can be because the crystal tilt for HRTEM imaging was optimized to mediate slight rotational misorientation of the bonded $Si/LiNbO_3$. The low energy ion induced 5 nm thick amorphous layer was observed across the interface. A dark contrast region, probably crystalline Fe, was found across the interface. In order to investigate the elemental distribution across the bonded interface, an electron energy loss spectroscopy (EELS) analysis was carried out. Figure 5 shows the longitudinal EELS analysis for elemental distribution across the $Si/LiNbO_3$ interface bonded at room temperature. If one takes a look at the intersection of Si and Nb curves, one can see that there is little Fe on $LiNbO_3$ compared with Si. However, the irradiation time for the $LiNbO_3$ wafer was 20 min, whereas the irradiation time for Si was 10 min. Thus, the thickness of Fe on $LiNbO_3$ should be higher than that of Si. This might correspond to the lower projected range and implantation[10] of Ar and Fe in $LiNbO_3$ than that in Si. The highest Fe peak was seen near the center (of the interface), and the amount of Fe decreased progressively as one moves into the bulk materials both on the Si (left) and $LiNbO_3$ (right) sides. The EELS spectra showed lower Fe implantation/occupation to the lattice sites of $LiNbO_3$. Damage accumulation may be due to the randomly incorporated Ar and Fe. Also heating effects may be due to the implanted Ar and Fe ions in the wafers. The prolonged irradiation with low energy ion beam depolarized[11] the surface of $LiNbO_3$, which was needed for bonding with Si. The presence of Fe nanolayers was found to be supportive to strong bonding of $LiNbO_3$ and Si. Further investigation is necessary to clarify the specific role of Fe in the bonding process.

The authors would like to acknowledge Fuji Photo Films Co., Ltd. for supplying $LiNbO_3$ wafers and Eiji Okunishi of JEOL Ltd. for TEM assistance. The scientific discussion on the radiation damage of low energy ion source with Professor Emeritus Chiken Kinoshita, who is also a special professor of the Department of Applied Quantum Physics and Nuclear Engineering, Kyushu University, Japan, was greatly appreciated.

[1] G. Griffel, S. Ruschin, and N. Croitoru, Appl. Phys. Lett. **54**, 1385 (1989).
[2] T. A. Rost, H. Lin, T. A. Rabson, R. C. Baumann, and D. L. Callahan, J. Appl. Phys. **72**, 4336 (1992).
[3] M. Levy, R. M. Osgood, Jr., R. Liu, L. E. Cross, G. S. Cargill III, A. Kumar, and H. Bakhru, Appl. Phys. Lett. **73**, 2293 (1998).
[4] Q. Y. Tong and U. Gosele, *Semiconductor Wafer Bonding* (Wiley, New York, 1999), p. 17.
[5] H. Takagi, R. Maeda, N. Hosoda, and T. Suga, Appl. Phys. Lett. **74**, 2387 (1999).
[6] M. M. R. Howalder, T. Watanabe, and T. Suga, J. Vac. Sci. Technol. B **19**, 2114 (2001).
[7] K. Peithmann, A. Wiebrock, and K. Buse, Appl. Phys. B: Lasers Opt. **68**, 777 (1999).
[8] M. M. R. Howalder, H. Okada, T. H. Kim, T. Itoh, and T. Suga, J. Electrochem. Soc. **151**, G461 (2004).
[9] T. Suga, T. H. Kim, and M. M. R. Howalder, Proceedings of the 54th Electronic Conference and Technology Conference, Las Vegas, NV, 2004, p. 484.
[10] C. J. McHargue, Mater. Sci. Eng., A **253**, 94 (1998).
[11] H. Turcicova, J. Zemeck, J. Vacik, J. Cervena, V. Perina, M. Polcarova, and J. Bradler, Surf. Interface Anal. **29**, 260 (2000).