# Room temperature nanocrystalline silicon single-electron transistors

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Single-electron transistors operating at room temperature have been fabricated in 20-nm-thick nanocrystalline silicon thin films. These films contain crystalline silicon grains 4 – 8 nm in size, embedded in an amorphous silicon matrix. Our single-electron transistor consists of a side-gated 20 nm×20 nm point contact between source and drain electrodes. By selectively oxidizing the grain boundaries using a low-temperature oxidation and high-temperature argon annealing process, we are able to engineer tunnel barriers and increase the potential energy of these barriers. This forms a ''natural'' system of tunnel barriers consisting of silicon oxide tissues that encapsulate sub-10 nm size grains, which are small enough to observe room-temperature single-electron charging effects. The device characteristics are dominated by the grains at the point contact. The material growth and device fabrication process are compatible with silicon technology, raising the possibility of large-scale integrated nanoelectronic systems. © *2003 American Institute of Physics.*
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## I. INTRODUCTION

The development of materials such as nanocrystalline silicon (nc-Si),[1] consisting of crystalline silicon grains 10 nm or less in size, has raised the possibility of a dramatic increase in the functionality of the silicon chip. Recently, there has been considerable interest in the optical properties of the nanoscale grains, where light emission and amplification effects have been observed.[2,3] The grains ''naturally'' form silicon quantum dots over the entire area of the nc-Si thin film and it is possible that the electronic transport properties of the film are dominated by quantum confinement and single-electron charging effects,[4] complementing the optical properties. Advanced quantum and single-electron devices may be fabricated in these films without the need for lithographic definition of quantum dots, opening a promising route for the development of room-temperature nanoelectronics in large-scale integrated (LSI) systems.

One of the most promising devices for future nanoelectronic LSI is the single-electron transistor (SET).[5] In this device, the single-electron charging effect is used to precisely control the charging of individual electrons on a conducting island. Electrons are transferred to the island from source and drain terminals by tunneling across potential barriers. The charging of the island by a single-electron can be controlled by a gate terminal. The SET has the advantages of very low power consumption, better immunity from statistical charge fluctuation, and very high scalability compared to conventional complementary metal–oxide–semiconductor devices.

The practical application of SETs to LSI systems requires room temperature operation and silicon process compatibility. For room temperature operation, the single-electron charging energy of the island, $E_C = e^2/2C_\Sigma$ ($C_\Sigma$ is the total island capacitance and $e$ is the elementary electronic charge) must be large compared to the thermal energy $\sim k_B T \approx 26$ meV ($k_B$ is Boltzmann's constant and temperature $T = 300$ K). Therefore, the value of the $C_\Sigma$ must be $\sim 1$ aF or less and in practice this implies that the charging island must be $< 10$ nm in size.[4] In addition, electrons must be localized on the island, which requires a large tunnel barrier resistance as compared to the quantum resistance $R_Q \sim 26\,\mathrm{k}\Omega$ at the operating temperature. Thus far, there have been only a few demonstrations of silicon SETs operating at room temperature.[6–9] In these devices, the islands are formed either by discontinuous ultrathin polycrystalline silicon (poly-Si) layers, or are defined in crystalline silicon-on-insulator films using high-resolution lithography and controlled oxidation.

In nc-Si, sub-10 nm size islands exist naturally over the entire film area and do not require high-resolution lithographic definition. In our earlier work[10], we fabricated SETs operating up to 60 K in heavily doped *n*-type nc-Si where the grains were isolated by hydrogenated amorphous silicon grain boundaries. In this material, the energy barrier at the heterojunction between the amorphous silicon and the crystalline Si grains formed tunnel barriers up to 40 meV high. However, while the grains were sufficiently small (4 – 8 nm), the barrier height and tunnel resistance were too low for electron confinement at higher temperatures.

In this article we report the improvement of the tunneling barrier in nc-Si SETs by oxidizing the grains and grain boundaries, which results in room temperature single-electron charging effects.

## II. FABRICATION

We begin with a 20-nm-thick hydrogenated nc-Si film prepared by very high frequency (100 MHz) low-

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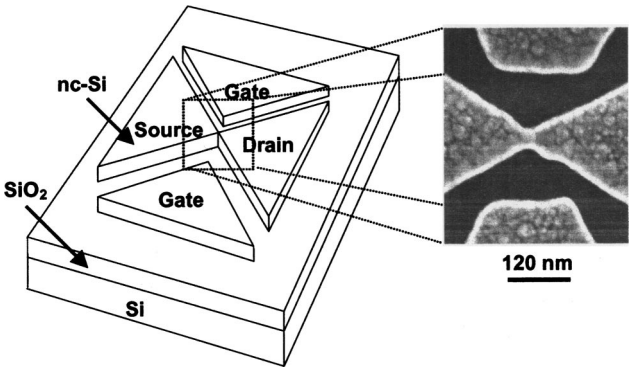



FIG. 1. A schematic diagram and a scanning electron microscopy micrograph of the point-contact device. The channel is 20 nm wide and 20 nm long. The gate-to-channel separation is 120 nm.

temperature plasma-enhanced chemical vapor deposition from a $SiF_4:H_2:SiH_4$ gas mixture. The use of $SiF_4$ increases the crystalline volume fraction, determined by Raman spectroscopy to be ~70%. [10] The film was deposited at 300 °C on a 150-nm-thick silicon dioxide layer grown thermally on an *n*-type crystalline silicon substrate and doped *in situ* with $PH_3$ (1% diluted with $H_2$ and 2% $PH_3$ in $SiH_4$. The room temperature carrier concentration and electron mobility, estimated by Hall effect measurements, were found to be $1\times10^{20}/cm^3$ and $0.7\,cm^2/V\,s$, respectively. At this stage, transmission electron microscopy (TEM) and Raman spectroscopy indicated that the grains were typically 4 – 8 nm in size, embedded in an amorphous silicon matrix.

Our SETs are defined in this ''as-deposited'' film using electron-beam lithography with polymethyl methacrylate resist and reactive-ion etching in a mixture of $SiCl_4$ and $CF_4$ gases. Figure 1 shows a schematic of a device. The device is a $20\,nm\times20\,nm$ point contact defined between source and drain electrodes, with in-plane gate electrodes on either side. The point contact is isolated from the gates by reactive-ion etching of the intervening nc-Si film down to the buried silicon dioxide layer.

After defining the SETs, a low-temperature oxidation/high-temperature annealing process is used to oxidize the grain boundaries. This process is performed after defining the SETs in order to simultaneously passivate the surface states in the device. We oxidize the SETs at a relatively low temperature of 750 °C for 1 h. The devices are then annealed at 1000 °C for 15 min.

## III. RESULTS

Figure 1 shows a scanning electron micrograph of an oxidized/annealed device, where the nanoscale silicon grains are clearly visible. Microscopy of the SET before and after the oxidation/annealing process did not show significant change in the grain shape and size. Figure 2(a) shows a TEM micrograph of the nc-Si film as-deposited, and the inset shows a (111) lattice image of a grain approximately 8 nm in size. Figure 2(b) shows a cross-sectional TEM micrograph of the nc-Si film after the oxidation/annealing process. The grains remain 4 – 8 nm in size but the film is reduced by approximately 5 nm in thickness due to the formation of

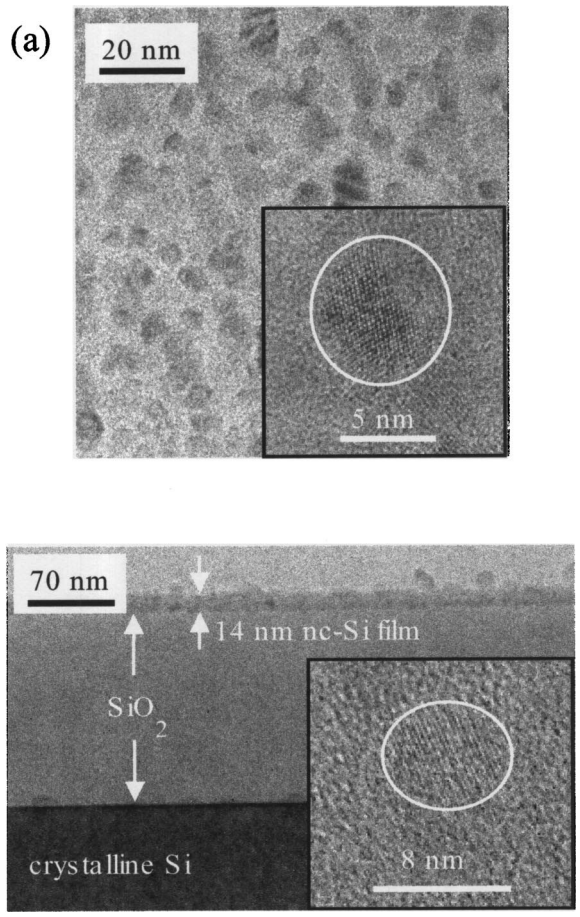



FIG. 2. (a) Transmission-electron micrograph of the nc-Si film as-deposited. The inset shows an atomic resolution image of a grain ~8 nm in size. (b) Cross-sectional transmission electron micrograph of the oxidized / annealed nc-Si film. The film is 14 nm thick, less than the as-deposited film thickness by 5 nm. The inset shows an atomic resolution image of a grain ~6 nm in size.

surface oxide. The inset shows a (111) lattice image of a grain approximately 6 nm in size. The grains are separated by amorphous regions ~1 nm thick, which we postulate to be silicon oxide layers formed by the oxidation/annealing process (to be discussed later). It should be noted that encapsulation of the grains with the silicon oxide would prevent any grain growth during annealing, which would otherwise increase the SET island size and lower the operating temperature.

nc-Si films created by silicon implantation in a silicon dioxide matrix have been reported previously.[3] However, the silicon dioxide regions in these films can be comparatively wide, which may reduce the film conductivity. In our films, ~1-nm -thick silicon oxide layers are grown by postdeposition thermal treatment of the film. The crystalline volume fraction remains high and the formation of the silicon oxide layers does not reduce the film conductivity dramatically. Our film is also continuous, unlike the approximately 3-nm-thick discontinuous polycrystalline silicon films used previously for room-temperature SETs.[6] This implies that high drain-source voltages are not required for device operation.

The nc-Si SETs were characterized electrically from 23 to 300 K. The source-drain current ($I_{ds}$) was measured with

respect to the source-drain voltage ($V_{ds}$) and the gate voltage ($V_{gs}$) and single-electron effects were observed over the entire temperature range. The device characteristics were stable to repeated temperature cycling over a period of 2 weeks. Figure 3(a) shows the $I_{ds}-V_{ds}$ characteristics of a device at 77 K. At $V_{gs}=1$ V a Coulomb gap of $\sim 100$ mV is observed, periodically modulated as $V_{gs}$ increases. Figure 3(b) shows single-electron current oscillations in the $I_{ds}-V_{gs}$ characteristics at 77 K. The oscillation period is 3 V. In these characteristics, $V_{ds}$ increases from $-50$ to 50 mV in 5 mV steps. We observe a single period oscillation, which may be associated with a single dominant charging island. The increase in the background current with gate voltage, similar to SETs fabricated in crystalline silicon, may be explained by a metal–oxide–semconductor field effect transistor-like field effect.[11] We note that while quantum confinement effects are a strong possibility in nanocrystalline silicon materials, we do not observe clear evidence of this in the temperature range of our $I-V$ characteristics.

Figure 4 shows the temperature dependence of the current oscillations, which persist up to 300 K with an unchanged period. However, there is a fall in the peak-valley ratio as the temperature increases due to a thermally activated increase in the tunneling probability. There is a small shift of $\sim 0.4$ V in the peak positions towards lower values of $V_{gs}$ as the temperature increases from 23 to 300 K. A zero-bias nonlinearity corresponding to the Coulomb gap persists in the corresponding $I_{ds}-V_{ds}$ characteristics at 300 K. We have fabricated devices in three independent processing runs and observed similar behavior in all point contacts narrower than 30 nm. We note that our devices are fabricated in the laboratory and improvement of the characteristics may be possible in a process-line environment.

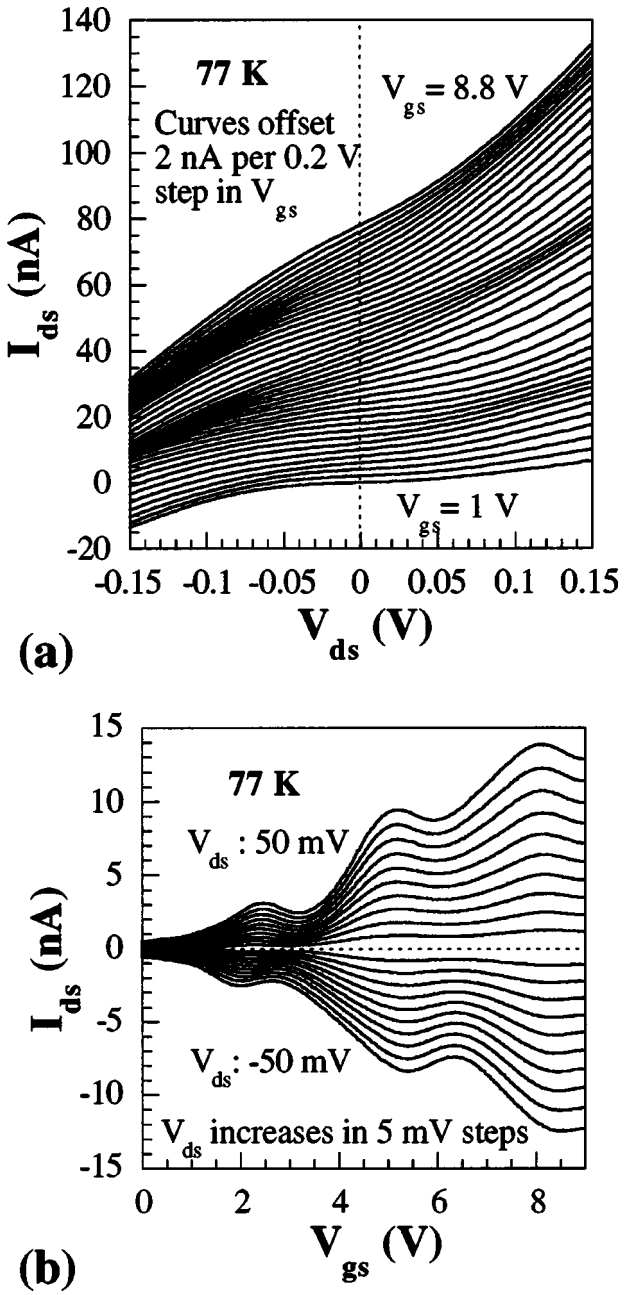
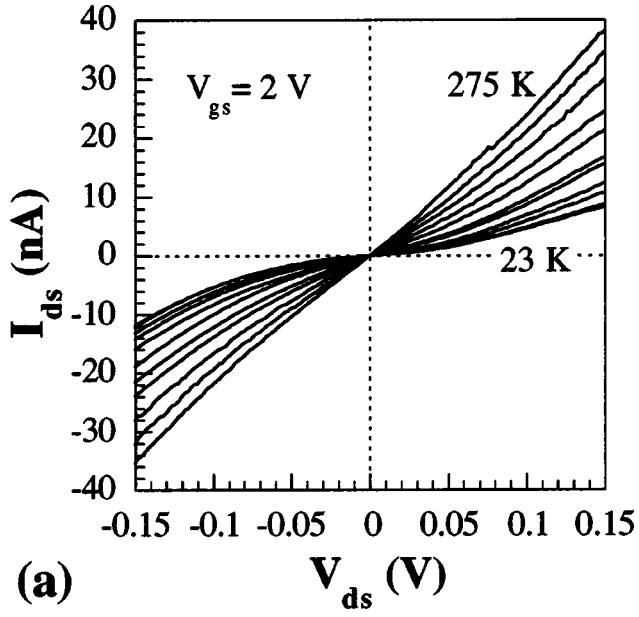



FIG. 3. (a) $I_{ds}-V_{ds}$ characteristics of device at 77 K. The Coulomb gap is modulated by applied $V_{gs}$. $V_{ds}$ is swept from $-150$ to 150 mV while $V_{gs}$ is swept from 1 to 8.8 V. Each curve is offset by 2 nA per 0.2 V step in $V_{gs}$ for clarity. (b) Gate-bias sweep of device at 77 K with current oscillation period of $\sim 3$ V.

## IV. DISCUSSION

We can estimate the size-of the charging island from our electrical characteristics.[12] The Coulomb gap $V_c=2e/C_\Sigma \sim 100$ meV is obtained from Fig. 3(a), implying a total island capacitance $C_\Sigma=3.2$ aF. The island-gate capacitance $C_g=e/\Delta V_g=0.05$ aF, where $\Delta V_g=3$ V is the current oscillation period obtained from Fig. 3(b). The total island capacitance $C_\Sigma=2C_t+C_g$, where $C_t$ is the tunnel junction capacitance between the source and the island or the drain and the island. Here we assume equal tunnel capacitances as we do not observe a Coulomb staircase. The relation implies that $C_t=1.6$ aF. We now assume a simple parallel plate capacitor model for the intergrain capacitance, where the grains are separated by a $SiO_2$ grain boundary $\sim 1$ nm thick. The charging island size is then $\sim 8$ nm, in agreement with the grain size observed in Fig. 2. These results support the idea that the charging islands are the naturally formed nanocrystalline silicon grains and the tunnel barriers are grain boundaries. We note that although there may be 2–3 grains in a 20 nm long point contact, our device characteristics are dominated by a single grain. This is possible because not all grains have tunnel barriers resistive enough for single-electron charging effects at high temperatures. We have observed multiple current oscillation periods in the $I_{ds}-V_{gs}$ characteristics in some devices at 4.2 K and these may be associated with more than one charging island, each with a different island-gate capacitance.

The properties of the tunnel barriers are investigated using Arrhenius plots of the device conductivity as a function of the inverse temperature. As it is difficult to extract the barrier height from the slope of the Arrhenius plot if the carrier transport is controlled by the tunnelling, we use a wider point-contact in which the single-electron charging effects terminate at $\sim 100$ K. Figure 5 shows the conductivity of a 40 nm wide point contact, outside the Coulomb gap. In this comparatively wide point contact, parallel conduction



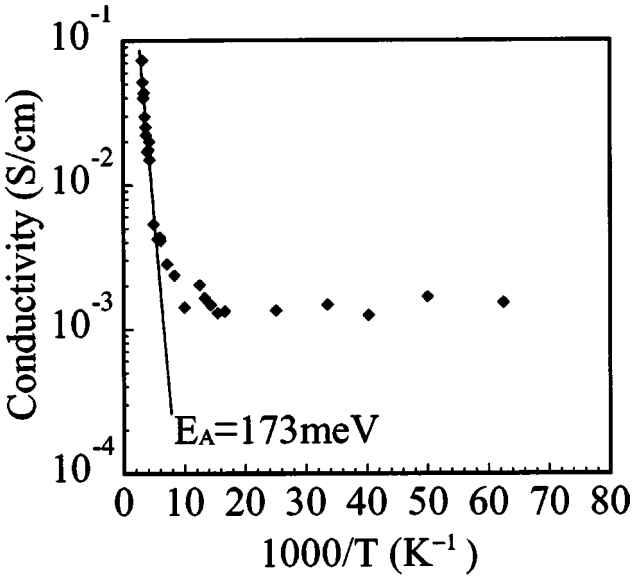




FIG. 5. Arrhenius plot of device at $V_{ds}=-140$ mV. $E_A$ is the activation energy.

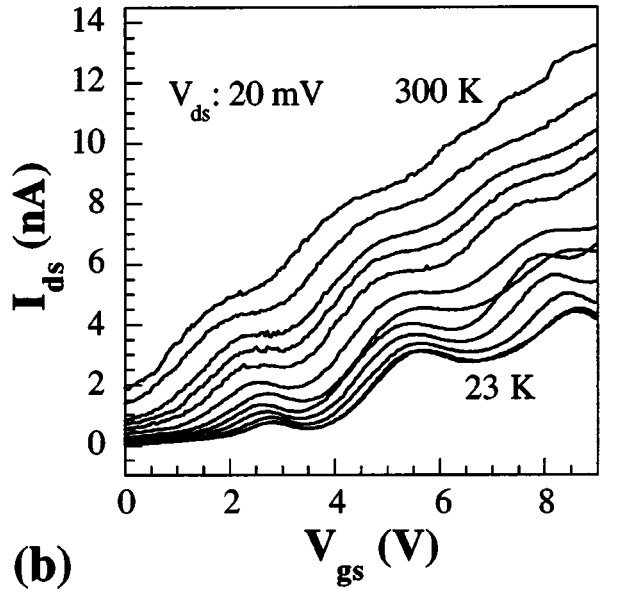



FIG. 4. Temperature dependence of (a) $I_{ds}-V_{ds}$ characteristics. $V_{ds}$ is biased at 20 mV and $V_{gs}$ is swept from 0 to 9 V. (b) Temperature dependence of current oscillations. $V_{ds}$ is swept from $-150$ to 150 mV and $V_{gs}$ is biased at 2 V. The first plot is obtained at 23 K and the next plot is measured at 50 K. Subsequent plots are measured at 25 K intervals.

paths through the grains are possible and single-electron effects persist only up to 100 K. A transition is observed in the gradient of the Arrhenius plots at this temperature. Below 100 K, the plots are almost independent of inverse temperature and this behavior can be associated with electron tunnelling through grain boundary potential barriers.[13] Above 100 K, the conductivity of the device increases logarithmically with inverse temperature due to thermally activated carrier transport over the potential barriers. Here, the gradient of the plot would correspond to the highest potential barrier along the carrier transport path. A potential barrier height of 173 meV can be extracted from this gradient. We may compare this value to our earlier work on SETs in as-deposited nc-Si films,[10] where we observed a maximum barrier height of 40 meV. The increase in the barrier height in oxidized/annealed SETs may be associated with the formation of oxide layers at the grain boundaries. We note that in crystalline silicon SETs formed by oxidized nanowires,[14] it is believed that the reduced width of the silicon nanowire region can produce potential barriers, while compressive stress at the $Si-SiO_2$ interface can reduce the band gap, lowering the bottom of the conduction band and producing a potential well which forms the charging island. In our system, grain-boundary potential barriers exist already, and it is difficult to ascertain the additional influence of stress associated with our oxidation and annealing process.

Oxygen incorporation in the oxidized/annealed nc-Si film can be investigated by an oxygen depth profile measured by using secondary ion mass spectroscopy (SIMS) (Fig. 6). It is known that simple oxygen diffusion can be explained with a single complementary error function or Gaussian function depending on the boundary conditions.[15] However, the oxygen concentration profile shows a gradient change at a depth of $\sim 10$ nm, suggesting that there is more than one oxygen diffusion path. Since the amorphous silicon grain boundaries in the nc-Si film are less dense compared to the crystalline silicon grains, oxygen atoms may diffuse faster in these grain boundaries[16,17] and the oxygen profile in the deep region may then be associated with grain boundary diffusion.

The oxygen content due to diffusion from the top surface, $x$ in $SiO_x$, in a 20-nm-thick film is only 5%, which is too low for the formation of a good tunnel barrier. However, the oxidation also occurs from the two sidewalls of the narrow point contact. If we assume that the point contact is 30 nm wide and that the amorphous silicon layers (30% in volume fraction) are oxidized selectively, then the value of $x$ in the oxidized phase is estimated to be 0.67. This implies that

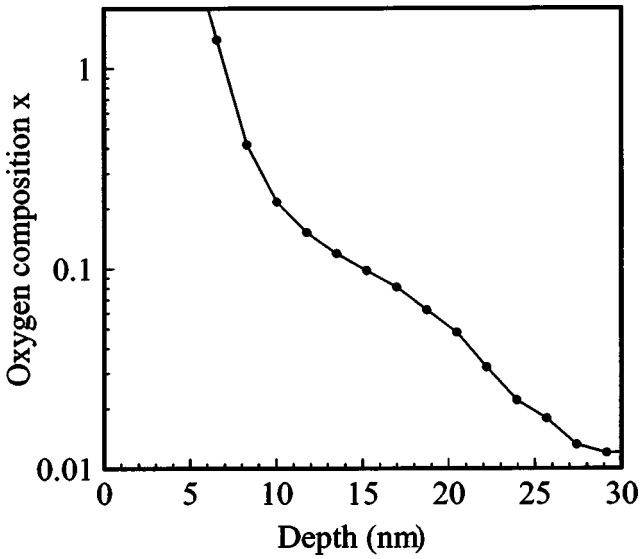



FIG. 6. SIMS oxygen depth profile for the oxidized/annealed nc-Si film.

silicon suboxide $SiO_x$ rather than $SiO_2$ is formed in the grain boundaries.[18]

We have also observed in a study using poly-Si point-contact devices that simple oxidation at 750 °C, i.e., without the postannealing, does not change the electrical characteristics significantly but that postannealing at 1000 °C in an Ar ambient increases the potential barrier height and the tunnel resistance.[18,19] It is known that thermal annealing of silicon suboxide induces phase separation into silicon and silicon dioxide, e.g., the process has been utilized to form nanocrystalline grains[20] or to fabricate ''separation by implanted oxygen'' substrates.[21] It is also reported that thermal annealing converts a partially oxidized $Si-Si_nO_{4-n}$ $(n<4)$ tetrahedral structure to $Si-O_4$ tetrahedral structure, confirmed by x-ray photoelectron spectroscopy.[22] On the other hand, there remain silicon rich phases $(Si-Si_nO_{4-n})$ after the thermal annealing at 1000 °C.

In our oxidized/annealed devices, the thermal annealing of the nc-Si film in an argon ambient at 1000 °C may form a more stable $Si-O_4$ tetrahedral structure locally at the atomic scale. This structure may have a large energy gap similar to the band gap of $SiO_2$. It also forms silicon or silicon-rich layers in the grain boundaries simultaneously. Such phase separation leads to the formation of parallel carrier transport paths at the grain boundary tunnel barrier. We speculate that the silicon/silicon-rich layers have energy gaps as low as the band gap of silicon, however, the electronic structure of these regions would be affected by the formation of the local $Si-O_4$ tetrahedral structure via the Coulomb potential caused by $Si^{4+}$ and $O^{2-}$ ions. These would increase the potential barriers around the silicon/silicon-rich regions. As we estimated the tunnel barrier height from the device conductance, this value reflects the minimum barrier height in the parallel paths through the tunnel barriers.

We believe that the tunnel barriers are made of silicon suboxide and the comparatively low device conductance originates from thin and low tunnel barriers. We have found that both low-temperature oxidation and high-temperature annealing are essential for room-temperature operation of our nc-Si SETs.

## V. CONCLUSION

This work demonstrates the operation of a nanoscale electronic device fabricated in nc-Si films. These films can be tailored chemically to obtain a sub-10 nm grain size along with a high crystalline volume fraction by choosing the proper chemistry in a plasma-enhanced chemical vapor deposition process. We have developed a low-temperature oxidation/high-temperature annealing process to selectively oxidize the grain boundaries and engineer tunnel barriers between the grains. We fabricate room-temperature SETs in the film, where the charging islands are formed naturally by the nanoscale grains. The devices are compatible with conventional silicon process technology, opening a possible route for nanoelectronics in LSI systems.

## ACKNOWLEDGMENTS

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