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Room temperature writing of electrically conductive and insulating zones in silicon by nanoindentation

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Conventional silicon devices are fabricated in the diamond cubic phase of silicon, so-called Si-I. Other phases of silicon such as Si-XII and Si-III can be formed under pressure applied by nanoindentation and these phases are metastable at room temperature and pressure. We demonstrate in this letter that such phases exhibit different electrical properties to normal (diamond cubic) silicon and exploit this to perform maskless, room temperature, electrical patterning of silicon by writing both conductive and insulating zones directly into silicon substrates by nanoindentation. Such processing opens up a number of potentially new applications without the need for high temperature processing steps. © *2011 American Institute of Physics*. [doi:10.1063/1.3549191]

Fabrication of conventional semiconductor devices and silicon circuits in particular requires substantial thermal processing, particularly following dopant introduction and for metallization. If it were possible to pattern and dope semiconductors at room temperature, without many of the current lithography and thermal processing steps, this may open up a number of new applications.

Diamond cubic silicon can transform to several different phases under the application of indentation pressure and some of these phases are stable at room temperature and pressure. For example, at a pressure of ~11 GPa diamond-cubic Si-I undergoes a phase transformation to the metallic β-Sn (Si-II) phase. During subsequent pressure release, the Si-II phase undergoes further phase transformations with the particular end phases dependent on the unloading conditions.[1–4] Two such crystalline end phases that can result from nanoindentation are so-called Si-XII (R8)[5] and Si-III (BC8).[6] A fine-grained (<100 nm grain size) polycrystalline zone composed of the mixture of these two phases is formed by slow unloading during nanoindentation. In previous studies, by the current authors, the volume ratio of Si-XII to Si-III has been found to be about 80% to 20% independent of indentation conditions.[3,7,8] Despite a lack of experimental data, these high pressure crystalline phases are expected to be electrically conductive since Si-III appears to be semimetallic[9,10] and recent theoretical studies have predicted Si-XII to be a narrow bandgap semiconductor,[10,11] although no experimental verification is yet available. Conversely, at very fast unloading rates an amorphous silicon (a-Si) end phase can result from nanoindentation[3,4] and this phase, despite the fact that electrical measurements have yet to made on it, is expected to be electrically insulating. Furthermore, these indentation-induced zones are relatively stable under ambient conditions.[1,3,12–14] In this paper we demonstrate that zones of Si-III and Si-XII are highly electrically conducting, whereas pressure-induced a-Si is insulating, leading to the ability to directly "write" conductive and insulating regions in crystalline and amorphous Si substrates by nanoindentation. These results are potentially significant for fabricating novel electronic device structures, in particular, for directly fabricating active devices at room temperature in silicon by a controlled indentation process without the need for conventional lithography.

Two types of sample structure were used to investigate the electrical conductivity of the zones of phase-transformed Si formed by nanoindentation. The first structure ("through-wafer") was fabricated in Czochralski grown single crystal Si(100) doped with boron to a resistivity of 10–20 Ω cm (background doping of $\sim 10^{15}$ cm^{-3}). A surface (insulating) amorphous layer (90 nm) was formed in the c-Si wafer by Si ion-implantation [see Fig. 1(a)]. Boron was implanted to a fluence of either 10^{14} or 10^{15} cm^{-2} into this surface amorphous layer (average concentration of $\sim 5\times10^{18}$ to 5×10^{19} cm^{-3}). Before indentation and electrical measurements, the a-Si layer was relaxed by annealing for 30 min at 450 °C, a step that was necessary to be able to induce phase transformations by nanoindentation.[3] Nanoindentation was performed to create a phase-transformed zone extending

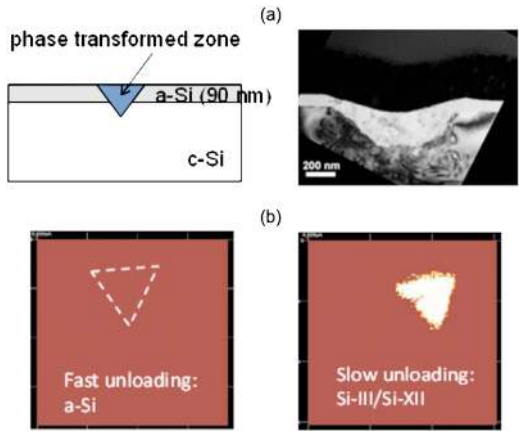

FIG. 1. (Color online) (a) Schematic and XTEM image of a phase-transformed zone formed through a thin surface a-Si layer in the through-wafer sample structures. The polycrystalline structure of a zone of Si-III/Si-XII formed using a spherical indenter is clearly visible in the XTEM. (b) Conductive AFM scans of indents made using a Berkovich indenter tip. Fast unloading is used to form a zone of pressure-induced a-Si. Also shown is slow unloading, where the end phase is Si-III/Si-XII and appears as the bright region in the conductive AFM scan.

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from the surface through the a-Si layer to the substrate [Fig. 1(a)]. The cross-sectional transmission electron microscopy (XTEM) image in Fig. 1(a) shows such a polycrystalline zone extending from the surface through the surface a-Si layer into the c-Si substrate. Here the zone is formed composed of Si-XII and Si-III (see introduction). The conductivity was probed in the vertical direction through a single indent either *in situ* via a conducting (boron-doped) diamond indenter tip or *ex situ* by conductive atomic force microscopy (AFM). The nanoindentation and *in situ* electrical measurements were performed on a Hysitron Triboindenter, Minneapolis fitted with the *nanoECR* system. These *in situ* electrical measurements have been described in detail elsewhere.[15]

Figure 1(b) shows conductive AFM scans over indents formed by slow and rapid unloading as an example of insulating and conductive regions created directly by pressing a Berkovich (shaped) indenter tip onto a Si surface. For fast unloading, a zone of pressure-induced a-Si is formed through the original a-Si layer. An insulating region is observed in the scanned area. In this case, the *in situ* electrical measurements achieved with the conducting tip confirmed that a phase transformation to the highly conducting Si-II phase occurred on loading and an insulating (a-Si) phase formed on unloading. In contrast, during slow unloading, a zone of Si-III/Si-XII is formed [similar to that shown in the XTEM figure in Fig. 1(a)], and a region of high conductivity is observed over the area of the indent. This simple demonstration illustrates the high conductivity of the zone composed of Si-III and Si-XII compared with the electrically insulating behavior of a-Si. Finally, *in situ* measurements with the conducting diamond indenter tip showed that the zones of Si-III/Si-XII formed by nanoindentation are at least three orders of magnitude more conductive than the surrounding a-Si.[16]

The second pair of structures was fabricated in silicon-on-insulator (SOI) wafers and as such these are referred to as the "resistive bar structures" (Fig. 2(a)). These structures allowed quantitative resistivity measurements to be made on zones of mixed phase Si-III/Si-XII or a-Si. The SOI wafer consists of a 180 nm crystalline, Czochralski grown, Si(100) layer (low level background doping of boron at $\sim 10^{15}$ cm^{-3}) on a 200 nm layer of SiO_2 on a crystalline silicon substrate. For measurements on zones of Si-III/Si-XII, heavily doped (p^+) contact pads (to facilitate low resistivity Ohmic contacts) were made to two sides of the structure by boron implantation of 30 keV to a fluence of 10^{15} cm^{-2}, followed by annealing at 900 °C for 30 min to activate the boron. A 20 μm wide strip of amorphous silicon (a-Si) was formed between the contact pads and extending to the buried SiO_2 layer, using Si ion-implantation. This a-Si layer was then relaxed by annealing at 450 °C for 30 min. In some cases, boron to fluences of 10^{14} or 10^{15} cm^{-2} at 30 keV was implanted into this a-Si strip. Thus the a-Si strip electrically isolates the two (contact) sides of the sample. A series of overlapping indents was then made across the a-Si strip to form a continuous bar of Si-III/Si-XII that electrically connects the two contact pads. Alternatively, for measurements on indentation-induced a-Si, a p^+ mesa structure was fabricated by patterning and etching down to the SiO_2 layer [see right hand schematic in Fig. 2(a)]. In this case a series of overlapping indents were made under conditions that formed an a-Si bar extending across the mesa to electrically isolate opposite contact regions of the mesa. Optical microscope

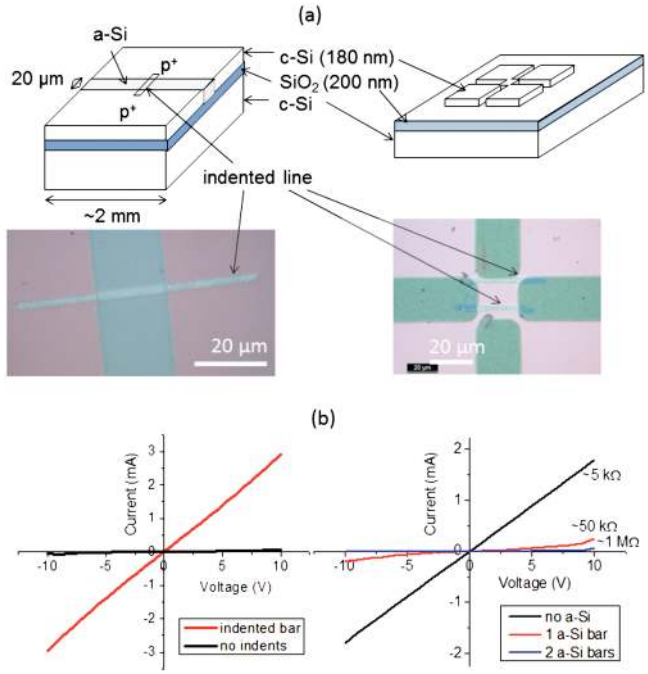

FIG. 2. (Color online) Summary of the resistive bar structures and results for measurements of Si-III/Si-XII and a-Si zones. Schematics (a) showing both the Si-III/Si-XII bar written across the a-Si strip (left figure) and the c-Si mesa structure into which the a-Si bars are written (right figure). I-V measurements (b) clearly show the low resistivity of the Si-III/Si-XII zone and high resistivity of the a-Si lines.

images of such lines across both the a-Si strip and c-Si mesa are also shown in Fig. 2(a). The indent-lines were made using an ultra-micro-indentation-system (UMIS) 2000, Australian Scientific Instruments Pty Ltd., Canberra with a spherical diamond indenter of ~ 10 μm radius. A maximum load of 200 mN was used for each indent which ensures phase transformation of a zone extending from immediately under the indenter contact to the SiO_2 layer. The indentation conditions were chosen to form either Si-III/Si-XII or a-Si zones. The zones of Si-III and Si-XII have the same polycrystalline structure and volume ratio of the two phases as those made for the through tip measurements (measured by Raman microspectroscopy previously—see introduction).[3,7,8,16] Thus, the cross-sectional area of the line is well defined (i.e., depth of 180 nm and width of ~ 4 μm). An I-V probe station was used to measure the resistance between the contact pads before and after formation of the bars of Si-III/Si-XII or a-Si.

Figure 2(b) shows the I-V characteristics extracted from the SOI resistance bar structure before and after indentation to form a line of Si-III/Si-XII material. The resistance of the Si-III/Si-XII bar can be estimated by applying a linear fit to the I-V curves in Fig. 2(b), giving resistance of ~ 1 MΩ for the entire a-Si strip before indenting, and ~ 3 kΩ for the 4 μm wide indented bar containing 10^{15} boron cm^{-2}. Hence, the resistivity of the bar is ~ 0.01 Ω cm, noting that the resistivity of the starting single crystal layer is 14–22 Ω cm.

Figure 2(b) also shows that an indentation-induced a-Si bar is effective at electrically isolating the c-Si contact pads across the mesa, with the resistance measured between opposite corners of the structure increasing by over an order of magnitude. This indicates that the pressure-induced a-Si, as

TABLE I. Summary of the electrical measurements made on the zones of Si-III/Si-XII and a-Si formed by nanoindentation. The conductivity of the Si-III/Si-XII zones increases with boron content. The nanoindentation-induced a-Si is electrically insulating.

Material	Details	Resistance
Conductive Si-III/Si-XII	$\sim 10^{11}$ B cm^{-2}	15–40 kΩ
	10^{14} B cm^{-2}	4 kΩ
	10^{15} B cm^{-2}	3 kΩ
Insulating a-Si	No bar	5 kΩ
	1 bar	50 kΩ
	2 bars	1 MΩ
	2 bars+annealing	25 MΩ

expected, is electrically insulating with respect to c-Si and the Si-III/Si-XII material. After indenting a second bar (effectively doubling the volume of a-Si), the resistance increases further to 1 MΩ. The increase in resistance is greater for the second a-Si bar than for the first. We attribute this to nonuniformities in the indented line which is formed by overlapping a series of indents (this can be seen in the optical image) and/or to the fact that the first line is at the mesa edge. Nevertheless, the resistance of the structure is increased by over two orders of magnitude by forming two narrow a-Si bars of total width around 8 μm. Annealing the indentation-induced a-Si at low temperature (300 °C) further increases the resistance to 25 MΩ, an overall increase of close to four orders of magnitude. This effect is similar to that in ion implanted silicon where annealing is known to cause structural relaxation, with a related decrease in the number of defects and dangling bonds in the amorphous network.[17]

Table I summarizes the resistance measurements made on the Si-III/Si-XII conductive bars and the insulating a-Si bars. The measured conductivity of zones of Si-III/Si-XII can be qualitatively understood in terms of what is already known about these phases. They are expected to be highly conducting given that Si-III formed in a high pressure cell was found previously to be a semimetal with an estimated hole concentration of around 5×10^{20} cm^{-3} (Ref. 9) and Si-XII is predicted to be a narrow bandgap semiconductor.[10,11] Indeed, the resistivity of the Si-III/Si-XII in our case is ~0.01 Ω cm, which is approximately five times higher than that of single crystal Si-I doped to the same level (0.002 Ω cm)[18] but comparable or lower than that of similarly fine-grained polycrystalline Si-I.[18,19] What is more difficult to understand is that the conductivity of the high pressure phases is increased with boron content in the a-Si prior to indentation. This suggests that boron is electrically activated in the mixed Si-III/Si-XII phases immediately following indentation. Based on the already high hole concentration in the Si-III phase, we believe that the dominant doping effect occurs in the Si-XII (semiconducting) phase. Further details of this aspect will be discussed in detail in a forthcoming publication on the electrical properties of Si-XII.[16] Suffice it to say here that the bar with the highest boron concentration exhibits good Ohmic behavior (see I-V characteristics in Fig. 2). This is consistent with high doping of the Si-XII phase where any internal electrical contacts between crystallites of Si-III and Si-XII in the mixed phase would be expected to be Ohmic, as would the contact between the Si-III/Si-XII zone and surrounding (p-type) crystalline Si-I. Conversely, the I-V characteristics of the lower boron concentration cases in Table I (not shown) exhibit Schottky behavior.[16]

It is worth noting that single step writing of nano- to microscale zones of Si-III/Si-XII and a-Si is possible using specially shaped indenter tips (e.g., a wedge indenter to write lines) and this approach could eliminate uncertainties in the exact composition of the phase-transformed zones associated with overlapping indents. This would provide more consistent electrical properties as variations in geometry and zone composition would be eliminated. Finally, the writing of conductive regions is not limited to zones composed of Si-III/Si-XII. It has been shown previously that low temperature annealing (≥200 °C) transforms Si-III/Si-XII back to polycrystalline Si-I.[7] Thus, indentation followed by a low temperature annealing step can allow patterning of polycrystalline Si-I.

In summary we have shown that zones composed of a mixture of Si-III and Si-XII, formed by nanoindentation, are highly electrically conducting compared to the electrically insulating behavior of a-Si formed by indentation. Furthermore the conductivity can be controlled by boron doping, which can be incorporated into active sites in the mixed Si-III/Si-XII phase by indentation at room temperature without the need for an annealing step. In principle, a range of pattern shapes and sizes ranging from nm to cm can be formed using appropriate indenter geometries and loading conditions. This opens up exciting possibilities for room temperature, maskless processing of silicon.

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