Router for Power Packet Distribution Network: Design and Experimental Verification

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***Abstract*—A power packet dispatching system is expected to be one of the advanced power distribution systems for controlling electric power, providing energy on demand and reducing wasted energy consumption. In this paper, power packet routers are designed and experimentally verified for realizing a networked power packet distribution system. While the previously developed router directly forwards the power packet to a load, the new router forwards the packet to the other router with an information tag reattached to the power payload. In addition, the new router can adjust the starting time for forwarding the received power packet to the other site, thus utilizing storage capacity integrated into the router. The results successfully clarify the feasibility of the power packet distribution network.**

***Index Terms*—Power packet, power distribution system, power routing.**

I. Introduction

RENEWABLE energy sources are in great demand as a means to reduce the use of fossil and nuclear fuels. Candidates for alternative energy sources include photovoltaic cells, fuel cells, wind generators, and sea wave generation. The amount of generated power is increasing. Power suppliers are preparing bulk of generations in accumulations. On the other hand, consumers are adopting apparatuses with high-efficiency power conversion systems to save energy. Using these apparatuses may be one strategy to reduce energy consumption. Expected innovations in the energy scenario also include the development of novel power distribution methods and of energy storage, as well as energy management based on demand.

In 1998, Toyoda et al. proposed the concept of an open-electric-energy network (OEEN), in which power flow is controlled by multiple electric-energy routers [1]. With this concept, electric energy is treated similar to a packet of mail tagged with information about the sender and receiver. Power routing makes it possible for many types of dispersed power sources to participate in an electrical power market without any disadvantages to existing power utilities and consumers. Based on the development of power electronics technologies, this concept was proposed before its time, unfortunately, and the system was never realized. Recently, however, wide-bandgap power semiconductor devices began to be produced, such as SiC and GaN. They have the potential to realize significantly lower switching power loss, higher frequency switching, and higher power capacity than Si power devices [2–4]. By extending the idea of the OEEN and applying these high-performance power semiconductor devices, we developed an AC power routing system and a DC power packet dispatching system with highly developed information and communications technologies [5–16]. The former is intended to realize a circuit matrix for establishing a power distribution circuit [5–10]. The latter is intended to realize a packet transfer in a network for electrical power distribution [5–7], [11–16]. Both systems are designed to integrate the information and power networks at the physical layer. The delivered power is labeled with the information tag attached to its power physically. Then, power flow on the power distribution network can be controlled according to the attached tag information, called the *routing of electric power*. In these systems, it is possible for power to flow from different sources to the objective load without being mixed even on the same power line. Basically, in the conventional system, electric power is automatically supplied to the load plugged into outlet. As is well known, the voltage and frequency of electricity delivered to each load are unified on the power line. These of the renewable energy should be converted into the rated ones to be delivered on the common power line. The systems are designed to accommodate each load's demand for appropriate electric power for a selected power source according to the quality of its energy without changing outlet. This is an energy on demand system such as that proposed in [17].

The power packet dispatching system uses a packet transfer in a network for electrical power distribution [5–7], [11–16]. The power packet delivers electric power according to the attached information tag superimposed on the voltage waveform. The configuration of a power packet and a conceptual diagram of a power packet distribution network are shown in Figs. 1 and 2, respectively. The details of the power packet and its dispatching system are explained in the following section. One of the rationales behind the power packet dispatching system is to realize a more intelligent DC power delivery system in which energy on demand can be adopted. Packetization is one possible method to achieve electric power routing in a discretized form. It is possible to reduce standby power consumption because the power flow can be managed flexibly. The identification of the electric power source is simultaneously achieved since the mixing of power from different sources can be avoided even on the same power line. This means that, in the power packet dispatching system, various qualities of power sources, e.g., whose voltages are different each other, can share the same power transmission line. Therefore, the number of the power line for power distribution can be reduced

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under the environment where several power sources supplying powers on different voltage level exist simultaneously. These are obviously impossible in the conventional power distribution system. This is the main challenge to address in a practical system.

In this paper, routers are designed for power packet distribution network, and these operations are experimentally verified. We have previously developed the router to verify the feasibility of power packet dispatching [11]. Power packetization was successfully examined, however, the router did not have a function to forward the received power packet to the other routers. This is because the information tag attached to the received power was lost at the point of transfer. The output of the router needed to be connected to the target load directly. (Note that the output port of the router can be selected from some choices according to the tag information of received power packet.) Therefore, in this paper, we developed a router that can reattach the information tag to establish a *networked* power packet distribution system. In addition, storage capabilities are integrated into the router for time management in forwarding the packet by temporarily holding the power of the received power packet. With this power packet distribution system, operations are executed without losing the origin information of the delivered power. We explain and experimentally verify the architectures of both routers, i.e., the new and previously proposed routers. A networked power packet distribution system can be constructed by these routers and Mixer which produces the power packet from a DC source explained later. The feasibility of a cascade network system is also experimentally examined. Hereafter, we call the previously proposed router *Router I* and the router proposed in this paper *Router II*.

This paper is organized as follows. In Sec. II, the concept of the power packet and its dispatching system is explained. In addition, the architecture of Mixer and Router I, as well as that of the previously examined power packet dispatching system, is also briefly explained. In Sec. III, we explain the newly designed architecture of Router II for the networked power packet distribution system. In Sec. IV, we discuss the operation of Router II and the feasibility of a cascade network power packet distribution system. Finally, we make our conclusion in Sec. V.

II. Power Packet and its Dispatching System

The structure of a power packet is depicted in the time domain as in Fig. 1 [7]. The payload corresponds to the power supplied by a selected power source. The amount of power supplied in a packet can be regulated, for example, by changing the length of the payload or modulating the payload, e.g., through pulse width modulation. The header and footer are physically attached as a tag to the payload. The tag contains several bits of information, such as the address of the source and destination load. The footer includes a mark at the end of packet. The electric power and information tag are transferred together in the packet in the same physical layer at the same velocity. This avoids any contradiction between the physical quantity and its information. Fig. 2 shows a conceptual diagram of power packet dispatching system. Multiple power sources and multiple loads are connected with this system. The mixers and routers that are linked in the system control the flow of the power packet on the power line network. Each of the sources, loads, mixers, and routers is assigned a unique individual address. The sources need to be connected to Mixers to convert DC power to the power packet. The loads are connected to the routers. Each router has functions to store the received power temporary and manage transfer timing.

In [11], a prototype power packet dispatching system was previously verified. Fig. 3 shows the configuration of that prototype system, which consists of one Mixer, one router i.e., Router I, two sources, and two loads. Figs. 4 and 5 show schematic diagrams of Mixer and its switch circuit, respectively. Multiple connection of the prototype Mixers is prohibited on the same line to avoid short circuit condition. The output port of Mixer needs to be connected to the input of the router. In addition, Figs. 6 and 7 show schematic diagrams of Router I and its switch circuit, respectively. Their details are explained in [7]. Briefly, the mixer and router are connected with a couple of electrical cables. The common clock signal is supplied from the mixer to the routers through a signal cable for achieving clock synchronization. On the prototype power packet dispatching system, the synchronization among

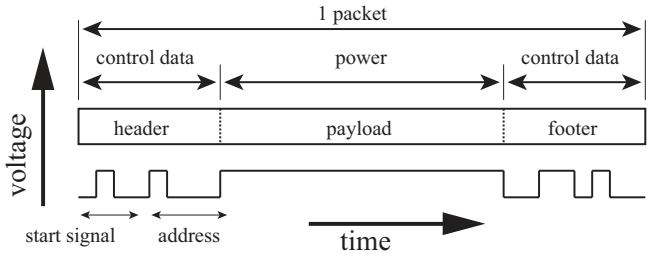

Fig. 1. Structure of power packet.

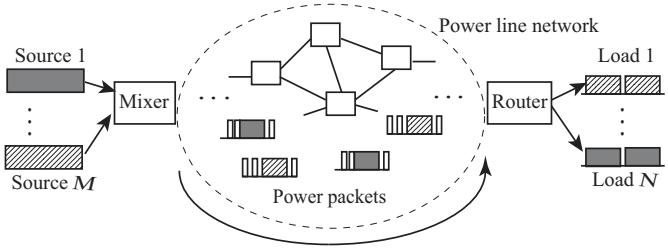

Fig. 2. Concept of power packet dispatching system.

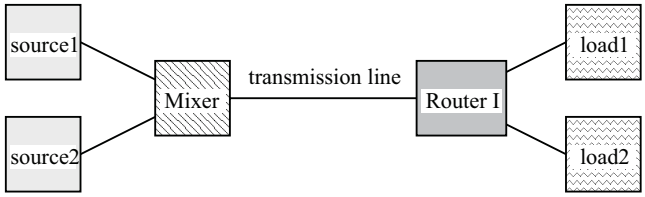

Fig. 3. Schematic diagram of a prototype system for power packet dispatching.

mixers and routers are necessary to read the bit information correctly. Since the power packets are dispatched with time-division multiplexing (TDM), it is possible to prevent the mixing of power from different sources even in the same power line. The capacity of a line is the same with the one in the standard impedance driven system. This is because the one power source occupies a power line to distribute its power packet while a time slot for its power packet is assigned.

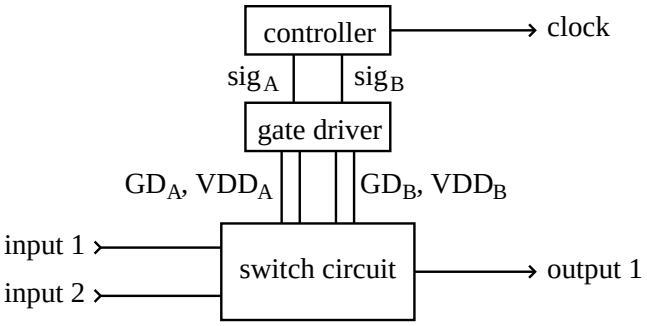

Fig. 4. Schematic diagram of Mixer.

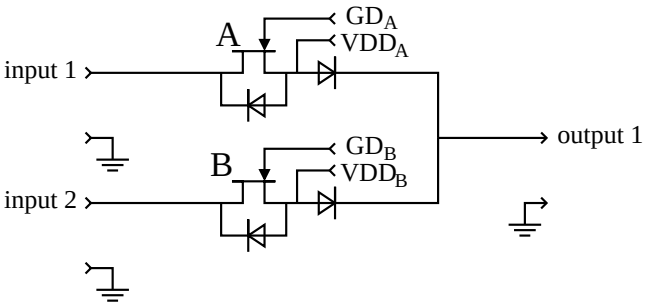

Fig. 5. Schematic diagram of the switch circuit in Mixer.

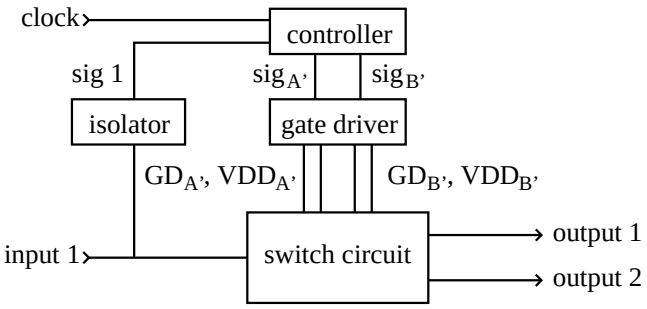

Fig. 6. Schematic diagram of Router I.

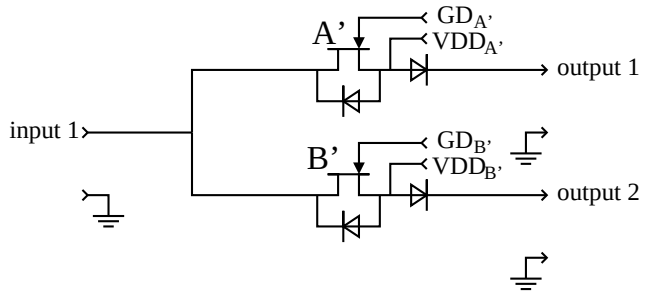

Fig. 7. Schematic diagram of switch circuit in Router I.

When the router receives a packet, it reads the header and footer attached to it. According to the address in the header, the router switches select one of the outputs. Then, the power packets are supplied to the objective load. However, Router I in the prototype system cannot be connected with other routers. This is because the power packet passing through the router loses the header signal, which must be read by the forwarding router, which in turn, makes the connection by Router I to the other router impossible. The new router explained in the next section is designed to forward the received power packets for networking.

III. Architecture of Router for Networked Power Packet Distribution System

In this section, we describe the development of Router II, which can forward a power packet with an information tag. To deliver a power packet from the desired source to the objective load via multiple routers, the router is requested to manage and reattach the information tag to the power packet. In addition, the router has multiple input and output ports. These are the minimum functions of Router II for network configuration.

Figure 8 shows a schematic diagram of Router II for the power packet distribution network. Router II consists of a switch circuit, gate driver, controller, and isolator. Currently, the lines for the system's common clock connect the mixers and routers to establish synchronization, as shown in Fig. 4. The controller reads the bit signals of power packets on the power distribution lines through an isolator. As the controller, we adopted a field-programmable gate array board. This controller also has a memory to capture the information obtained from the received power packet. The isolator consists of a photocoupler, Zener diode, and register. The isolator realizes the isolation between the controller and power distribution line, and also appropriately regulates the voltage level for input to the controller. When the input voltage is higher than the threshold of the isolator, and the rising edge of clock signal is simultaneously detected on the controller, the controller is given a designation as "1". In contrast, the signal "0" is set when the voltage is lower than the isolator threshold. The controller also outputs signals for ON/OFF regulation to the switches on the switch circuit via the gate drivers. Fig. 9 shows a schematic diagram of the switch circuit. The prototype Router II has a minimum of two input ports, two output ports, and two storage areas. It has sufficient generality to confirm

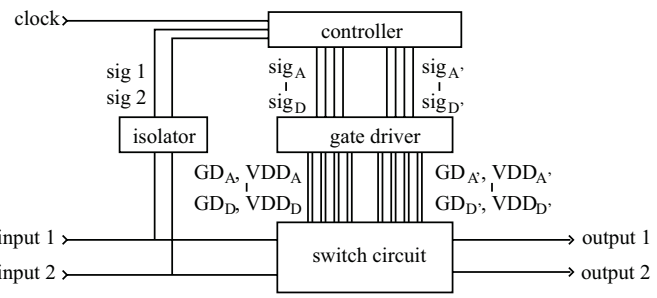

Fig. 8. Schematic diagram of Router II.

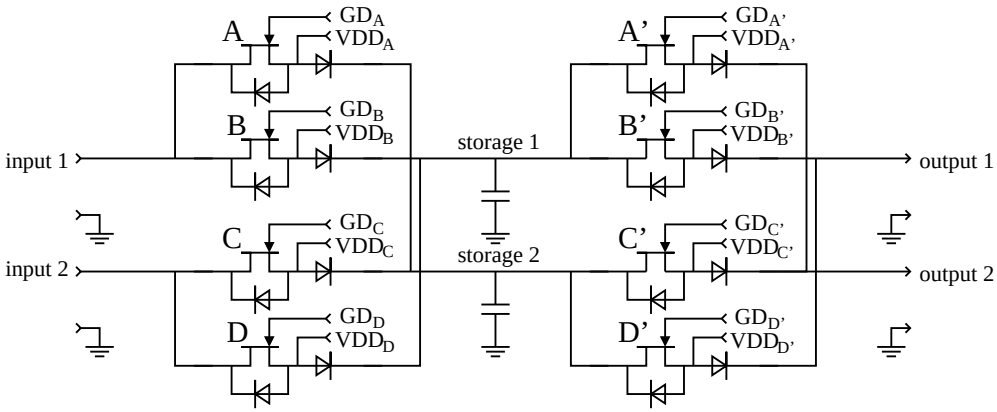

Fig. 9. Schematic diagram of switch circuit in Router II.

its feasibility for the functioning of Router II. The switches in the former block, i.e. A, B, C, and D in Fig. 9, guide the received power packet to the specified storage area according to its tag information. The number of the former switches is decided by the number of input ports multiplied by the number of storage areas (here, $4 = 2 \times 2$). The energy of the received power packets is stored in the storage areas temporarily. The storage areas are separated by source to avoid any loss of origin information of power. The switches in the latter block, i.e. A', B', C', and D', select the forwarding destination of the power packet, i.e., the objective load or the other router. As with the number of switches in the former block, the number of switches in the latter block is decided by the number of storage areas multiplied by the number of output ports (here, $4 = 2 \times 2$). In addition, the latter switches must also reproduce power packet information. They attach the information tag to the power payload based on the original tag information stored in the memory. Router II can be considered to be an integrated apparatus of the previous router and Mixer, that is, Mixer is added to be back of Router I.

In the prototype of Router II, SiC junction field-effect transistors (JFETs) (200 V, 5 A) are applied as the switching devices. The gate driver ADuM1233 is used to exchange the normally-off gate driving signal for the normally-on JFET [3]. The SiC JFET adopted here has a body diode; thus, the Si diodes are connected in series with each switch to prevent reverse current flow and to keep signals out of filtering by capacitive loads. For the storage areas in this prototype router, 1000 μF capacitors are set. A secondary battery for high power/energy densities can also be used for storage.

Table I shows the bit assignment of Router II that we used in the following experiments, in which assignments were fixed under the assumption that the connection status is static and already known. Note that these bit assignment and the number of bits can be changed. The design of bit assignment is one of the next topics. Six bits are assigned to the header. The first to third bits signal the beginning of a power packet. The fourth bit indicates the source address. The fifth and sixth bits are the set for the destination address. The controller reads the bits via the isolator. Soon after reading the bits of the header, the switch in the former block is turned ON to connect the specified storage area. The header bits are held in memory temporarily. After reading all the header bits, the switch connecting the objective output port in the latter block is operated to reproduce the power packets based on bit information in memory. In the experiments, the operation of the switch starts soon after the end of reading the header. However, by regulating the starting time of the switching operation, it can be expected to manage the power packet traffic. The footer has nine bits, which are the stop signal at the end of a power packet. After the controller reads the footer bits, the switches of the input port receiving its power packet are turned OFF. The footer bits are also held in memory temporarily and then are reattached to the reproduced power packet. All the switches of the used output ports are turned OFF after reproducing the power packet.

IV. Experimental Verification of Power Packet Forwarding over Connected Multiple Routers

In this section, the operation of the routers for the cascade network power packet distribution system is examined experimentally. We focus on the fundamental operations of Router II in forwarding the power packet, assuming that the network structure of the power packet dispatching system is already known and the path for forwarding the power packet to the objective load is fixed, as previously mentioned.

First, we verify that the Router II reproduces the power packet without losing the information tag attached to the received power packet. Second, we show that Router II can forward the power packet without losing the origin information

TABLE I
Bit Assignment of Router II

	start signal	source	address	storage	output
Header 1	1 0 1	0	1 0	storage 1	output 1
Header 2	1 0 1	0	1 1	storage 1	output 1
Header 3	1 0 1	0	0 1	storage 1	output 2
Header 4	1 0 1	1	1 0	storage 2	output 1
Header 5	1 0 1	1	1 1	storage 2	output 1
Header 6	1 0 1	1	0 1	storage 2	output 2

	end signal	storage	output
footer	0 0 1 0 1 0 0 0 0	–	–

of the delivered power. Finally, we confirm that the power packet is forwarded from the source to the objective load via multiple routers.

A. Reattachment of information tag to power packet passing through Router II

Figure 10 shows a schematic diagram of the system to verify the reattachment of the information tag to the power packets in Router II. This system consists of one Mixer, one Router II, one source, and two loads. A stretched VVF (Vinyl insulation, Vinyl sheath, Flat) electrical cable is connected between the output of Mixer and the input port 1 of Router II. A DC power source is set as the source, and non-inductive resistances are set as the loads at the outputs of Router II. In this experiment, both resistances are set at 100 Ω. The voltage of the DC source is set at 12 V. The bit assignment of the source in the header is fixed at "0" because the number of sources in the system is one. The bits "10" and "01" are assigned to loads 1 and 2, respectively. The power packets with Header 1 or 3 in Table I are transmitted from the mixer to the router alternately. The durations of a power packet and a bit are set at 256 μs and 2.56 μs, respectively. However, this is only an example and does not imply any restriction on higher frequency bit signals.

Figure 11 shows the measured voltage waveforms for the input port 1 of Router II and for the storage area 1 of Router II, load 1, and load 2. We found that the power packets from Mixer are delivered to the objective loads alternately. The voltage drops because of the SiC JFETs and diodes. Fig. 12 shows an extension of the waveforms at interval A in Fig. 11. The Router II waveform from 0.2 μs to 23.3 μs corresponds to the footer bits "001010000". From 23.3 μs to 38.6 μs, the header bits "101010" appear. The rest are the payloads. The load 1 waveform from 37.3 μs to 52.7 μs is "101010" corresponding to the header bits of the received power packet.

These results clarify that the reproduced power packet successfully replicated the information of the power packet received by Router II.

B. Conserving origin information of power delivered using Router II

In this subsection, we experimentally show that, using the Router II power packet dispatching system, each power packet from a different source is delivered to the respective objective loads without losing the origin information, even when being transmitted on the common power transmission line. We focus on two power sources. Fig. 13 shows a schematic diagram of the system to verify that the origin information of the power packet is conserved. This system consists of one Mixer, one Router II, two sources, and two loads. The voltage of the DC source 1 (2) is set at 12 V (5 V), and the bit assignment for source 1 (2) in the header is "0 (1)". Headers 1 and 6 in Table I are assigned to the power packets of sources 1 and 2, respectively. These power packets are then alternately delivered on the common power line. Other settings and parameters are maintained as in the previous subsection.

Figure 14 represents the input/output currents of the storage areas in Router II. Fig. 15 shows the input voltage waveform to Router II from source 1, and Figs. 16–19 show the current waveforms of the storage areas and loads. These waveforms were measured independently. As shown in Fig. 16, from 0.2 μs to 15.6 μs, the current of source 1 becomes 0 mA or 9 mA intermittently in response to the header bits. At 15.6 μs, the output current of source 1 changes from 0 mA to 107 mA. Simultaneously, the input current of storage 1 changes from 0 mA to 97 mA. The current corresponding to the difference between 107 mA and 97 mA flows to an isolator consisting of a diode and register. From these results, we conclude that all of the output current from source 1 flows to storage area

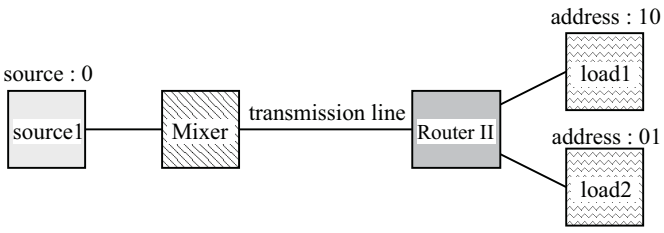

Fig. 10. Schematic diagram of the system to verify the reconstruction of power packets.

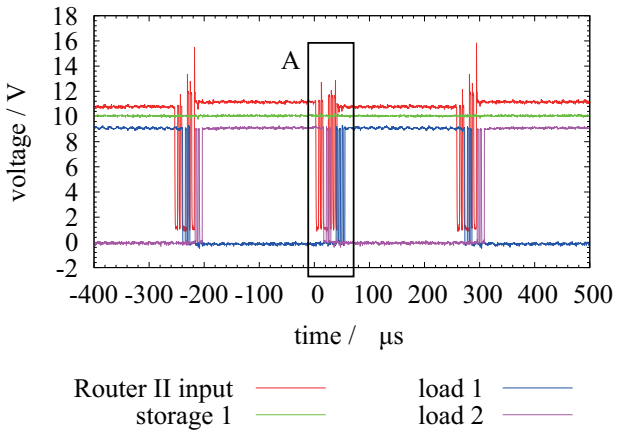

Fig. 11. Measured voltage waveforms on the system to verify the reconstruction.

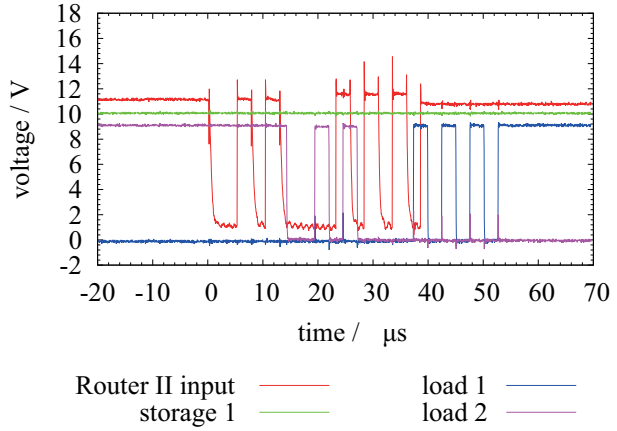

Fig. 12. Extension of interval A in Fig. 11.

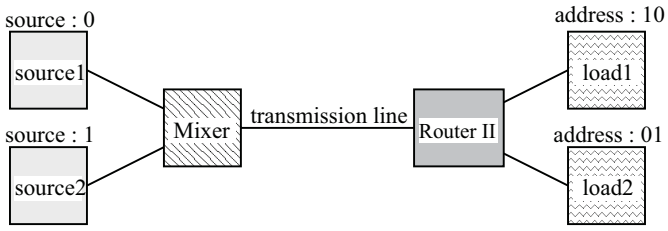

Fig. 13. Schematic diagram of the system to verify the reconstruction of power packets.

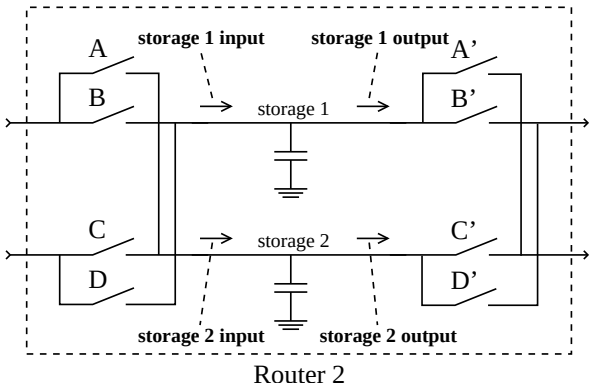

Fig. 14. Input/Output currents of storage areas in Router II.

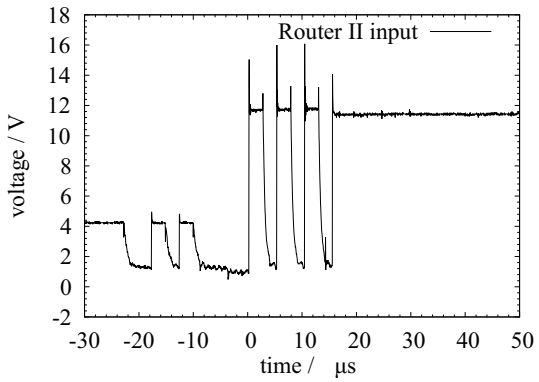

Fig. 15. Input voltage to Router II.

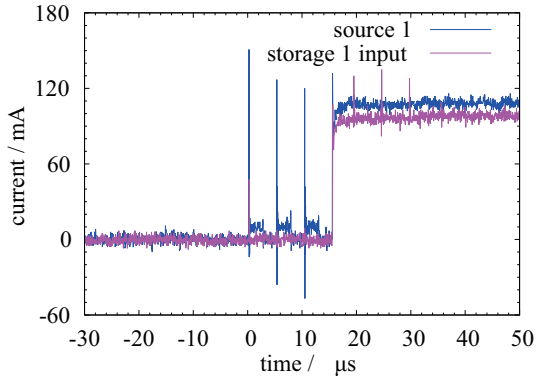

Fig. 16. Measured current waveforms of source 1 output and storage 1 input.

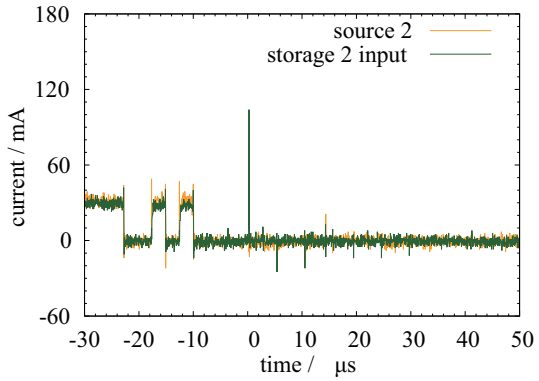

Fig. 17. Measured current waveforms of source 2 output and storage 2 input.

1. In the same manner, as shown in Fig. 17, all of the source 2 output current flows to storage area 2. When the current from one source flows to the storage area, the current from the other sources does not. Therefore, currents from different sources flow to each storage area without mixing. Next, we focus on the output current of storage area 1 and the current on load 1. In Fig. 18, from 14.2 μs to 29.6 μs, we see that both of the currents become 0 mA or 89 mA intermittently in response to the header bits of the power packet toward load 1. In this experiment, the output current of the storage area is lower than the input current. This is because the duration of the current output from the storage area corresponds to a duration of 90 bits (header, payload, and footer), while the input current to the storage area corresponds to a duration of 87 bits (payload and footer). Thus, we conclude that the storage area 1 and 2 currents flow to objective loads 1 and 2 respectively and individually, because the current waveforms of the storage areas correspond to the objective load.

Based on these results, we conclude that the power from source 1 (2) is delivered to objective load 1 (2) via storage area 1 (2), without mixing the power from various sources. This clarifies that power can be delivered by Router II without losing the origin information of the power.

C. Power packet delivery over multiple routers

In this subsection, we experimentally show that a power packet can be forwarded from a source to the objective load via multiple routers according to the power packet's tag information. Fig. 20 shows a schematic diagram of the system to verify the forwarding of the power packet via multiple routers. This system consists of one Mixer, two routers (Routers I and II), one source, and three loads. The input port 1 of Router II is connected to the output port of Mixer with a power transmission line. A load is set at one of Router II's two output ports. Another output port is connected to the Router I input port. Each of Router I's two output ports is connected to a load. The bit assignments of Routers II and I are shown in Tables I and II, respectively. The voltage of the DC source is set at 12 V, and the bit assignment of the source is fixed at "0". All loads have 100 Ω non-inductive resistances. The bits assigned to each load are as shown in Fig. 20. The duration of a power packet and bit are set at 256 μs and 2.56 μs, respectively. The power packets with Headers 1, 2, and 3 shown in Table I are

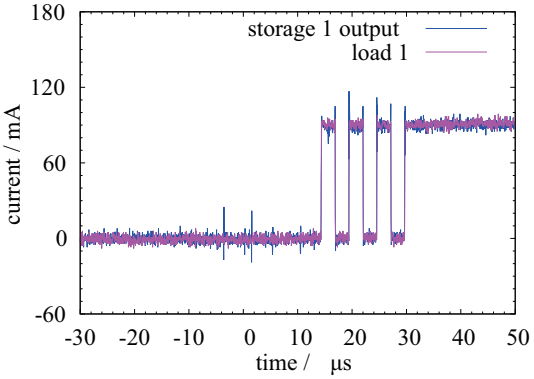

Fig. 18. Measured current waveforms of storage 1 output and load 1.

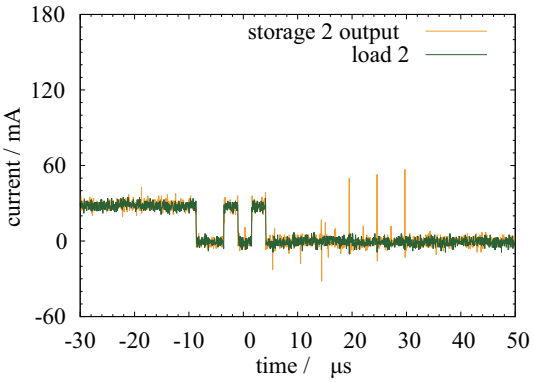

Fig. 19. Measured current waveforms of storage 2 output and load 2.

transmitted from Mixer in this order.

Figures 21–23 show the voltage waveforms when Router II received the power packets. In each figure, Router II received power packets with different tag information. For example, at around 20.6 μs in Fig. 21, the power packet is received by Router II and is then forwarded to objective load 1 via Router I. In Fig. 23, the voltage is applied to load 3 soon after

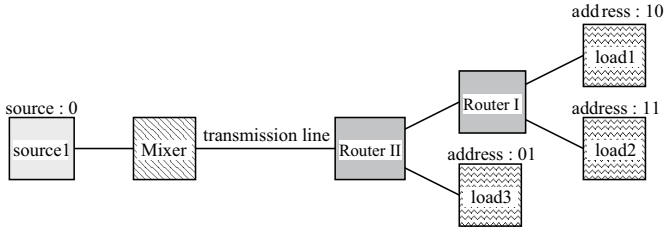

Fig. 20. Schematic diagram of the system to verify the forwarding of the power packet via multiple routers.

TABLE II
BIT ASSIGNMENT OF ROUTER I. "*" INDICATES "DON'T CARE".

	start signal	address	output
Header 1	101	010	output 1
Header 2	101	011	output 2

	end signal	output
footer	10100*	–

Router II finishes reading the header of the received power packet. In Figs. 21 and 22, however, we observe a delay in the application of voltage to each load. This is because, to be delivered from the source to loads 1 and 2, the power packet must be forwarded by not only Router II but also Router I. In addition, headers are not observed for the power packets arriving at loads 1 and 2. This is because the power packet passing through Router I loses the header signal, as mentioned

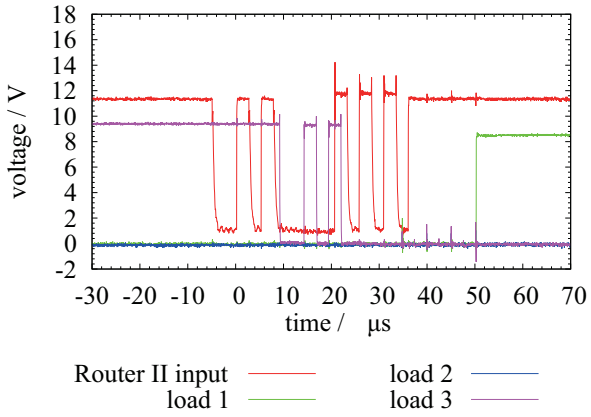

Fig. 21. Measured voltage waveforms when the power is started to be supplied to the load 1.

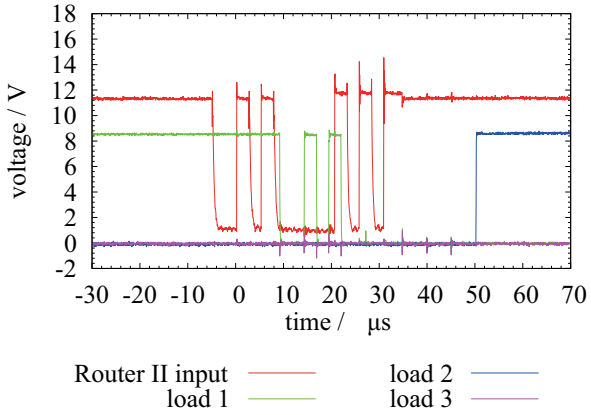

Fig. 22. Measured voltage waveforms when the power is started to be supplied to the load 2.

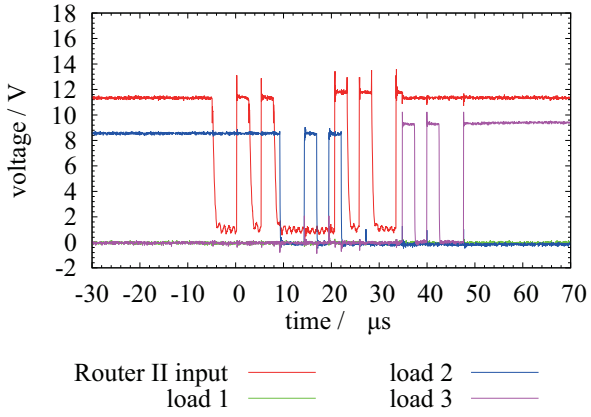

Fig. 23. Measured voltage waveforms when the power is started to be supplied to the load 3.

above.

These results experimentally confirm that power packets can be forwarded to their objective loads according to their tag information via multiple routers.

V. Conclusion

In this paper, we developed routers for a networked power packet distribution system. We then experimentally examined the delivery of power packets from the power source to the destination load via multiple routers in a cascade-network power packet distribution system with these routers. The results successfully established the feasibility of the power packet distribution network. Using a power packet distribution network, it is possible to forward and flexibly manage a power packet. As is mentioned before, this prototype system requires clock synchronization between all apparatuses, i.e., mixers and routers. Therefore, the signal cables are connected among them. Currently, we intend to take the cables away by establishing the synchronization with the preamble newly attached to each power packet [13]. This method has a potential to make it as a distributed control system. Since the TDM transmission method is applied to power packet transmission, the duration of the power packet should be shortened to increase the number of connected sources and loads. In these experiments, while the maximum frequency of the switching operation is around 400 kHz, it has been confirmed that this operation can achieve several tens of megahertz. Not only higher frequency but also larger power capacity can be expected to accompany the development of these power devices [4]. The performance of the power packet dispatching system heavily depends on these of the power devices, i.e., switches and diodes. As is shown in Fig. 9, a power packet passes through two pairs of SiC JFET and Si diode in the process of forwarding by one router. As a result, a part of delivered power is consumed because of these resistances. In addition, the power level in the system also depends on the power devices. The prototype system with SiC JFETs has a potential to manage 1000 W power packet. We have already confirmed 48 V power packet dispatching. Current target field to introduce the system is not high-power system, but less than home or community level. We consider that the design concept of the power packet dispatching system has scalability. In addition, we are intending to integrate the circuits and devices of each apparatus. This integration makes it possible to reduce the cost to introduce the power packet distribution system. The development of these power devices makes it possible to increase the power level and reduce the cost and power losses in the power packet dispatching system.

The packet congestion would be inevitable as the number of power packet delivered simultaneously on the network increases. However, the number of storage areas installed in the newly proposed router can be also increased. In addition, the starting time for forwarding the power packet can be managed. Therefore, power packet traffic can also be managed. The required energy delivered from source is stored in the storage area in the router once. The amount of stored energy is decided by capacities of the storage and power source. Using several storages and packets from several routers, the total amount of energy required by each load is intended to be satisfied. Several routing protocols and rule generation methods matching with this power packet distribution network have already been investigated for achieving an energy-on-demand system [22], [23]. These are collaborative research results from the same project. We also intend to establish the theoretical background of the power packet distribution network [14–16]. As is known, there are switching control theories from the viewpoints of power electronics, control theory, hybrid system theory [24], [25], and so on. Since power and information are integrated in this system, conventional approaches are not enough to analyze the whole system. We intend to extract the essential factors to establish the theory from an experimental approach.

The power packet dispatching system is believed to be one of the power distribution methods of the future. Renewable power sources and energy saving loads must be accompanied by the development of new power transfer methods, which as yet lag in 19th century technology. We believe power packet dispatching and networking will be a key factor in the development of a highly integrated novel power delivery system. We also believe that this represents a game changing technology in the history of electrical engineering.

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