IEEE Open Journal of
Circuits and Systems

Received 22 November 2020; revised 2 February 2021 and 10 March 2021; accepted 11 March 2021. Date of publication 17 March 2021; date of current version 2 April 2021.

Digital Object Identifier 10.1109/OJCAS.2021.3066645

Sampling and Comparator Speed-Enhancement Techniques for Near-Threshold SAR ADCs

BOJUN HU, SANFENG ZHANG (Graduate Student Member, IEEE), XIANGXIN PAN, XIANGYU ZHAO, ZHAOMING DING, XIONG ZHOU (Member, IEEE), SHIHENG YANG (Member, IEEE), AND QIANG LI (Senior Member, IEEE)

Institute of Integrated Circuits and Systems, University of Electronic Science and Technology of China, Chengdu 610054, China

This article was recommended by Associate Editor Y. Dong.

CORRESPONDING AUTHORS: Q. LI AND S. ZHANG (e-mail: qli@uestc.edu.cn; zhangsanfeng3031@foxmail.com)

This work was supported by the National Natural Science Foundation of China under Grant 62090041 and Grant 61534002.

ABSTRACT This paper presents the sampling and comparator speed-enhancement techniques for SAR ADCs under near-threshold supply voltages. The proposed level-shifted boosting circuit generates sharp falling edges for the sampling clock, which is found a key factor limiting the sample speed under ultra-low voltages. Delayed cross-coupling comparator is introduced in this work, which enhances the comparator regeneration while keeping the noise comparable. A 0.35V 8b 12MS/s SAR ADC is designed in a 65nm CMOS technology to prove the proposed techniques. The post-layout simulated SAR ADC consumes only 6.71μW and achieves SNDR of 48.8dB at Nyquist input, resulting in a figure-of-merit (FoM) of 2.47 fJ/convertion-step. Simulation results show the proposed speed-enhancement techniques improve the sampling rate of SAR ADC significantly under near-threshold supply voltages.

INDEX TERMS Sampling rate, SAR ADCs, comparators, ultra-low voltage, near-threshold.

I. INTRODUCTION

WITH the scaling down of feature sizes in advanced CMOS technologies, the standard supply voltages are getting lower. In order to achieve high speed under low voltages, pipeline [1] and flash [2] analog-to-digital converters (ADC) are designed to achieve tens of MHz sampling rate under 0.5V. But their figure-of-merits (FoMs) are not competitive as compared to successive approximation register (SAR) based ADCs due to the simple architecture with no need for power hungry modules. Working at low power supply voltage, SAR ADCs have a wide range of applications in wireless sensor network, biomedical (EEG, ECG, EMG), environmental monitoring (temperature, humidity, pressure) and other fields. However, the working principle of SAR ADCs normally limits the sampling rate at hundreds of kS/s with supply voltages lower than 0.5V.

Conventional SAR ADC is composed of two boosted sampling switches, a differential binary-weighted capacitive DAC, a comparator and control logics. For an asynchronous SAR ADC, the total time for each conversion cycle is

$$T_{all} = T_{samp} + \sum_{i=1}^{N} (T_{DAC}[i] + T_{comp}[i] + T_{logic}[i]), \quad (1)$$

where T_{samp} is the sampling time of the ADC. DAC settling time ($T_{DAC}[i]$), comparison time ($T_{comp}[i]$) and propagation delay time for digital control logics ($T_{logic}[i]$) consume the time budget of each successive approximate (SA) cycle. N SA cycles are needed for an N-bit SAR ADC with 1b-per-cycle architecture.

Constant-V_{GS} bootstrapping technique is commonly used for sampling switches, which keeps the on-resistance the same over the rail-to-rail input voltage range. The overdrive voltage of the sampling switch with constant-V_{GS} bootstrapping technique is VDD-V_{TH}. However, under near-threshold supplies, the overdrive voltages become too low for MHz sampling. A cascade of clock boosting circuits [3] is employed to achieve higher switch-on voltage, but the

falling edge of the boosted signal becomes slower, resulting in a slow turn-off of the sampling switch.

Comparator is the key analog block in a SAR ADC. The working speed of the comparator affects the comparison time ($T_{comp}[i]$) in each SA cycle, and the noise performance of the comparator affects the resolution of the ADC directly. Speeding up a comparator with large input transistors leads to large kick-back noise to the capacitor array, which is more severe for small arrays under ultra-low voltages. Another approach is to enhance the positive feedback of the cross-coupling transistors. However, because the amplification time is shortened, the comparator noise is enlarged [4].

Two speed-enhancement techniques for near-threshold SAR ADCs are introduced in this work. The level-shifted boosting circuit is proposed to achieve sharp-edged sampling clock for megahertz rail-to-rail sampling. Delayed cross-coupling comparator is exploited to improve the comparison speed and, at the same time, keep the comparator noise low. In order to demonstrate the proposed techniques, a 0.35V 8b 12MS/s SAR ADC is designed, achieving 7.82b ENOB and 2.47 fJ/conv.-step FoM.

The rest of this paper is organized as follows. Section II introduces the level-shifted boosting circuit. Delayed cross-coupling comparator is presented in Section III. Section IV shows the architecture of the SAR ADC with the proposed speed-enhancement techniques. Post-layout simulation and comparasion with recent design are carried out in this section. Section V concludes this paper.

II. LEVEL-SHIFTED BOOSTING CIRCUIT

The performance of sampling circuits limits both the speed and linearity of the whole ADC. High switch-on voltage is generally preferred for linear sampling of a rail-to-rail input. Clock boosting technique is often employed to boost the switch-on voltage. Constant-V_{GS} bootstrapping technique is widely used for sampling switches, since the overdrive voltage of the sampling switch remains the same with different input voltages, which doesn't introduce extra nonlinearity to the system. Since the overdrive voltage of the sampling switch with constant-V_{GS} bootstrapping technique is VDD-V_{TH}, the overdrive voltage is close to zero under a near-threshold supply voltage, which increases the switch-on resistance by several orders of magnitude. Hence, the sampling speed with constant-V_{GS} bootstrapping is limited under ultra-low voltages. A cascade of clock boosters [3] was introduced to boost the switch-on voltage several times, which ensures a sampling with 8-bit linearity.

Nevertheless, we found switch-off speed, or the falling time of the sampling clock, is the main limitation for sampling rate under low supply voltages. The relationship between the falling time of the sampling clock and SFDR & SNDR is analyzed in Fig. 1, where the sampling rate and switch-on voltage of the sampling clock are fixed at 12MS/s and 1V, respectively, and a 0.35V, 5.86MHz sine wave is used as the input signal. The simulation result in Fig. 1 indicates that SFDR and SNDR degrade when the

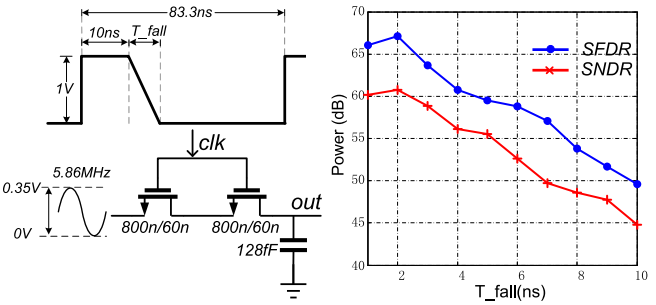

FIGURE 1. Simulated SFDR & SNDR versus the falling time of the sampling clock. The sampling rate and switch-on voltage of the sampling clock are fixed at 12MS/s and 1V. The input signal is a 0.35V, 5.86MHz sine wave.

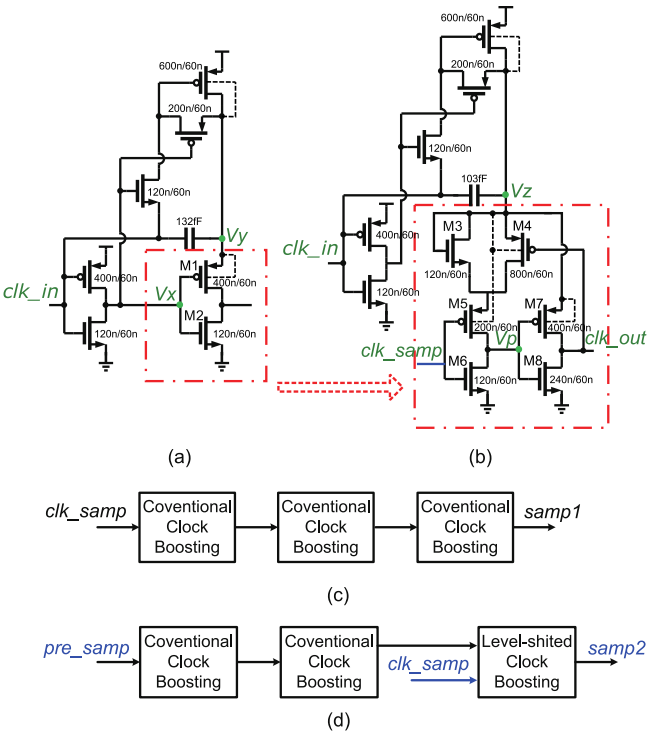

FIGURE 2. Schematics of (a) the conventional clock boosting circuit and (b) the proposed level-shifted boosting circuit; block diagrams of (c) three cascaded conventional clock boosting circuits and (d) two conventional clock boosting circuits cascaded with a level-shifted boosting circuit.

falling time of sampling clock increases. And a falling time less than 4ns is needed to achieve over 60-dB SFDR.

Fig. 2(a) presents the schematic of a single stage of conventional clock boosting circuit [5]. When *clk_in* gets high, *Vy* is set to *clk_in*+VDD and *clk_out* is connected to *Vy* through M1. When *clk_in* is low, *Vx* is set high to switch on M2, which pulls *clk_out* to low. Since *Vx* is limited by VDD, the voltage of *clk_out* in Fig. 2(a) falls slowly under near-threshold supply. Fig. 2(b) shows the schematic of the proposed level-shifted boosting circuit. A level shifter is utilized to replace the inverter in the dotted box in Fig. 2(a). Signal *clk_in* in Fig. 2(b) is used to pre-charge *Vz* to *clk_in*+VDD. When *clk_samp* is high, *Vp* goes low and *clk_out* is connected to *Vz* through M7. When *clk_samp* is

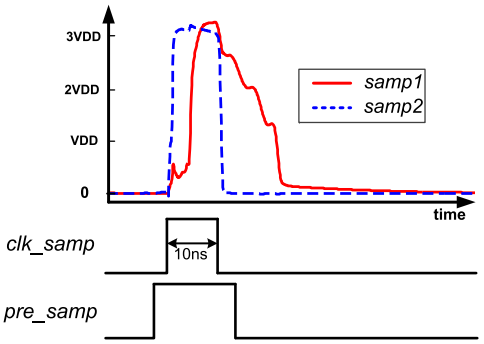

FIGURE 3. Simulated results of Fig. 2(c) and Fig. 2(d) under 0.35V supply voltage. The timing diagram is also shown.

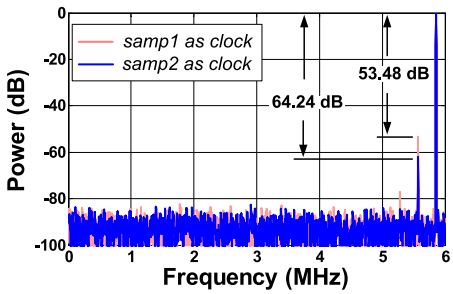

FIGURE 4. Simulated spectrum of 0.35V sampling circuit with clocking boosting circuits of Fig. 2(c) and Fig. 2(d). A 5.86MHz input is sampled at 12 MS/s.

low, Vp and Vz are connected together through M5 and M3. Hence, $Vp = Vz - V_{TH} = clk\_in + \text{VDD} - V_{TH}$. If clk_in is a high voltage signal, Vp is higher than VDD. So M8 pulls clk_out to zero much faster than M2. The connection of the PMOS substrate in the Fig. 2(a) and Fig. 2(b) is indicated with dotted lines. The purpose of this connection is to prevent the substrate leakage.

Since the maximum output voltage of a single stage of Fig. 2(a) and Fig. 2(b) is clk_in+VDD, the switch-on resistance of the sampling switch is limited under near-threshold supply. Therefore, cascade of boosting circuits is needed. Fig. 2(c) shows the block diagram of a popular solution with three cascaded conventional clock boosting stages. When *clk_samp* gets high, the output of the conventional clock boosting circuit goes high stage by stage. After three-boost-stage delay, signal *samp*1 rises to a boosted voltage. Similarly, when *clk_samp* gets low, the output of the conventional clock boosting circuit goes low stage by stage.

Fig. 2(d) presents the proposed circuit with two conventional clock boosting stages cascaded with a level-shifted boosting stage. Fig. 3 shows the timing diagram together with simulation results. Signal *pre_samp* is employed to pre-charge the capacitors to high voltage in the boosting circuits. When *pre_samp* gets high, the output of the two conventional clock boosting stages goes high stage by stage. Then *clk_samp* is set high to pull the output, *samp*2, to the boosted voltage only after two-stage gate transmission delay. When *clk_samp* goes low, Vp is pushed to a voltage higher than supply. Large overdrive voltage of M8 pulls the output voltage to zero in a very short time. Then signal *pre_samp* goes low after *samp*2 gets to zero.

From Fig. 3, the switch-on voltages of *samp*1 and *samp*2 are over 1 V, which ensures a small switch-on resistance. The falling time of *samp*1 is more than 10 ns. The falling time of *samp*2 from 0.9 maximum voltage to 0.1 maximum voltage is 1.8 ns, which is sufficient for a 0.35V 8b 12MS/s ADC according to Fig. 1. Fig. 4 shows the simulated spectrum of a 0.35V sampling circuit with the proposed clock boosting technique shown in Fig. 2(d). The performance with the conventional clock boosting circuit of Fig. 2(c) is also given as reference. The simulated sampling circuit is the same with the one in Fig. 1. With a 5.86MHz Nyquist input sampled at 12MS/s, 58.71dB SNDR and 64.24dB SFDR are achieved with the proposed clock boosting technique. As shown in Fig. 4, 10.76dB improvement on SFDR is obtained.

III. DELAYED CROSS-COUPLING COMPARATOR

Speed and noise are the key considerations for ultra-low voltage comparators. The comparison consumes the time of each SA cycle, and the input referred noise of the comparator affects the resolution of the ADC directly. In addition, there are tradeoffs between the speed and noise of the comparators.

Fig. 5(a) shows the schematic of a typical P-latch comparator. M1, M6 and M7 are used as switches to enable and reset the comparator. M2 and M3 are input differential transistors. M4 and M5 are cross-coupled for positive feedback. The process of comparison can be viewed as four phases [4], [6], i.e., reset, amplification, regeneration and decision, as shown in Fig. 6. When *clk* is low, M1 is turned off, M6 and M7 are turned on. The comparator is in reset phase, *Vop* and *Von* are reset to high. Sampling phase starts after the rising edge of *clk*, where the voltage difference of *Vop* and *Von* is sampled and amplified to trigger the following regeneration phase. The speed of the comparison can be improved with larger pull-down current by increasing the size of the M1, and increasing the size of M2 & M3 in the same proportion to achieve greater transconductance. However, increasing the size of the input transistors results in higher kick-back noise to the capacitor array, which degrades the linearity.

As a direct approach, an additional cross-coupled pair, M8 and M9, can be introduced to enhance the positive feedback, as shown in Fig. 5(b). Right after reset, the NMOS cross coupled pair is in on-state and starts regeneration, which greatly reduced the duration of amplification phase. To show the influence of the changing part, the transistors marked with the same name in Fig. 5 are also sized the same for the simulation in Fig. 7. The result shows NP-latch comparator is much faster than the P-latch one. However, the extra cross-coupling circuit decreases the sampling time as well. Since the input signal is sampled and amplified in amplification phase, the input referred noise of the comparator is inversely proportional to the time of amplification phase [4]. Hence, the noise performance of NP-latch comparator is degraded. The simulation result proves the root-mean-square (RMS)

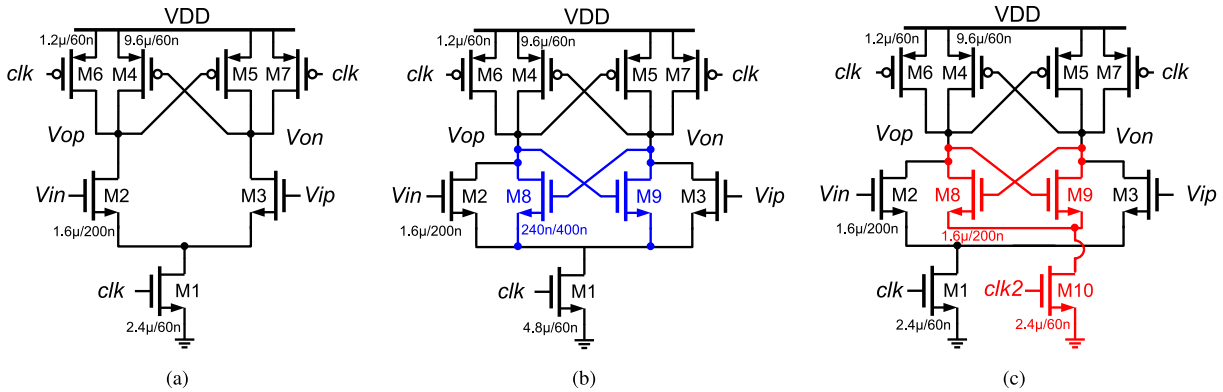

FIGURE 5. Schematics of (a) a P-latch comparator, (b) a NP-latch comparator, (c) the proposed delayed cross-coupling comparator.

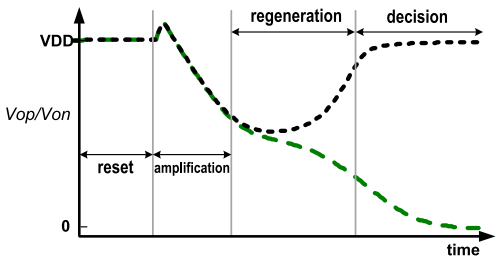

FIGURE 6. Four phases of conventional comparator.

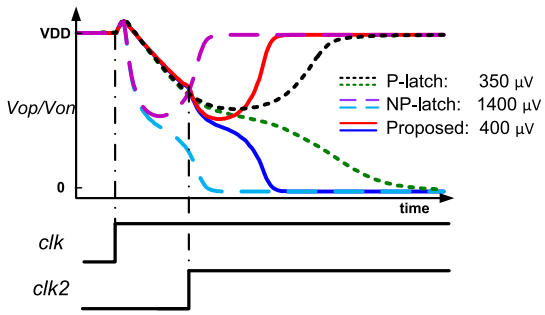

FIGURE 7. Simulated timing diagram and noise performance of the three kinds of comparators under the situation of "same name sized the same".

noise of NP-latch comparator is 1490 μV, whereas the noise of P-latch comparator is 350 μV.

The delayed cross-coupling comparator is proposed to decrease the comparison time without degrading the noise performance, as depicted in Fig. 5(c). Since M8 & M9 in Fig. 5(b) decrease the time for amplification phase and increase the comparator noise, the additional cross-coupling pair is delayed to work until the amplification phase ends. The timing of the comparator is given together with the simulation results in Fig. 7. The comparator is enabled when *clk* gets high, while *clk*2 is kept low during the amplification phase, disconnecting the extra cross-coupling pair from the comparator. Therefore, the equivalent circuit of Fig. 5(c) in amplification phase is the same with Fig. 5(a). *clk*2 gets high after amplification phase, then M8 & M9 are added into the circuit to enhance the regeneration. So the delayed

TABLE 1. Simulated noise and power with same delay.

	RMS noise	Average current
NP-latch comparator	767 μV	2.35 μA
Delayed cross-coupling comparator	400 μV	2.41 μA

cross-coupling comparator improves the speed of comparator without degrading the noise performance. In order not to degrade the noise performance, the rising edge of *clk*2 should be later than the amplification phase. While if *clk*2 is too late, the comparison speed would be affected. Hence, *clk*2 is generated by a voltage-controlled delay circuit from *clk*. The control signal can be adjusted manually in the simulation. When this value is set larger, the delay time is shorter, and the comparator is faster but noise performance gets worse. When this value is set small, the rising edge of *clk*2 arrives later, and the comparator's noise is reduced but the speed is limited. After a lot of simulations and comparisons, when the control voltage is set to 185mV, the optimal delay time on *clk*2 is 1.86ns, and the speed and noise performance of delayed cross-coupling comparator are optimized. From Fig. 7, the RMS noise of the proposed comparator is 400 μV, which is similar to the noise performance of the traditional P-latch comparator. It shows the proposed comparator can enhance the working speed while remaining the noise performance.

In order to show the improvement of the proposed delayed cross-coupling comparator, the sizes of M8 & M9 in the NP-latch comparator are tuned to achieve the same delay of the proposed comparator. The simulated noise and power are listed in Table 1. The average current is achieved under 125 MHz speed. Simulation results show the proposed comparator achieves similar power with NP-latch comparator, but the noise of the proposed one is much lower.

IV. ADC ARCHITECTURE AND SIMULATION

Sections II and III introduce two speed-enhancement techniques for near-threshold SAR ADCs. A 0.35V SAR ADC with those techniques has been designed with post-layout simulations. Fig. 8 presents the system architecture of the

TABLE 2. Performance summary and comparison.

	This work*	ESSCIRC'12 [8]			ISSCC'13 [9]		TCAS-II'15 [10]		TCAS-II'16 [11]		JSSC'16 [12]		JSSC'17 [13]	JSSC'19 [14]
Resolution (bit)	**8**	8			10		11		10		10		9	10
Tech. (nm)	**65**	40			90		130		90		90		28	40
Area (mm2)	**0.018**	0.0153			0.0418		0.868		0.0125		0.0408		0.00312	0.00975
Voltage (V)	**0.35**	0.35	0.4	0.5	0.4	0.5	0.4	0.5	0.3	0.5	0.4	0.5	0.47	0.5
Sampling rate (MS/s)	**12**	0.512	1.3	6.144	0.5	1.25	0.5	0.5	0.25	1	0.25	1	2	0.02
ENOB (bit)	**7.82**	6.79	7.08	7.07	8.72	8.94	9.6	10.03	8.21	8.65	8.63	8.75	7.42	8.77
Power (μW)	**6.71**	0.4	1.06	6.43	0.5	1.8	26.1	39.9	0.052	0.475	0.2	1.2	0.94	0.021
FoM (fJ/conv.-step)	**2.47**	6.8	5.9	7.7	2.37	2.93	67.3	76.3	0.705	1.18	2.02	2.77	2.7	2.4

* Post-layout simulation results

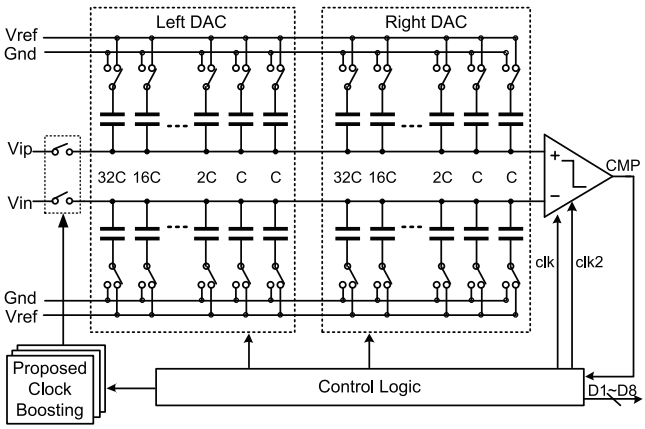

FIGURE 8. System architecture of the proposed SAR ADC.

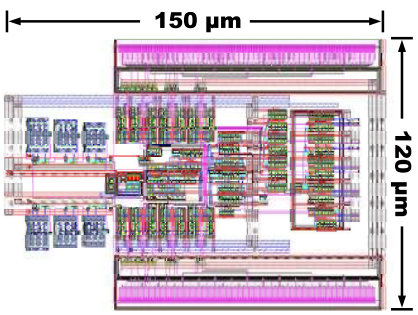

FIGURE 9. Layout of the proposed SAR ADC.

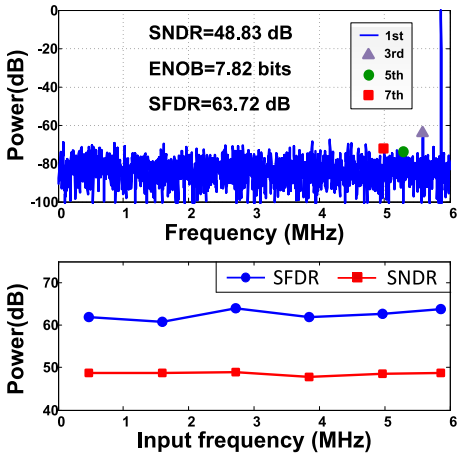

FIGURE 10. Dynamic performances of the proposed SAR ADC at 12 MS/s.

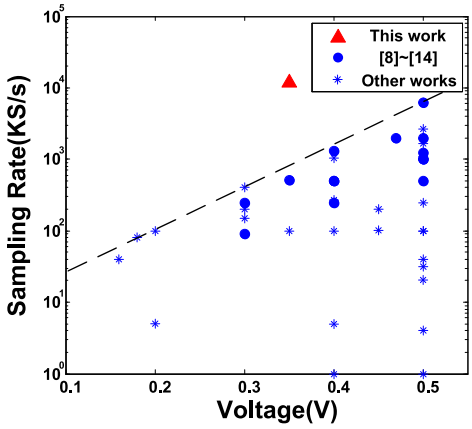

FIGURE 11. Sampling rates vs. supply voltages of reported sub-0.5V SAR ADCs.

proposed SAR ADC. It is composed of a split capacitor array [7], two sampling switches with the proposed level-shifted clock boosting circuits, the proposed delayed cross-coupling comparator and control logics. The split capacitor array is employed to avoid the common-mode reference voltage Vcm (0.5*VDD), because the low overdrive voltage for switching on Vcm affects the DAC settling time under ultra-low supply voltages.

The 0.35V ADC has been post-layout simulated in a 65-nm CMOS technology. Fig. 9 shows the layout of the proposed ADC. The unit capacitance of the CDAC is 1 fF. Fig. 10 shows the 4096-points fast Fourier transform (FFT) spectrum result with a 5.86 MHz input sampled at 12 MS/s. The SNDR and SFDR are 48.8 dB (7.82 ENOB) and 67.39 dB, respectively. The simulated results of SFDR and

SNDR versus input frequency are also presented in Fig. 10. The whole ADC consumes only 6.71 μW with DAC of 0.7 μW, comparator of 0.78 μW, clock boosting of 0.71 μW, and logic of 4.52 μW. With the Walden FoM definition,

$$FoM = [power]/[2^{ENOB} * fs], \quad (2)$$

a FoM of 2.47 fJ/conv.-step has been achieved. Table 2 summarizes the simulated performance and compares the proposed work with previously reported sub-0.5V SAR ADCs with 8-11 bits of resolution. Fig. 11 plots the speed performance of reported sub-0.5V ADCs, which indicates the proposed speed-enhancement techniques have significantly increased the potential sampling rate of near-threshold SAR ADCs.

V. CONCLUSION

Sampling and comparator speed-enhancement techniques for SAR ADC under near-threshold supply voltages have been introduced in this work. Sharp-edged sampling signal with 1.8-ns falling time has been generated by the proposed level-shifted boosting circuit. The proposed delayed cross-coupling comparator improves the comparator speed without degrading the noise performance. The proposed speed-enhancement techniques have been post-layout simulated in a 0.35V 8b 12MS/s SAR ADC. The results has proved the proposed sampling technique and comparator design with significantly enhanced speed as compared to reported near-threshold ADCs.

REFERENCES

[1] J. Shen and P. R. Kinget, "A 0.5-V 8-bit 10-Ms/s pipelined ADC in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 787–795, Apr. 2008.

[2] J. E. Proesel and L. T. Pileggi, "A 0.6-to-1V inverter-based 5-bit flash ADC in 90 nm digital CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, USA, Sep. 2008, pp. 153–156.

[3] X. Zhou and Q. Li, "A 160 mV 670 nW 8-bit SAR ADC in 0.13 μm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, USA, Sep. 2012, pp. 1–4.

[4] J. Kim, B. S. Leibowitz, J. Ren, and C. J. Madden, "Simulation and analysis of random decision errors in clocked comparators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1844–1857, Aug. 2009.

[5] D. C. Daly and A. P. Chandrakasan, "A 6-bit, 0.2 V to 0.9 V highly digital flash ADC with comparator redundancy," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 3030–3038, Nov. 2009.

[6] B. S. Leibowitz, J. Kim, J. Ren, and C. J. Madden, "Characterization of random decision errors in clocked comparators," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, USA, Sep. 2008, pp. 691–693.

[7] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 739–747, Apr. 2007.

[8] K. Yoshioka, A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro, "An 8bit 0.35–0.8V 0.5–30MS/s 2bit/step SAR ADC with wide range threshold configuring comparator," in *Proc. Eur. Solid-State Circuits Devices Conf. (ESSCIRC)*, Bordeaux, France, Sep. 2012, pp. 381–384.

[9] C.-Y. Liou and C.-C. Hsieh, "A 2.4-to-5.2fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with charge-average switching DAC in 90 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Techn. Papers*, Feb. 2013, pp. 280–281.

[10] X. Wang, H. Huang, and Q. Li, "Design considerations of ultralow-voltage self-calibrated SAR ADC," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 4, pp. 337–341, Apr. 2015.

[11] S.-E. Hsieh and C.-C. Hsieh, "A 0.3-V 0.705-fJ/conversion-step 10-bit SAR ADC with a shifted monotonic switching procedure in 90-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 12, pp. 1171–1175, Dec. 2016.

[12] Y.-J. Chen, K.-H. Chang, and C.-C. Hsieh, "A 2.02–5.16 fJ/conversion step 10 bit hybrid coarse-fine SAR ADC with time-domain quantizer in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 357–364, Feb. 2016.

[13] C. Wulff and T. Ytterdal, "A compiled 9-bit 20-MS/s 3.5-fJ/conv.step SAR ADC in 28-nm FDSOI for Bluetooth low energy receivers," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1915–1926, Jul. 2017.

[14] Z. Ding, X. Zhou, and Q. Li, "A 0.5–1.1-V adaptive bypassing SAR ADC utilizing the oscillation-cycle information of a VCO-based comparator," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 968–977, Apr. 2019.

BOJUN HU was born in China, in 1996. He received the B.S. degree from the University of Electronic Science and Technology of China, China in 2019, where he is currently pursuing the M.S. degree with the Institute of Integrated Circuits and Systems.

His current research interests include analog, mixed-signal circuits, and analog-to-digital converters.

Mr. Hu serves as a Reviewer for the IEEE International Symposium on Circuits and Systems and *Journal of Sensors*.

SANFENG ZHANG (Graduate Student Member, IEEE) received the B.S. degree from the School of Microelectronics and Solid-State Electronic, University of Electronic Science and Technology of China, Chengdu, China, in 2015, where he is currently pursuing the Ph.D. degree with the Institute of Integrated Circuits and Systems.

XIANGXIN PAN received the B.S. degree from the School of Microelectronics and Solid-State Electronic, University of Electronic Science and Technology of China, Chengdu, China, in 2018, where she is currently pursuing the M.E. degree with the Institute of Integrated Circuits and Systems.

Her research interests include analog circuit design and analog-to-digital converters.

XIANGYU ZHAO was born in China, in 2000. He received the B.Eng. (Hons.) degree from the University of Glasgow. He is currently pursuing the B.Eng. degree with the University of Electronic Science and Technology of China.

His current research interests include analog, mixed-signal circuits, and analog-to-digital converters.

ZHAOMING DING was born in Chongqing, China, in 1989. He received the B.S. degree in microelectronics from the University of Electronic Science and Technology of China, Chengdu, China, in 2012, where he is currently pursuing the Ph.D degree with the Institute of Integrated Circuits and Systems.

His research interests include analog, mixed-signal circuits, analog-to-digital converters, and phase-locked loops.

XIONG ZHOU (Member, IEEE) received the B.S. degree from the School of Microelectronics and Solid-State Electronic, University of Electronic Science and Technology of China, Chengdu, China in 2011, and the Ph.D. degree from the Department of Engineering, Aarhus University, Denmark, in 2016.

He has been an Associate Professor with the Institute of Integrated Circuits and Systems, and School of Electronic Science and Engineering, University of Electronic Science and Technology of China, since 2017. His current research interests include analog-to-digital converters, biopotential amplifiers and acquisition systems, low-power analog, and mixed-signal circuits.

Dr. Zhou serves as the Reviewer for several international journals and conferences.

SHIHENG YANG (Member, IEEE) received the B.Sc. degree in electrical and electronics engineering and the Ph.D. degree in electronic and computer engineering from the University of Macau (UM), Macau, China, in 2014 and 2019, respectively.

From 2019 to 2020, he was with the State-Key Laboratory of Analog and Mixed-Signal VLSI, UM. Since 2020, he has been a Faculty Member with the University of Electronic Science and Technology of China, Chengdu, China. His research interests include analog/mixed IC designs and RF circuits and specializing in the frequency synthesizers. He serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–II: EXPRESS BRIEFS.

QIANG LI (Senior Member, IEEE) received the B.Eng. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2001, and the Ph.D. degree from Nanyang Technological University (NTU), Singapore, in 2007.

Since 2001, he has been working on analog/RF circuits in both academia and industry, holding positions of an Engineer, a Project Leader and a Technical Consultant in Singapore, and an Associate Professor in Denmark. He is currently a Full Professor with the University of Electronic Science and Technology of China (UESTC), heading the Institute of Integrated Circuits and Systems. His research interests include low-voltage and low-power analog/RF circuits, data converters, and mixed-mode circuits for biomedical and sensor interfaces.

Dr. Li was a recipient of the Young Changjiang Scholar Award in 2015, the UESTC Teaching Excellence Award in 2011, and the Service Excellence Award in 2018. He was the TPC Chair of the 2018 IEEE Asia Pacific Conference on Circuits and Systems. He serves as a Guest Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS and an Associate Editor of IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS. He is the Founding Chair of IEEE Chengdu SSCS/CASS Joint Chapter. He serves as the Distinguished Lecturer of the IEEE Solid-State Circuits Society. He serves as a member of the Technical Program Committee of IEEE Custom Integrated Circuits Conference, European Solid-State Circuits Conference, and IEEE Asian Solid-State Circuits Conference.