Satellite L-Band Front End Design

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Abstract: - The design, simulation and experiments of an L-band front end for the new AMSAT Phase 3E satellite are presented here. At the project beginning several ways of solution have been considered. The double conversion receiver for the transponder and command unit described in this paper is based on the double PLL frequency synthesizer synchronized by an ultra stable oscillator positioned on-board the satellite.

Key-Words: - Satellite Communication, Phase Lock Loop Synthesizer, Noise Figure

1 Introduction

AMSAT P3E is a new project of the experimental spin-stabilized satellite that will be launched on high elliptical orbit with an apogee of 47 000 km. Requirements for an L-band front end on-board the satellite are very demanding. Besides high reliability in the temperature range from –30 up to +40 degrees, mechanical resistance and low power consumption, the requirement for high frequency stability is equally important. The reason for that is given by the exigency of low data rate transmission in both the coherent and non-coherent modes. The next requirement results from the ESA Galileo project. The experimental satellites' traditional frequency of 1268 MHz is allocated as the downlink frequency for GALILEO (European GPS) space segment as well. We have to make calculations with a possible receiver retuning of 1260 MHz. These are the reasons why we have decided to develop the L-band front end, as shown in fig.1, based on the double PLL frequency synthesis procedure.

2 Receiver Concept

At the receiver's input is a filter for effective suppression of transmitted signals on 2.4 10.5 and 24 GHz bands. Especially, the suppression of 2.4 GHz signal is very important for providing low isolation between satellite antennas. A two-stage low noise amplifier (LNA) allows to achieve extremely good receiver sensitivity. The 10.7 MHz intermediate frequency, which is common for all the satellite receivers and transmitters, demands the use of double conversion concept of the L-band receiver. The first mixer is double balanced diode mixer (RMS-30 from Mini-Circuits®) used for good inter-modulation feature achievement. Both the local oscillators are synthesized by a PLL synchronized by a frequency of 5 MHz. Next to the second mixer are two 10.7 MHz chains: - the first one for digital and analog transponder with radar signal limiter and AGC and the second one for 400 bps BPSK command detection.

3 Low Noise Amplifier

The two-stage LNA has been designed with Agilent pseudomorphic HEMTs ATF-55143, which work in an enhancement mode. These transistors do not require a negative bias voltage and have an extremely good typical noise figure. The design includes an input reject filter as well as an interdigital tuned band pass filter between stages. Microstrip technique has been applied on a PTFE substrate DiClad® 880 by ARLON with relative permitivity 2.2 and tg $\delta = 0.001$.

3.1 LNA Simulation and Experiment

The designed structure is shown in fig.2 and has been simulated by the Ansoft-Serenade tool. Fig.3 shows the parameters which have been achieved: gain about 38 dB, pass band riple about 2 dB, rejection of 2.4 GHz about 160 dB, noise figure < 0.5 dB and acceptable matching at both the input and output ends. The simulation showed that a good solution of noise matching to optimal source impedance, as shown in fig. 4, can be achieved by the wire of defined length (18 mm) laying on the substrate.

The LNA has been realized and the consequent measurements have confirmed the designed parameters as selectivity, gain (35 dB) and noise figure (0.57 dB).

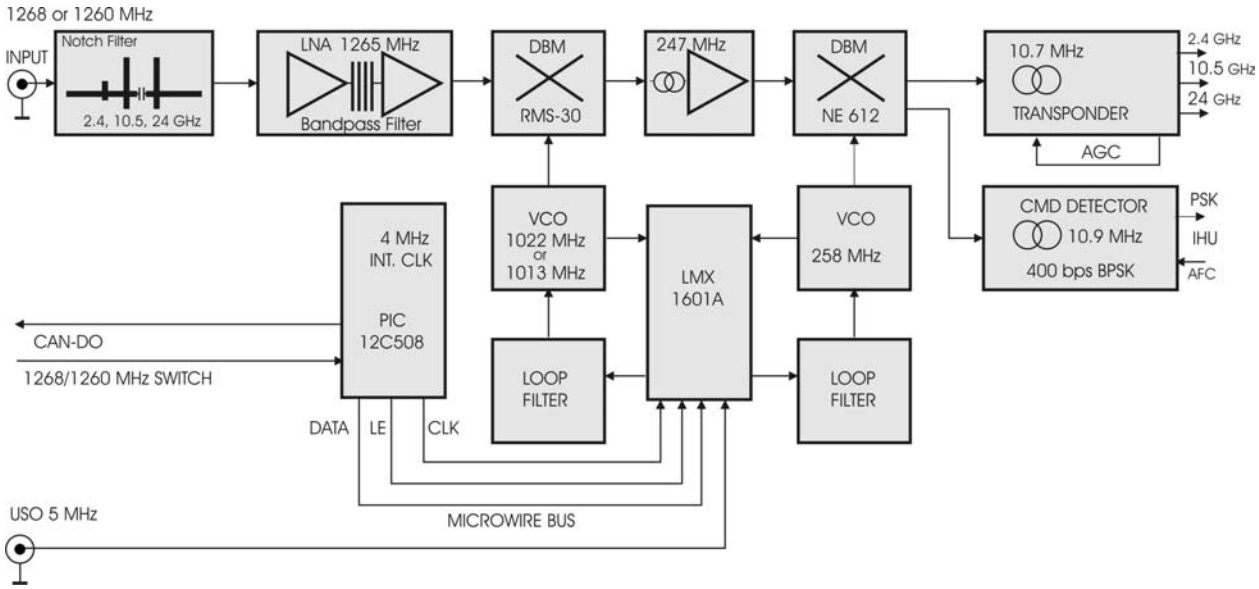

Fig. 1. Concept of the Phase 3E satellite L-band front end

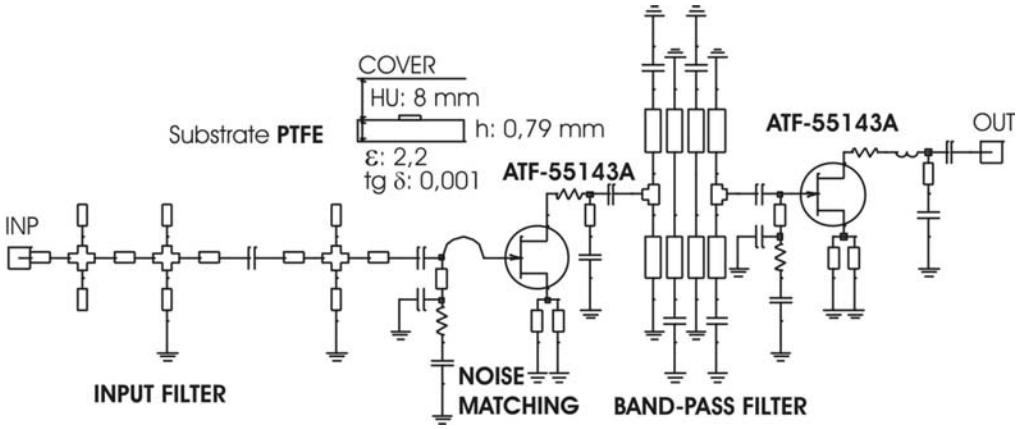

Fig. 2. Modeled structure of the input low noise amplifier including filters

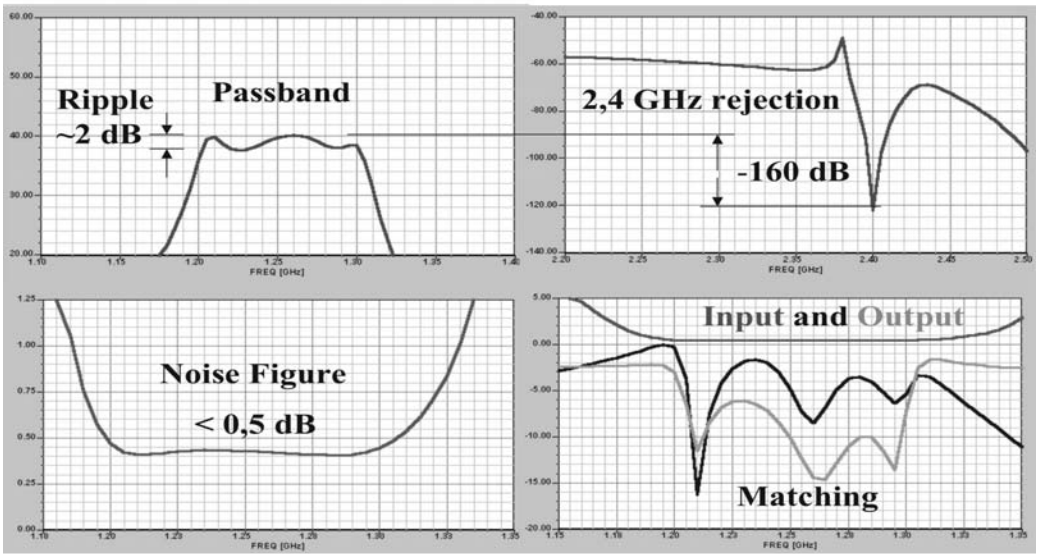

Fig. 3. Simulated parameters of the LNA model

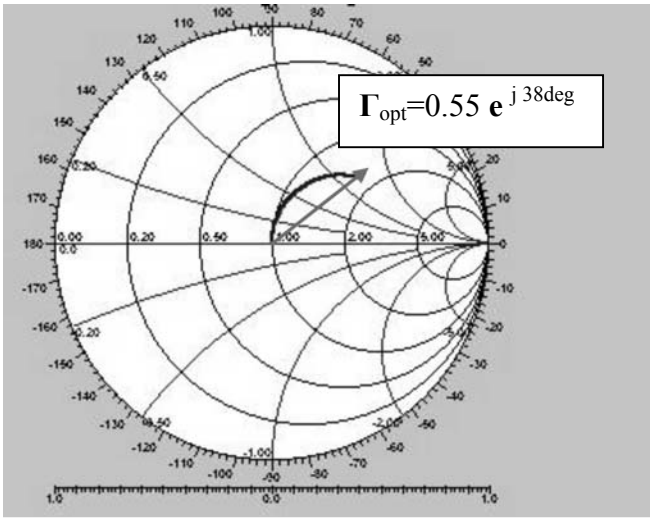

Fig. 4. Noise matching at the input of the first HEMT – the end point of the curve corresponds to 50 Ohms source impedance transformed by 18 mm wire laying on the substrate

4 Frequency PLL Synthesis

For the dual conversion front end, two local oscillators are needed. The first oscillator's nominal frequency is 1022 MHz. Comparative frequency for this synthesizer is 1 MHz as well as a possible frequency step. The second oscillator nominal frequency is 258.25 MHz at a comparative frequency of 250 kHz. Then the receiver may be tuned over tens of MHz with a step of 250 kHz. We suppose a possibility to retune the receiver of about 10 MHz by one bit according to a command from the ground. The receiver should be able to process very slow data rate (from 20 up to 400 bps) PSK signals. The spectral purity close to the carrier needs to be high. Power consumption should be as low as possible.

4.1 Serial Controlled Dual Synthesizer

Our solution uses the modern monolithic dual integrated synthesizer LMX1601 from National Semiconductor®. This part has been designed to be used in a local oscillator subsystem for a radio transceiver. The LMX1601 includes two dual modulus prescalers (up to 1.1 GHz and 500 MHz), four programmable counters and two selectable gain charge pumps. Digital filtered lock detectors for both PLLs are included. Data are transferred into the synthesizer by a three wire serial interface.

Low current consumption at low supply voltage and small dimensions (TSSOP-16 package) are the main advantages of this part. Both PLLs are independently programmable. It means that dividing ratios of all prescalers and charge pump gains are separated. Only a reference frequency input is common for both PLLs. The frequency of the reference ultra stable oscillator (USO) placed on the satellite board is 5 MHz. The LMX1601 contains single programmable (by Microwire™ serial interface) 18-bit data register for all of the four internal counters. The lock detector indicates the lock state of both the PLLs. The controller is the PIC12C508 from Microchip® chosen for its small package (SO-8) and low current consumption. The synthesizer and the controller have the same supply voltage of 3.3 V. The Main PLL section operates up to 1100 MHz and the Aux PLL section operates up to 500 MHz. The phase comparator's reference frequencies have been selected as maximal as possible with respect to the required output frequencies. The divide ratios in both PLLs are similar and phase noise degradation can be expected as uniform.

The chosen Voltage Controlled Oscillators (VCOs) are ROS-1500 and ROS-285PV respectively. They are made using hybrid technology by Mini-Circuits®. The PLLs need to be designed for low phase noise near the carrier because it is a part of the slow rate data PSK receiver. Lock time can be long because the synthesizer will not be tuned during operation. To minimize the low frequency phase noise, bandwidth of the loop filter should be narrow. Supply voltage of the main circuit LMX1601, including the charge pumps, is 3.3 V, which is lower than the required tuning voltage of VCOs in a wide temperature range. Therefore, the loop filters must be active. The operation amplifier used in the filter should be of low noise and must be fast with a bandwidth of tens of MHz. A suitable low noise type is MC33077 from ON-Semiconductor®. The MC33077 used in the active filter is speed low noise operational amplifier. The main advantages include, low noise, typically 4.4 nV/Hz^{½} at 1 kHz and a high slew rate of 11 V/μs. Configuration of the loop filter and its connection to the 1 GHz oscillator tuning input is shown in fig. 5.

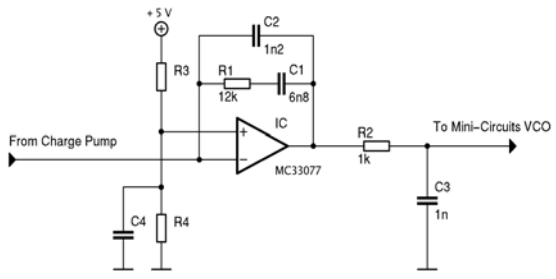

Fig. 5. The 2nd order loop filter

The filter is of second-order integration type. The near to ideal integration type of the active filter is important for phase conformity of both oscillators in

ranging experiments. The third order for the separation of the filter and the VCO tuning input is formed by R2 and C3 parts but its time constant is significantly higher than T_1 (R_1, C_1) and T_2 (R_1, C_1, C_2). The value of R2 should be small for good noise parameters [1][3]. Synthesizer's PLL loops have been simulated in National Semiconductor® WEBENCH™ tool Easy PLL [2]. Other parameters such as VCO, XO constants (gain, noise floor), filter components and tolerances have been defined. The charge pump gain is about 100 µA, the VCO gain on Main side is 20 MHz/V and 10 MHz/V on Aux side. The loop bandwidth of both PLLs is about 5 kHz. Calculated RMS phase error is 1.2 deg. Results of the phase noise simulation are shown in fig. 6.

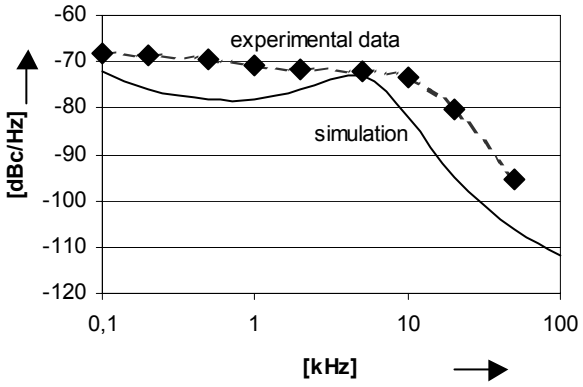

Fig. 6. Phase noise simulation and measured data (fig. 7.) for 1 GHz PLL synthesizer

A code for the controller has to provide a repeated data loading to the synthesizer, independent of other satellite operations. The program of the controller has to be simple and resistant to random interferences that could occur on board the satellite. The data loading needs to be repeated every time one of the loops gets unlocked too. But we also have to assume a soft damage to the registry contents (e.g. by radiation). For this reason, the data could be loaded at a regular interval.

4.2 Spectral purity measurement

The measured output signal of the 1 GHz synthesizer is shown in fig. 7. Then the calculated level of phase noise is given by,

$$\underset{\text{Measured}}{PN} = \underset{\text{Resolution}}{60\ \text{dB}} + \underset{\text{Log. Detector}}{10.8\ \text{dB}} + 2.5\ \text{dB} =$$

$$= \mathbf{73.3\ dBc/Hz\ @\ 5\ kHz}$$

and

$$\underset{\text{Measured}}{PN} = \underset{\text{Resolution}}{83\ \text{dB}} + \underset{\text{Log. Detector}}{10.8\ \text{dB}} + 2.5\ \text{dB} =$$

$$= \mathbf{96.3\ dBc/Hz\ @\ 50\ kHz}$$

The 258 MHz synthesizer has been measured in the same way and the results obtained are as follows:

PN = **81.3 dBc/Hz @ 1-10 kHz**

PN = **103.3 dBc/Hz @ 50 kHz**

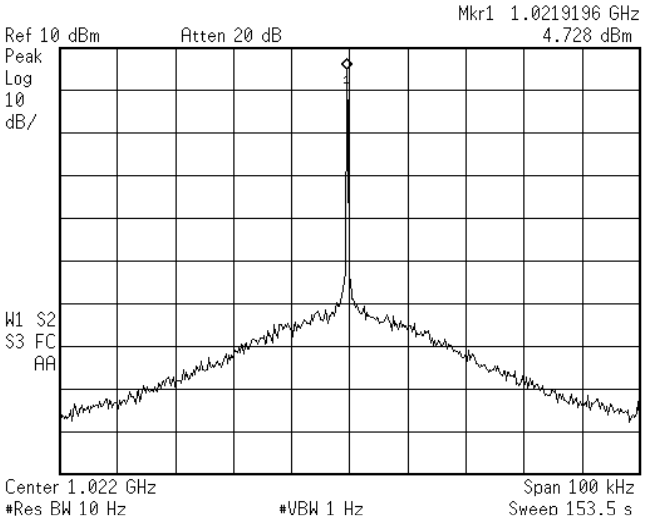

Fig. 7. Measured spectrum of the optimized 1GHz PLL synthesizer

The experimental results are thus in good agreement with the simulated parameters of fig. 6.

5 Conclusion

The satellite L-band front end has been developed, realized and measured. Besides the described work, additional tasks have been carried out. Thermal vacuum test alerts a possible problem with heat dissipation around the 1 GHz VCO [4]. Also the radiation resistivity test is prepared.

Acknowledgements

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