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# SC Amplifier and SC Integrator With an Accurate Gain of 2

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**Abstract**—A fully differential switched-capacitor (SC) amplifier and integrator with an accurate gain of 2 are proposed. Both circuits are based on a novel capacitor mismatch compensation scheme which uses the same capacitor as the charge sampling and summing element. Therefore, the gain error which is linearly proportional to the capacitor mismatch in conventional SC circuits becomes proportional to the square of the mismatch. In addition, the proposed scheme does not require additional active blocks, and the valid output is generated within two clock cycles.

**Index Terms**—Capacitor mismatch, gain error, mismatch compensation, switched-capacitor (SC) circuits.

## I. INTRODUCTION

SWITCHED-CAPACITOR (SC) amplifiers and integrators with an accurate gain of 2 are often used as the basic building block of high resolution pipeline/algorithmic analog-to-digital converters (ADCs) and sigma-delta ( $\Sigma\Delta$ ) modulators [1]–[5]. In conventional SC gain blocks and integrators, the gain error is mainly caused by the mismatch between the sampling and the summing capacitor, which is proportional to the mismatch itself [6].

For ADCs, the gain error of the interstage amplifiers limits the overall linearity and the resolution [7]. SC amplifiers using capacitor exchanging [1] and capacitor error averaging [2] have been proposed to solve this problem. Although both techniques enable an excellent reduction of the gain error, scheme [1] requires 4 clock periods for the complete operation, whereas scheme [2] needs 3 clock periods to generate the final output and an additional op-amp for the error averaging operation. An alternative approach is using the voltage adder [3]. However, in this scheme, special techniques such as the *floating hold buffer* proposed in [3] are required to minimize the parasitic capacitance coupling which limits the accuracy of the voltage adder. In case of  $\Sigma\Delta$  modulators, the integrator gain error increases the in-band noise level, thus degrading the signal-to-noise ratio (SNR) of the modulator [8]. However, for  $\Sigma\Delta$  modulators using the double sampling scheme, the capacitor mismatch can be corrected with the *fully floating SC configuration* proposed in [9]. In this approach, the folding effect caused by the spectral

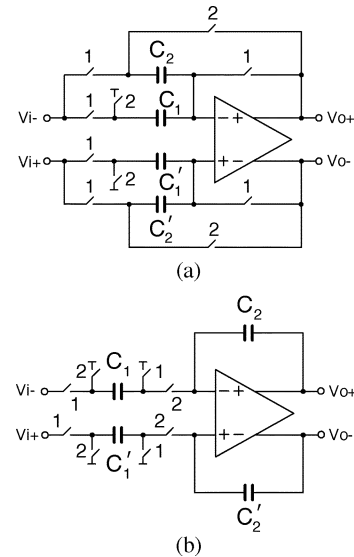


Fig. 1. Conventional circuits. (a) SC amplifier. (b) SC integrator.

components near the sampling clock frequency is eliminated, but the gain error itself due to the capacitor mismatch still remains.

In this brief, we present a novel SC amplifier and SC integrator both with a gain of 2 that are immune to capacitor mismatches. The conventional SC circuits are mentioned in Section II. In Section III, we first describe the concept of the proposed capacitor mismatch compensation scheme, and show how it can be applied to the SC amplifier and SC integrator. The proposed scheme differs from [3], since it is based on the charge transfer concept which is similar to [1], [2] and [9]. Section IV shows the effect of nonidealities, and the conclusion is given in Section V.

## II. CONVENTIONAL CIRCUITS

A fully differential SC configuration of a conventional amplifier and integrator, both with a gain of 2 are described in Fig. 1(a) and (b), respectively. For the SC amplifier, the input is sampled at  $C_1$ ,  $C_1'$ ,  $C_2$  and  $C_2'$  during  $\Phi_1 = H$ , and charge summing occurs at  $C_2$  and  $C_2'$  during  $\Phi_2 = H$ . Assuming the capacitors are mismatched as  $C_1 = C_2(1 + \varepsilon_1)$  and  $C_1' = C_2'(1 + \varepsilon_2)$ , the differential output during  $\Phi_2 = H$  becomes

$$V_{od} = \frac{1}{2} \left( 2 + \frac{C_1}{C_2} + \frac{C_1'}{C_2'} \right) V_{id} = \left( 2 + \frac{\varepsilon_1 + \varepsilon_2}{2} \right) V_{id} \quad (1)$$

where  $V_{od} = V_{o+} - V_{o-}$  and  $V_{id} = V_{i+} - V_{i-}$ . In addition, the above output expression is derived assuming that the direct

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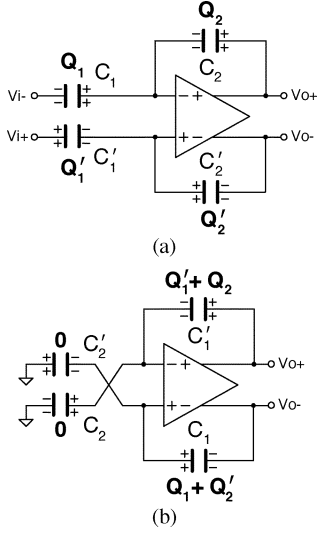


Fig. 2. Capacitor mismatch compensation scheme. (a) Sampling phase. (b) Summing phase.

inputs of the op-amp are unchanged during  $\Phi_1$  and  $\Phi_2$ . The remaining output expressions for the SC amplifiers and integrators that appear in this brief are all derived based on the same assumption.

The SC integrator samples the input at  $C_1$  and  $C'_1$  during  $\Phi_1 = H$ , and accumulates the sampled charge at  $C_2$  and  $C'_2$  during  $\Phi_2 = H$ . The capacitor ratio  $C_1/C_2$  and  $C'_1/C'_2$  are set to 2, in order to realize a gain of 2. Assuming  $C_1 = 2C_2(1 + \varepsilon_3)$  and  $C'_1 = 2C'_2(1 + \varepsilon_4)$ , the differential output is

$$V_{od}(n) = V_{od}(n-1) + (2 + \varepsilon_3 + \varepsilon_4)V_{id}(n-1) \quad (2)$$

where  $V_{od}(n) = V_{o+}(n) - V_{o-}(n)$  and  $V_{id}(n) = V_{i+}(n) - V_{i-}(n)$ .

From (1) and (2), the gain error of the conventional SC amplifier and integrator is  $(\varepsilon_1 + \varepsilon_2)/2$  and  $(\varepsilon_3 + \varepsilon_4)$ , respectively. Therefore, the gain error is linearly proportional to the capacitor mismatch for both circuits.

### III. PROPOSED CIRCUITS

#### A. Basic Concept Overview

The proposed capacitor mismatch compensation scheme is described in Fig. 2(a) and (b), where all the capacitors are identical. Also, the top plates of  $C_1$  and  $C'_1$  are connected to the input node of the op-amp during each phase. In the sampling phase, the input is sampled at  $C_1$  and  $C'_1$ , thus the charge stored in each capacitor is  $Q_1 = C_1V_{i-}$ ,  $Q'_1 = C'_1V_{i+}$ . Furthermore, the charge stored in each capacitor  $C_2$  and  $C'_2$  is  $Q_2 = Q_1$  and  $Q'_2 = Q'_1$ . During the summing phase,  $C_1$  and  $C'_1$  are cross coupled and connected in the feedback path of the op-amp, whereas the bottom plate of  $C_2$  and  $C'_2$  are connected to the signal ground. Therefore,  $Q_2$  and  $Q'_2$  will be injected into  $C'_1$  and  $C_1$ , respectively. This operation enables the gain of 2. Noticing  $V_{o+} = (Q'_1 + Q_2)/C'_1$  and  $V_{o-} = (Q_1 + Q'_2)/C_1$ , the differential output of the summing phase is

$$V_{od} = \frac{1}{2} \left( 2 + \frac{C_1}{C'_1} + \frac{C'_1}{C_1} \right) V_{id}. \quad (3)$$

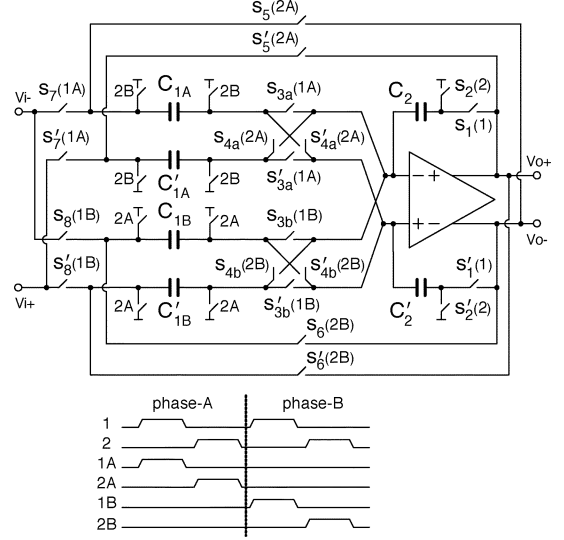


Fig. 3. Proposed SC amplifier.

Equation (3) shows that the gain error of the proposed scheme will only be affected by the mismatch between  $C_1$  and  $C'_1$ , since  $C_1$  and  $C'_1$  are used as the actual charge sampling and summing element, whereas  $C_2$  and  $C'_2$  are just for temporary charge storing. Moreover, replacing  $C_1$  with  $C_1 = C'_1(1 + \varepsilon)$  in (3), the gain error will be  $\varepsilon^2/2(1 + \varepsilon)$ , which is proportional to the square of the mismatch. This is much less than the gain error of the conventional circuits shown in Fig. 1(a) and (b), since  $\varepsilon^2 \ll |\varepsilon| \ll 1$ , and comparable to the gain error of the voltage adder proposed in [3], since the gain error of this scheme is proportional to  $C_{par}/C$  where  $C$  is the sampling capacitor and  $C_{par}$  is the average value of the parasitic capacitors at the amplifier input, and generally  $C \approx 100C_{par}$ .

#### B. SC Amplifier

In order to use the SC configuration shown in Fig. 2(a) and (b) as an amplifier that generates the valid output within 2 clock cycles,  $C_1$  and  $C'_1$  should be periodically discharged before the next sampling phase. However, this is problematic, since  $C_1$  and  $C'_1$  each stores the output voltage during the previous summing phase. This limitation can be solved by using another pair of capacitors. Fig. 3 shows the proposed circuit along with the control clocks. The operation of each phase A and B is exactly same as Fig. 2(a) and (b). But during phase A,  $C_{1B}$  and  $C'_{1B}$  are discharged, and during phase B,  $C_{1A}$  and  $C'_{1A}$  are discharged.

Assuming the capacitors are mismatched as  $C_{1A} = C'_{1A}(1 + \varepsilon_A)$  and  $C_{1B} = C'_{1B}(1 + \varepsilon_B)$  the differential output of each phase A and B is

$$\begin{aligned} \{V_{od}\}_{2A} &= \frac{1}{2} \left( 2 + \frac{C_{1A}}{C'_{1A}} + \frac{C'_{1A}}{C_{1A}} \right) \{V_{id}\}_{1A} \\ &= \left[ 2 + \frac{1}{2} \left( \frac{\varepsilon_A^2}{1 + \varepsilon_A} \right) \right] \{V_{id}\}_{1A} \end{aligned} \quad (4a)$$

$$\begin{aligned} \{V_{od}\}_{2B} &= \frac{1}{2} \left( 2 + \frac{C_{1B}}{C'_{1B}} + \frac{C'_{1B}}{C_{1B}} \right) \{V_{id}\}_{1B} \\ &= \left[ 2 + \frac{1}{2} \left( \frac{\varepsilon_B^2}{1 + \varepsilon_B} \right) \right] \{V_{id}\}_{1B} \end{aligned} \quad (4b)$$

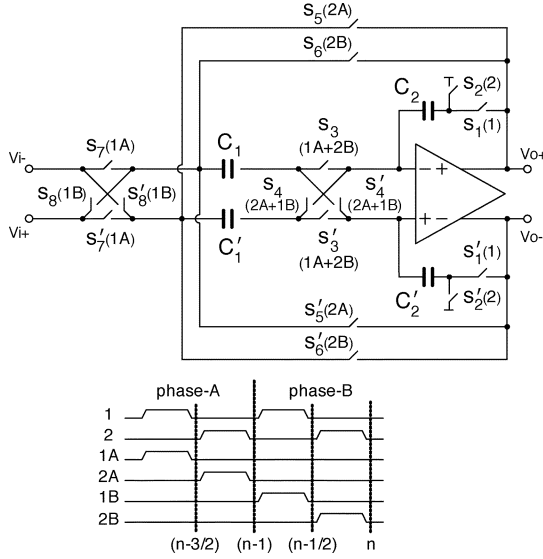


Fig. 4. Proposed SC integrator.

where  $\{V_{od}\}_{2X}$  is the output during  $\Phi_{2X} = H$  and  $\{V_{id}\}_{1X}$  is the input sampled during  $\Phi_{1X} = H$ ,  $X = A$  or  $B$ . Therefore, using another pair of capacitor does not affect the basic operation. The only problem is that the gain error of each phase can be different, since  $\epsilon_A \neq \epsilon_B$ . This periodical difference repeating every half the sampling frequency  $f_s/2$  will modulate the input and generate an image within the signal band, similar to the gain mismatch effect of the 2-channel time-interleaved ADC [10]. However, this effect can be negligible, since the gain error itself is very small. Moreover, the mismatch between  $C_2$  and  $C'_2$  does not affect the gain error, since they only function as a temporarily charge storing element during  $\Phi_{1A} = H$  and  $\Phi_{1B} = H$ . Thus, the mismatch between  $C_2$  and  $C'_2$  will only cause second-order effects.

### C. SC Integrator

Fig. 4 shows the proposed SC integrator. The basic operation is similar to the proposed SC amplifier, since  $C_1$  and  $C'_1$  are used for the charge sampling and summing purpose whereas  $C_2$  and  $C'_2$  are just for temporary charge storing. However, to accumulate the sampled charge,  $C_1$  and  $C'_1$  should be periodically swapped for each phase  $A$  and  $B$ .

We derive the complete time-domain output expression of the proposed SC integrator by combining the output terms of each phase  $A$  and  $B$ . For phase  $B$ , during  $\Phi_{1B} = H$ , the inputs  $V_{i+}(n-1/2)$  and  $V_{i-}(n-1/2)$  are sampled at  $C_1$  and  $C'_1$ , so the same amount of sampled charge will be induced in  $C_2$  and  $C'_2$ . At the same time, the charge that was previously stored in  $C_1$  and  $C'_1$  will transfer to  $C'_2$  and  $C_2$ , respectively, and will add up with the charge previously stored in  $C'_2$  and  $C_2$ . Thus, the charge stored in  $C_2$  and  $C'_2$  during  $\Phi_{1B} = H$  becomes

$$Q_{C_2} \left( n - \frac{1}{2} \right) = Q_{C'_1}(n-1) - Q_{C_1} \left( n - \frac{1}{2} \right) \quad (5a)$$

$$Q_{C'_2} \left( n - \frac{1}{2} \right) = Q_{C_1}(n-1) - Q_{C'_1} \left( n - \frac{1}{2} \right) \quad (5b)$$

where  $Q_{C_1}(n-1) = C_1 V_{o-}(n-1)$  and  $Q_{C'_1}(n-1) = C'_1 V_{o+}(n-1)$ . Furthermore, noticing that  $V_i(n-1/2) = V_i(n-$

$1)$ , since the inputs are sampled only during  $\Phi_{1A} = H$  and  $\Phi_{1B} = H$ , the sampled charge can be rewritten as

$$Q_{C_1} \left( n - \frac{1}{2} \right) = C_1 V_{i+}(n-1) \quad (6a)$$

$$Q_{C'_1} \left( n - \frac{1}{2} \right) = C'_1 V_{i-}(n-1). \quad (6b)$$

During  $\Phi_{2B} = H$ , since  $C_1$  and  $C'_1$  are connected in the feedback path, the accumulated charged stored in  $C_2$  and  $C'_2$  transfers to  $C'_1$  and  $C_1$ , respectively, and adds up with the sampled charge that is remaining in  $C'_1$  and  $C_1$ . This operation makes the gain of the integrator to 2. Now, the charge stored in  $C_1$  and  $C'_1$  during  $\Phi_{2B} = H$  becomes

$$Q_{C_1}(n) = Q_{C_1} \left( n - \frac{1}{2} \right) + Q_{C_2} \left( n - \frac{1}{2} \right) \quad (7a)$$

$$Q_{C'_1}(n) = Q_{C'_1} \left( n - \frac{1}{2} \right) + Q_{C'_2} \left( n - \frac{1}{2} \right). \quad (7b)$$

Using (5a)–(7b) and noticing  $V_{o+}(n) = Q_{C_1}(n)/C_1$  and  $V_{o-}(n) = Q_{C'_1}(n)/C'_1$ , the output of the SC integrator during  $\Phi_{2B} = H$  is

$$V_{o+}(n) = \frac{C'_1}{C_1} V_{o+}(n-1) + V_{i+}(n-1) - \frac{C'_1}{C_1} V_{i-}(n-1) \quad (8a)$$

$$V_{o-}(n) = \frac{C_1}{C'_1} V_{o-}(n-1) + V_{i-}(n-1) - \frac{C_1}{C'_1} V_{i+}(n-1). \quad (8b)$$

The integrator output for phase  $A$ , during  $\Phi_{2A} = H$  can be obtained by performing a similar analysis. The final results are

$$V_{o+}(n-1) = \frac{C_1}{C'_1} V_{o+}(n-2) + V_{i+}(n-2) - \frac{C_1}{C'_1} V_{i-}(n-2) \quad (9a)$$

$$V_{o-}(n-1) = \frac{C'_1}{C_1} V_{o-}(n-2) + V_{i-}(n-2) - \frac{C'_1}{C_1} V_{i+}(n-2). \quad (9b)$$

Finally, replacing the  $V_{o+}(n-1)$  and  $V_{o-}(n-1)$  terms in (8a) and (8b) with (9a) and (9b), the relationship between the differential output  $V_{od}(n)$  and  $V_{od}(n-1)$  results in

$$V_{od}(n) = V_{od}(n-1) + \left[ 1 + \frac{1}{2} \left( \frac{C_1}{C'_1} + \frac{C'_1}{C_1} \right) \right] V_{id}(n-1). \quad (10)$$

Due to the  $C_1/C'_1 + C'_1/C_1$  term in (10), the gain error of the SC integrator will also be proportional to the square of the capacitor mismatch.

## IV. EFFECT OF NONIDEALITIES

The limitation of the proposed circuits due to capacitor mismatch, switch clock feedthrough mismatch, op-amp dc gain, and op-amp input offset was investigated through circuit simulations. For all the simulations, the clock frequency  $f_s = 50$  MHz and input sinusoidal frequency  $f_{in} = 4.007$  MHz was assumed. The value of the unit capacitor was 1 pF.

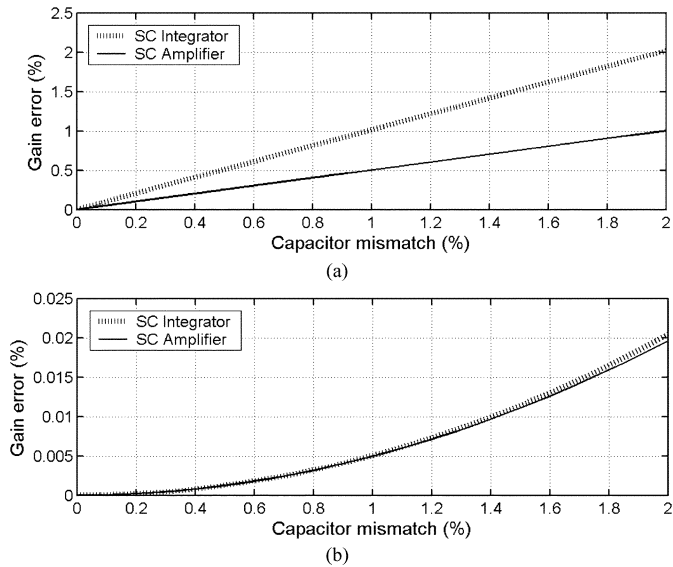


Fig. 5. Gain error versus capacitor mismatch. (a) Conventional. (b) Proposed.

### A. Capacitor Mismatch

For the capacitor mismatch simulation, ideal op-amps and switches were used to exclude the additional gain error terms caused by the switch and op-amp nonidealities. In addition, the mismatches among all critical capacitors were considered. Fig. 5(a) and (b) shows the gain error with respect to the capacitor mismatch  $\varepsilon$  for the conventional and proposed circuits. Comparison of Fig. 5(a) and (b) supports the validity of our analytical results. With a 1% mismatch, the gain error of the proposed circuits reduces to approximately 0.005%.

### B. Switch Clock Feedthrough Mismatch

Generally, for SC circuits, the clock feedthrough mismatch of the MOS switches causes distortion [1], [5], and since our proposed SC circuits use a complex switching scheme compared to the conventional circuits, this effect can be critical. However, for the proposed circuits, the mismatch caused by switches  $S_5 - S_8$  and  $S'_5 - S'_8$  shown in Figs. 3 and 4 can be eliminated by using the bottom plate sampling technique [5]. However, the mismatch effect of switches  $S_1, S'_1, S_2,$  and  $S'_2$  can still be critical, since they are directly connected to  $C_2$  and  $C'_2$ .

To simulate the clock feedthrough mismatch effect of the short-channel MOS switches, all the ideal switches were replaced with MOS switches with channel length of  $0.18\text{-}\mu\text{m}$ . CMOS transmission gates were used for switches  $S_5 - S_8$  and  $S'_5 - S'_8$  for both circuits, whereas the other switches were all NMOS. The size of the NMOS and PMOS devices were set to  $W_n/L_n = 2\ \mu\text{m}/0.18\ \mu\text{m}$  and  $W_p/L_p = 10\ \mu\text{m}/0.18\ \mu\text{m}$ , respectively, with gate control voltage of  $\pm 1.5\ \text{V}$ . Furthermore, the mismatch was induced between all the switches using the same control clock by giving a geometry error. Dummy switches were used for  $S_1, S'_1, S_2,$  and  $S'_2$  to minimize the mismatch effect. The harmonic tones caused by the switch mismatch were observed for each simulation. However, for the proposed circuits, it was difficult to measure the exact gain

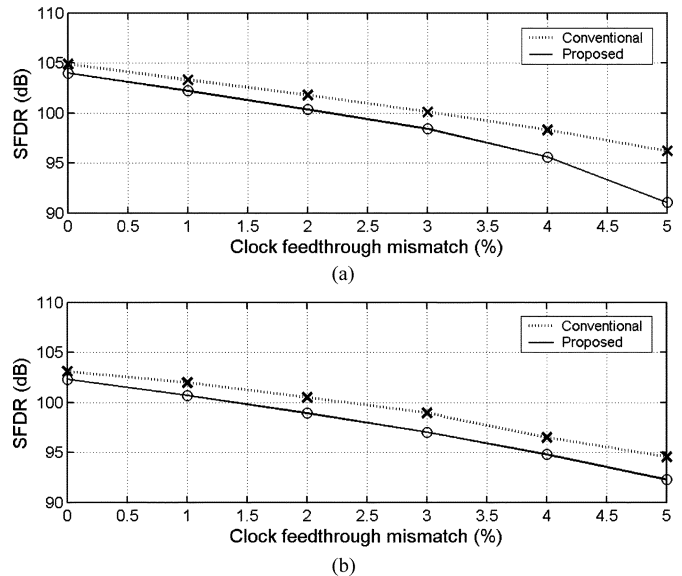


Fig. 6. SFDR versus clock feedthrough mismatch. (a) SC amplifier. (b) SC integrator.

TABLE I  
GAIN ERROR (%) OF PROPOSED CIRCUITS WITH RESPECT TO  $A_o$

$A_o$	40dB	50dB	60dB	70dB	80dB	90dB
SC AMP.	0.99	0.47	0.1	0.045	0.014	0.005
SC INTEG.	1.46	0.48	0.14	0.047	0.015	0.005

error contribution owing to the clock feedthrough mismatch, since the circuits contain switches with signal dependent and signal independent charge injection which cause gain error as well as offset error [1].

Fig. 6(a) and (b) each shows the spurious free dynamic range (SFDR) degradation with respect to clock feedthrough mismatch. The conventional circuits correspond to Fig. 1(a) and (b). The SFDR degradation of the proposed circuits is not much compared to the conventional circuits. This shows the tones due to switch mismatch can be considerably suppressed by using bottom plate sampling and half size dummy switches for  $S_1, S'_1, S_2,$  and  $S'_2$ . The SFDR of the proposed SC amplifier and integrator for 2% clock feedthrough mismatch is 100.4 dB and 98.9 dB, respectively. However, the abrupt SFDR degradation of the proposed SC amplifier around 4% mismatch is due to the  $(f_s/2 - f_{in})$  tone which became dominant as the mismatch increased. For the SC integrator, the effect of this tone was minor.

### C. Op-Amp DC Gain $A_o$

Table I shows the simulation results. The gain error of the proposed circuits is proportional to  $1/A_o$ , which is also the case for conventional circuits [2], [6]. Thus, to obtain accuracy near 0.01%,  $A_o$  should be at least 80 dB.

### D. Op-Amp Input Offset $V_{os}$

To see the effect of  $V_{os}$ , we applied the offset voltage  $V_{os}$  to the inverting input of the op-amp shown in Fig. 2(a) and (b), and

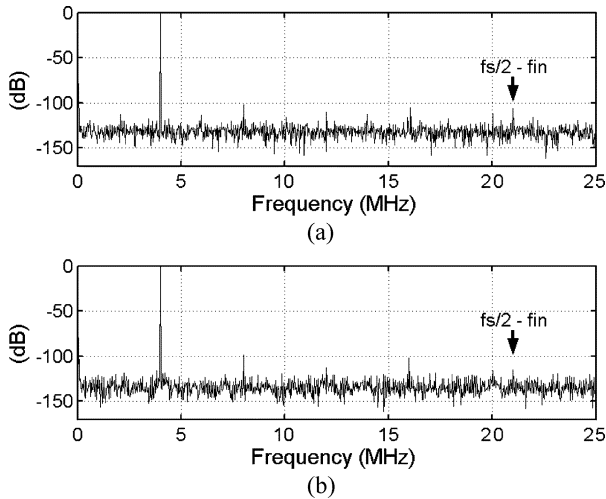


Fig. 7. Output spectrum of the proposed circuits with clock feedthrough mismatch of 2%,  $A_o = 80$  dB,  $V_{os} = 0.1$  mV. (a) SC amplifier with  $|\epsilon_A - \epsilon_B| = 1\%$ . (b) SC integrator with  $\epsilon = 1\%$ .

derived the output expression of the summing phase. The result is given by

$$V'_{od} = \frac{1}{2} \left( 2 + \frac{C_1}{C'_1} + \frac{C'_1}{C_1} \right) V_{id} + \left( 2 + \frac{C_1}{C'_1} \right) V_{os} \quad (11)$$

The input offset term is included in the output. This indicates that  $V_{os}$  will not be cancelled in the proposed SC amplifier and integrator. Circuit simulation showed the same result for both circuits. Therefore, an additional offset cancellation scheme is required for the proposed circuits if they are to be used in offset sensitive applications. However, input offset of the SC integrator is not problematic in  $\Sigma\Delta$  modulators, since the offset is cancelled by the operation of the loop filter [6].

### E. Output Spectrum

Fig. 7(a) and (b) shows the output spectrum of the proposed circuits including all the nonidealities. A 4096-point FFT was taken with the 1-V peak-to-peak output to generate the spectrum. For both circuits, the even harmonics are dominant. This is expected to be due to the clock feedthrough mismatch of the

MOS switches. In addition, tones are also present at dc and  $(f_s/2 - f_{in})$ . However, the  $(f_s/2 - f_{in})$  tone of the SC integrator is not large.

### V. CONCLUSION

A SC amplifier and SC integrator with an accurate gain of 2 are proposed. Both SC circuits are based on the capacitor mismatch compensation scheme. The accuracy of the proposed circuits is proportional to the square of the capacitor mismatch. Results show the gain error respect to a 1% capacitor mismatch is only 0.005%. Although it is shown that the accuracy of the proposed circuits is limited by the switch clock feedthrough mismatch, op-amp dc gain, and op-amp input offset, we have also proposed guide lines to minimize the effect of these nonidealities.

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