SCALABLE AND HIGH THROUGHPUT BIOSENSING PLATFORM

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ABSTRACT

A novel multi-channel high performance embedded system capable of high throughput biological analysis is proposed in this paper. Despite other integrated lab-on-chip solutions based on magnetoresistive biochips have already been developed, they lack the scalability and computational resources to cope with new biochip designs featuring more than 1000 sensors. A new configurable acquisition and processing architecture is proposed, combining dedicated co-processors to perform signal filtering and other computational demanding tasks, with a central processor controlling the whole system. The mapping of the architecture into a Zynq SoC demonstrated its ability to support 8 times more sensors, while ensuring a sampling frequency 1000+ times higher than the previous platforms. Furthermore, the Zynq reconfiguration abilities provide a mechanism to adapt the processing and maximize the biological sensitivity.

1. INTRODUCTION

Conventional biological analysis methods are being gradually replaced by sophisticated and compact biochip-based point-of-care devices. These perform common blood or glucose analysis at a fraction of the cost and require a much shorter analysis time [1, 2]. Given the high potential of these technologies, the research in biodetection methods and biochips has significantly grown in the past decade. From this research, new and more efficient methods became possible, providing a valuable tool for several applications, like clinical diagnostics, forensics or drug screening. A good example is gene expression profiling, where thousands of biosensors analyze a given sample in parallel [1]. However, given the complexity and computational needs of the electronic sensing system, portable and standalone embedded systems with adequate computational capabilities for such high throughput analysis have not yet been developed.

Recently, magnetoresistive biochips have been developed and integrated with electronic systems to provide complete lab-on-chip solutions [2, 3]. INESC-ID and INESC-MN developed a system [4] that has a low throughput but achieves a high sensitivity, high Signal-to-Noise Ratio (SNR) and high dynamic range [5]. The developed system includes all the electronic circuitry for addressing the biochip, for driving control signals and for conditioning and acquiring the biochip signals. It has a single acquisition channel, with a maximum rate of 3.52 k samples per second (sps). However, by using Time-Division Multiplexing (TDM), it is able to address up to 256 biosensors. The acquired signals are processed by a micro-controller and transmitted to a digital analyzer where, through a conventional graphical user-interface, the experiment is controlled by the operator or analyst [4].

However, more than 256 sensors are required for many important applications (e.g., gene expression profiling). To tackle this limitation, a new type of magnetoresistive biochip that combines CMOS with thin film fabrication technologies has been recently developed [6]. Currently, faster multi-channel biochips are being prototyped and will reach more than 1000 sensors. These require multiple acquisition channels operating at a higher sampling rate, thus producing a much higher volume of data and demanding a computation power that cannot be delivered by the current platform [4].

To deliver the computational power required by the new generations of biochips and allow simultaneous acquisition and processing at higher sampling rates, a high-performance and configurable acquisition and processing architecture is herein proposed. It uses multiple dedicated co-processors performing Fast Fourier Transform (FFT)-based signal filtering, as well as other complex correction algorithms. An additional dedicated processor is used to synthesize the stimulus signals for the sensors, and a *central* processor to control the whole system. With this approach, a fully autonomous embedded system is envisaged to allow a standalone operation of the platform and to increase its flexibility and usability. This system is prototyped on a Zynq-based board and shows to be able to support the growing demands of computational resources, which will be required by future analysis systems based on the new generations of biochips.

The paper is organized as follows. Section 2 introduces the biological detection principles and the inherent signal processing algorithms, which are implemented by the architecture proposed in Section 3. Section 4 details the system

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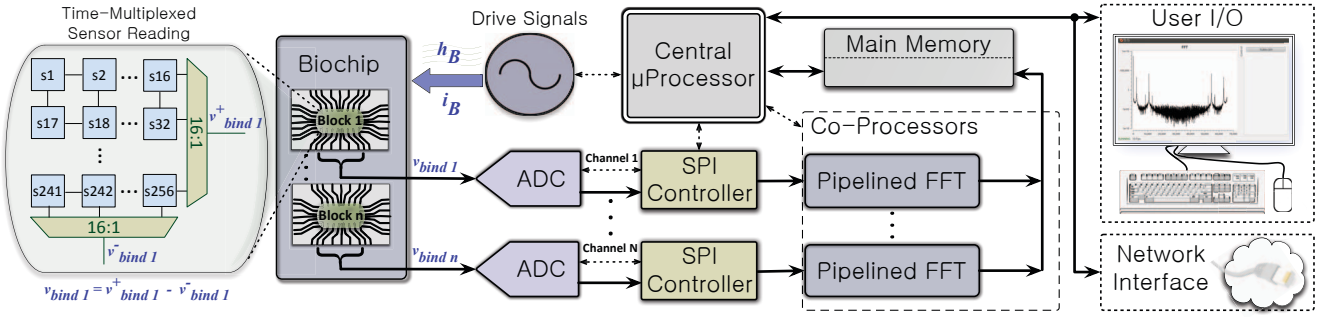

Fig. 1. Proposed scalable and high-throughput biosensing platform.

implementation on a Zynq prototyping board and experimental results are provided in Section 5. Finally, Section 6 concludes the paper.

2. BIOLOGICAL DETECTION PRINCIPLE

Figure 1 depicts the biochip schematic representation and its interface with the proposed platform. The laboratory assay begins by labelling the biological targets under analysis with Magnetic Particles (MPs). Then, a bias current, i_B, and an oscillating magnetic field, h_B, are applied to the sensors. Upon biomolecular recognition and washing, the sensors detect the fringe fields created by the MPs that have been captured by biological probes placed above the sensors [2, 3]. The biological information is then extracted by measuring the variations of the sensor voltage signal, v_{bind} [4].

To reduce the system cost and complexity, the 256 biochip sensors are measured in TDM. Since reaching a low noise level requires a high number of samples per sensor, biochip reading times in the previous version of the platform is about 4 minutes [4]. Because biomolecular recognition occurs at a low speed, this strategy is acceptable for previous biochips. However, it does not scale when the number of sensors grows to 1000+. To circunvent this, newer biochips are organized in groups of at most 256 elements and time multiplexed within each group. With this approach, the total reading time is constrained to the number of sensors within each group. Thus biochip size can be scaled without increasing the overall reading time. Nevertheless, this also imposes significant changes in the platform electronics. Each group must be serviced by a dedicated acquisition channel comprising signal conditioning circuits and an Analog-to-Digital Converter (ADC). Furthermore, the data from each channel needs to be processed in parallel, to allow the observation of the assay evolution in real-time.

Additional characteristics of the biochip must also be considered. To avoid the effect of low frequency noise and maximize the attained SNR, the applied signals i_B and h_B must include an AC component. Consequently, v_{bind} needs to be measured at a specific binding frequency, f_{bind}, which is determined by the modulation induced by the magnetic field $h_B\{f_2\}$, the bias current $i_B\{f_1\}$, the sensor's response to these AC signals, and the system's noise and cross-talk. Due to the complexity of the biochip technology and of the circuitry that drives and measures the sensors, it is not easy to determine a good a-priori estimate of the frequency at which the SNR is maximum. To optimize the biological sensitivity, f_{bind} should be adapted in real-time, by changing the frequencies of i_B and/or h_B. However, this introduces the added difficulty of determining the signal amplitude at an unknown frequency. A flexible and tractable method is to use an FFT of the signal acquired at each of the 1000+ sensors, to compute the signal amplitude v_{bind} at the frequency f_{bind}. Although it ensures a good adaptability, this approach requires a sampling frequency greater than 50 kHz and a frequency resolution as low as 1 Hz, for a 24-bit resolution in each sensor. This imposes large memory and hardware requirements, constraining the scalability of the system.

3. PROPOSED ARCHITECTURE

The computational performance required to ensure the resolution and reliability of bio-recognition assays can be achieved by optimizing the processors' architecture and by increasing the exploited parallelism with the usage of multicore structures. Nonetheless, similarly to what happens with most high throughput applications, it would be insufficient to exclusively address the performance limitations, since the bottleneck may also arise in the communication channels, such as the one connecting the acquisition circuits to the processing unit. Furthermore, due to the significant complexity of the underlying algorithms, the processing unit must be able to store and manipulate large datasets, making it clear that a high memory bandwidth and capacity are necessary to take full advantage of the enhanced processing capabilities.

The architecture proposed to fulfil the requirements of the high throughput biosensing platform is depicted in Fig. 1. A high-speed serial interface must be selected in order to provide a fast communication between the ADC and the set of dedicated cores where the most computational intensive tasks are handled. All components, including the generator of the stimuli signals, are configured by a General

Purpose Processor (GPP) which, aside from acting as the main system controller, can also perform auxiliary computations on the acquired data. This processor shares its main memory with a set of I/O devices, such as the input peripherals used to control the experiment and the display on which the results are presented to the user. A network interface is also included, allowing the processed data to be transferred to an external database, easily available to other users.

The following subsections provide a more detailed description of the embedded system main building blocks.

3.1. Central Processor and Main Memory

A GPP is the most suitable device to configure the several system components and it plays a key role on easing the system integration. Operating System (OS) support is absolutely necessary, in order to benefit from the available software packages that provide complex system management functionalities and high-level interfaces to the standard I/O and memory peripherals. The processor-memory interconnection subsystem should be equipped with DMA channels (or equivalent), allowing the processor to communicate with streaming peripherals within a shared memory space.

3.2. High-throughput sensor interface

Each acquisition channel is linked to one biochip sensor group and directly feeds one specialized co-processor with the data sampled by the ADC. Since each ADC can operate at a maximum rate of 96 Mbit/s, the absence of a high-speed data channel would seriously compromise the overall throughput. A standard Low-Voltage Differential Signaling (LVDS) was chosen as a cost-effective and noise tolerant solution to achieve high transmission rates. On top of this physical layer, a Serial Peripheral Interface (SPI) bus protocol is considered, to provide configuration and addressing capabilities based on a SPI *master/slave* controller.

3.3. Specialized Co-processors

The specialized FFT co-processors are responsible for measuring the amplitude of the sensors binding signal, v_{bind}, at a specific frequency. This signal is estimated using a *zoom-in* FFT approach. In a first step, an FFT is performed with a low frequency resolution, and by using a subset of sensors in the same channel. This provides a coarse and preliminary identification of the best f_{bind} frequency to measure the v_{bind}, while keeping the hardware resources and power consumption at tolerable levels. After identifying the f_{bind} range, band-pass filtering and signal demodulation are performed, to displace the frequency of interest down to base band. This allows the computation of multiple FFTs (one per channel) with a higher bit and frequency resolution, while still confining the required resources. Also, to increase SNR and achieve system scalability, the *zoom-in* procedure can be performed as many times as required.

Due to the involved computational complexity, a reconfigurable FPGA device is regarded as the most suitable technology to accommodate the multi-core infrastructure of specialized FFT co-processors. It combines the required high performance level, while still conferring the flexibility to change or update the adopted processing algorithms. In particular, multiple configurations are stored in memory: one for each *zoom-in* level. In run-time, the user starts by observing the coarse signal spectrum of the initial subset of sensors. Then, the most favourable demodulation frequency and spectrum band is selected. This will trigger the FPGA reconfiguration and the deployment of the specialized co-processors in hardware, configured with the target demodulation frequency. At this point, the user can observe the binding signal for each sensor.

3.4. Stimulus signal generator

As referred in Section 2, reference AC signals must be supplied to the biosensors, to produce a measurable response. The amplitude and frequency ranges of these stimuli is partially constrained by the considered biochip technology. However, since the noise level at which the measurements are exposed to is inversely proportional to the frequency of these signals, the accuracy of the results is strongly constrained by this parameter. As a consequence, a variable and configurable frequency generator, which can be adjusted and parametrized by the GPP, will ensure the adaptability of the biosensing platform to new generations of the biochip. The required signal generators can be easily implemented by using Direct Digital Synthesizers (DDSs) deployed in the reconfiguable fabric and controlled by the GPP.

3.5. I/O Peripherals and User Interface

A convenient set of I/O peripherals are required to make this biosensing platform a truly standalone analysis and diagnosis system. These modules not only allow the user to take full control of the experiment, but also offer the visualization means for clinical interpretation purposes. The standard set of computer peripherals (i.e. USB keyboard / touch screen panel and HDMI monitor) is regarded as the most appropriate means to prototype this interface, conferring the desired usability experience. Furthermore, thanks to the OS running on the GPP, the evolution from the proposed system to a final commercial product will require little engineering and adaptation efforts.

4. IMPLEMENTATION

The Xilinx Zynq 7000 Extensible Processing Platform was considered the most appropriate prototyping technology for

the proposed embedded system. This particular System on a Chip (SoC) includes a state of the art reconfigurable fabric and it offers most of the features required for the proposed system. This section starts with a brief overview of the Zynq architecture, followed by a description of the implemented scalable and high-throughput biosensing platform.

4.1. Zynq SoC Architecture

The Zynq SoC integrates two independent modules in the same chip: a Processing System (PS), featuring a dual-core ARM Cortex-A9 processor, and Programmable Logic (PL), consisting of reconfigurable fabric compatible with Xilinx 7-Series FPGAs. In addition to the ARM processors and the associated DDR-memory controller, the PS also integrates a collection of industry-standard communication interfaces (Gigabit Ethernet, USB, I2C and SPI). At boot time, the PS configures the PL by means of the Processor Configuration Access Port (PCAP) and initializes the system clocks. Through the PCAP, the ARM processor is able to exploit the software-driven dynamic partial reconfiguration capabilities of the reconfigurable fabric, thus promoting an adapted and optimized usage of the reconfigurable part of this SoC.

The PS-PL interconnection can be achieved by using the Advanced eXtensible Interface (AXI) bus protocol through any of the provided connectivity ports, namely, General-Purpose (AXI-GP), High-Performance (AXI-HP), and Accelerator Coherency Port (AXI-ACP). Two master and two slave AXI-GP interfaces connect the PL to the PS central interconnect, allowing for low throughput data and control transfers. When high throughput is required, the AXI-HP interface, that connects directly to the main memory, is used. In this interface, read and write operations are mediated by an asynchronous 1 kB FIFO with a configurable data width of 32 or 64 bits. The AXI-ACP interface connects the PL directly to the Snoop Control Unit (SCU), to ensure data coherency at the L2 shared cache of the ARM processors. All these ports can be individually enabled and configured. On the PL side, these interfaces are implemented using the existing reconfigurable logic, thus having an associated cost in terms of hardware resources.

4.2. Prototype Implementation

While the ARM processor on the PS is used to control the platform, the reconfigurable fabric on the PL is used to implement the dedicated co-processors and to support the interface with the biochip. The base software layer running in the PS is the Linaro Ubuntu GNU/Linux OS, which provides optimized tools and software packages for ARM SoCs. By adopting this OS, the PS provides a rich interface to the user by using the existing set of computer peripherals.

Figure 2 depicts the block diagram of the implemented architecture, considering a single-channel prototype. It corresponds to the initial zoom-in phase, where an FFT is computed over a small subset of sensors from a single acquisition channel to determine the binding frequency, f_{bind}, that maximizes the SNR. In the multi-channel implementation, where parallel channels read biological information of 1000+ sensors, the shaded area in Fig. 2 is replicated.

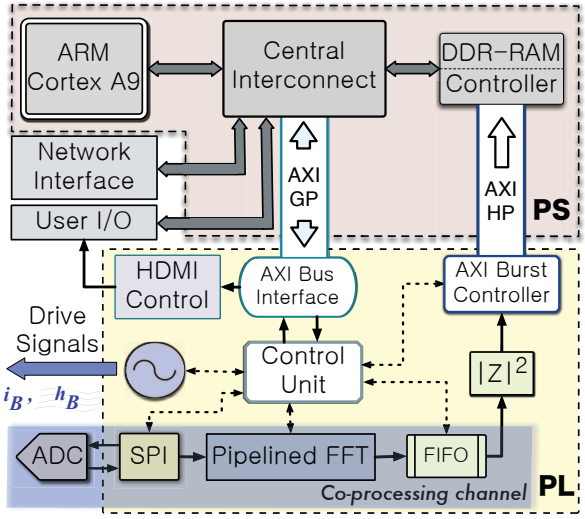

Fig. 2. Implemented prototype on a Zynq SoC device.

Several AXI interfaces connect the reconfigurable fabric to the ARM processor and to the associated main memory, either for control or for high throughput data transfers. By following the design strategy commonly adopted in DMA-based peripherals, each devised co-processor provides a slave interface for configuration purposes, along with a master controller that writes in the shared memory bus. Data consistency between the dedicated co-processors and the GPP is achieved by using a contiguous region in the main memory, marked as non-cacheable and excluded from the system's memory management. The OS is able to read this memory region by remapping the region into the kernel virtual address space, thus allowing it to be easily accessed by a custom device driver.

4.2.1. FFT co-processor

The FFT co-processors in the PL are based on the Xilinx FFT IP core v7.1, and adopt a pipeline operation to produce an output per clock cycle in a stream-based processing scheme. The cores are configured to receive 24-bit fixed-point real inputs, although a higher precision is used inside the cores to decrease numerical error propagation between intermediate stages. Furthermore, embedded DSP blocks are used in the butterfly computations, to allow for a better balance in the DSP/BRAM usage within the available reconfigurable fabric. As it will be shown in Section 5, a significant amount of BRAMs is needed for data and phase factor storage when the FFTs are computed with a high amount

of points. However, the adoption of the zoom-in approach allows to keep the total memory requirements per channel at reasonable levels. In all zoom-in levels, the synchronous reset and start bit signals are obtained from a control register, allowing for an operation fully controlled by the PS. Also, since the considered signal processing algorithm requires the squaring of the FFT complex output, an additional squaring block is introduced at FIFO output.

4.2.2. PL-PS Data Streaming and Interface

The communication between the several logic blocks on the reconfigurable fabric and the ARM GPP is ensured by specifically defined control and data channels. By following a memory-mapped I/O approach, a set of control registers are made accessible to the programs executing on the ARM, providing convenient software reset and start flags triggering functionalities. These registers are placed on an AXI bus, mastered by the CPU through an AXI-GP interface port. An AXI-HP port is used to transfer the FFT output frames directly to the main memory, where they can be subsequently accessed by the CPU. Since this shared memory region is contiguous and is not directly managed by the OS kernel (as explained above), an AXI Burst Master Controller is used to provide these co-processing channels with a direct memory access. This solution provides a data-transfer performance equivalent to a conventional DMA engine, but reduces the hardware requirements by approximately 7 times.

When multichannel processing is considered, the architecture in Fig. 2 is expanded to incorporate as many co-processing blocks as the number of channels (shaded block in the lower part of Fig. 2). The co-processing blocks are then connected to the AXI-HP port, which provides a communication channel between the co-processors and the main memory capable of supporting data transfers of up to 1.2 GByte/s (estimate). This is well above the 72 KBit/s bit-rate of the ADC in the previous biosensing platform implementation. Even considering that higher bit-rates are required for the new biosensing platform, this bandwidth is enough to support multiple channels (the next generation biochips will provide 4 channels), and still provides enough resources for future expansions. However, it should be noticed that a continuous data transmission must be assured to achieve a throughput of 1.2 GByte/s. To guarantee this requisite, a dual clock domain FIFO memory is used to implement a bridge between the FFT processing channels and the AXI-HP bus connected to the main memory (see Fig. 2).

4.2.3. System I/O and User Interface

Two different interfaces need to be supported by the biosensing platform: i) an SPI-based interconnection with each channel ADC and with stimuli generator, ii) the interface with the human operator. The connection to the biosensing ADC and with the stimuli generator are accomplished by an off-the-shelf and open-source core implementation of the SPI protocol, available at *OpenCores.org*. The selection of this particular core took into account its particular characteristics in terms of versatility and resource efficiency.

The user interface is accomplished by using the HDMI graphics port and an USB keyboard (the latter is planned to be replaced by an USB touch-screen panel). Although an HDMI interface already exists in the Zynq platform, the controller has to be implemented on the reconfigurable fabric. The controller module was obtained from a reference design targeting an HDMI output interface, along with the physical and data streaming blocks required to handle DMA video streams [7]. These DMA engines are connected to two separate AXI-HP ports, enabling them to directly gather video data from the main memory. The HDMI control logic (also on the PL side), is connected to an AXI-GP interface and mapped into the memory-space of the OS, allowing the usage of existing software device drivers.

Since the biosensing platform is not yet deployed on a clinical laboratory, its user interface is still focused on development purposes. Currently, it displays frequency spectrum of the biosensors signal and, from this, it measures the voltage amplitude at the binding frequency.

5. EXPERIMENTAL RESULTS

To properly evaluate the proposed scalable multichannel architecture, experimental results were obtained by using a ZedBoard featuring a Zynq XC7Z020, one of the smallest and less power demanding Zynq SoCs, and was synthesized and mapped using the Xilinx 14.3 development tools.

The presented analysis starts by considering a single channel architecture implementation with the largest allowed FFT core, which is used to determine, with maximum accuracy, the biosensors binding frequency region. Experimental results are presented in Table 1 and show that the FFT-size (64k samples) is limited by the amount of available block RAMs in the PL. Furthermore, the results show that the resources required by the remaining structure corresponds to only 33.5% of the available LUTs, only 8 BRAMs and 19 DSPs. From this, it can be concluded that the majority of the PL hardware resources are made available to be used by the co-processing channel(s).

To evaluate the scalability and adaptability of the pro-

Table 1. System resources for a single channel 64K FFT.

Component	**LUT** (53200)	**BRAM** (140)	**DSP48** (220)
64k FFT core	7157 (13.5%)	106 (75.7%)	103 (46.8%)
Squaring module	149 (0.3%)	0 -	16 (7.2%)
Drive signals (DDS)	174 (0.3%)	2 (1.4%)	3 (1.4%)
AXI wrapper	572 (1.1%)	0 -	0 -
SPI Master	131 (0.2%)	0 -	0 -
Core system	13857 (26.0%)	6 (4.3%)	0 -
Full system	25097 (47.2%)	114 (82.1%)	122 (55.4%)

Table 2. Co-processing channel hardware requirements.

FFT size *(#samples)*	Hardware resources (per channel) LUT (53200)		BRAM (140)		DSP48 (220)		Maximum #channels
1024	3686	(7%)	8	(6%)	24	(11%)	8
2048	4375	(8%)	11	(8%)	31	(14%)	6
4096	4765	(9%)	14	(10%)	31	(14%)	6
16384	7201	(14%)	28	(20%)	40	(18%)	4
32768	7916	(15%)	55	(39%)	49	(22%)	2
65536	7254	(14%)	106	(76%)	103	(47%)	1

posed architecture to the case when zoom-in is performed and multiple channels are required, bit-streams with smaller FFT cores were generated and the number of channels was maximized by balancing the usage of DSPs, BRAMs and LUTs. Table 2 presents the resources used by a single co-processing channel (i.e., the shaded block of Fig. 2), considering FFTs with increasing number of points, and the maximum number of co-processing channels supported on the PL. It should be noticed that for the 1k-, 2k- and 4k-FFT the maximum number of channels is constrained by the number of available DSP48 elements; for larger FFTs the limitation lies in the BRAMs. Also, in the 32k-FFT, to support 2 channels, some block RAMs were implemented using LUTs.

The presented results suggest that it is possible to achieve a multichannel processing system composed of 8 FFT channels of 1024 points. Hence, with up to 256 biosensors per channel, a total of 2048 biosensors can be processed and the sweep time is reduced by a factor of 8. This demonstrates the adaptability of the proposed system to multichannel processing, while keeping the required amount of hardware resources compatible with this entry level Zynq SoC. The FFT cores are capable of operating above 180 MHz, producing 1 output sample per clock cycle. Considering that the system must support an ADC sample rate of up to 4 Msps, which corresponds to the state of the art in high resolution converters, this suggests that the FFT cores do not impose any limitation to the signal analysis performance.

On the other hand, the AXI-HP allows an estimated maximum transfer rate of 1.2 GByte/s, while, for a data width of 32 bits, the FFT core outputs a bit-rate of at most 128 Mbit/s. Hence, the AXI-HP bandwidth does not limit the system operation, supporting multiple acquisition channels. Considering that the developed biochip prototype features 4 sensor blocks (1024 sensors), the bit rate could still be increased if faster ADCs become available.

From these results, it can be concluded that the proposed architecture, mapped on a Zynq SoC, provides the computational resources required to implement a fully embedded and high performance biosensing platform. Furthermore, the implemented prototype also demonstrated that a scalable and adaptable platform can be obtained with the existing reconfiguration capabilities, capable of adapting to biochips with higher sensor count and different computational needs.

6. CONCLUSION

New high density biochips are regarded as highly promising solutions for numerous applications, where high throughput analysis is required. However, existing electronic platforms are not able to acquire and process the higher amount of produced data. To tackle this problem, a novel scalable multi-channel and high-throughput architecture is proposed and implemented on a Zynq SoC. Even when using one of the smallest Zynq's, experimental results demonstrate that the system supports 8 times more sensors and a 1000+ times higher sampling frequency than the previous generation of the biosensing platform. By taking advantage of the reconfigurable characteristics of this SoC, results also suggest that the chosen platform allows to implement a scalable system supporting co-processors with configurable FFT sizes, enabling optimized and adjustable signal measurement for each biochip, without sacrificing efficiency in hardware resource usage, allowing the developed system to be expanded in order to deal with the requirements of future biochips.

7. ACKOWLEDGMENTS

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