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Review

Scalable Fabrication of 2D Semiconducting Crystals for Future Electronics

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Abstract: Two-dimensional (2D) layered materials are anticipated to be promising for future electronics. However, their electronic applications are severely restricted by the availability of such materials with high quality and at a large scale. In this review, we introduce systematically versatile scalable synthesis techniques in the literature for high-crystallinity large-area 2D semiconducting materials, especially transition metal dichalcogenides, and 2D material-based advanced structures, such as 2D alloys, 2D heterostructures and 2D material devices engineered at the wafer scale. Systematic comparison among different techniques is conducted with respect to device performance. The present status and the perspective for future electronics are discussed.

Keywords: 2D materials; transition metal dichalcogenides; field effect transistors; scalable synthesis; vapor phase deposition; 2D semiconducting alloys; 2D heterostructures; selective growth; multi-level stacked devices

1. Introduction

Two-dimensional (2D) layered materials, such as graphene, boron nitride (BN) and transition metal dichalcogenides (TMDCs), have attracted tremendous interest in extensive research fields [1–3], due to their general excellent electronic, optical and mechanical properties. It is widely accepted that 2D materials will play an important role in the applications of next-generation nanoelectronics [4–6],

optoelectronics [7,8], emerging (flexible, organic, printed and stretchable) electronics [9], energy conversion and storage [10], sensing [11] and medicine and biology [12]. As for the application in the upcoming high-end nanoelectronics, 2D materials possess unique electronic performance as compared with their bulk form (conventional three-dimensional (3D) materials) [13] and easy manipulation for complex structures as compared with the one-dimensional materials [14]. Recently, 2D semiconducting crystals, such as TMDCs and black phosphorous [15], have received increasing attention in electronic applications. At present, the majority of 2D semiconducting crystals lie in the family of TMDCs with the formula MX_2, where M is a transition metal element from Group IV (e.g., Ti, Zr or Hf), Group V (e.g., V, Nb or Ta) or Group VI (e.g., Mo or W), and X is a chalcogen (S, Se or Te) [2]. With a simple mechanical cleavage technique, monolayer (sub-nm thick) MoS_2 has been fabricated and used to demonstrate high-performance field-effect transistors (FETs) with room-temperature mobility ~200 $cm^2\ V^{-1}\ s^{-1}$ and a current on/off ratio ~10^8 [14], verifying the promise of 2D materials for nanoelectronics. However, in order to realize the transfer from lab-scale fabrication to industrial-scale manufacturing for future electronics, scalable synthesis techniques of 2D semiconducting crystals are indispensable.

A variety of scalable synthesis techniques for 2D TMDCs have been developed in the recent literature. In this review, we systematically introduce those techniques that produce highly-crystalline large-area 2D crystals and that have great potential for manufacturing in future nanoelectronics. There are also some other scalable synthesis techniques for nanosheets of 2D materials, such as solvent exfoliation [16] and inkjet printing [17,18]. Despite their promising applications in other fields, e.g., printed electronics and energy storage, they may not be suitable for high-end nanoelectronics and are not included in this review. Section 2 introduces scalable synthesis techniques for large-area (typically wafer-scale) monolayer or few-layer TMDCs. Section 3 introduces the advanced engineering of 2D TMDCs, including 2D TMDC alloys, 2D heterostructures and wafer-scale fabrication of 2D TMDC devices. In Section 4, we benchmark the performance of TMDC FETs based on different scalable synthesis techniques against those based on mechanical cleavage, and offer an outlook for the research tendency in the near future.

2. Scalable Synthesis Techniques for TMDCs

Here, we briefly introduce the recently-developed synthesis techniques for wafer-scale TMDCs, including vapor phase deposition, thermal decomposition, magnetron sputtering and molecular beam epitaxial.

2.1. Vapor Phase Deposition

Currently, the predominant and most promising scalable synthesis technique for large-area atomically-thin TMDCs is vapor phase deposition (VPD). In general, VPD relies on the chemical reaction or physical transport (often with inert gas as the carrier) of vaporized precursors to deposit TMDCs onto the substrate surface. In terms of the initial precursor state, VPD can be classified into solid-precursor VPD and gas-precursor VPD.

2.1.1. Solid-Precursor VPD

So far, most of the VPD techniques are based on solid-state precursors. Usually, transition metal, metal oxides or chlorides, such as MoO_3, $MoCl_5$ and WO_3, act as the metal precursors, while S/Se powders as the chalcogen precursors [19]. Solid-precursor VPD has been widely employed to synthesize not only pure 2D TMDC crystals, but also TMDC alloys and heterostructures, to be discussed in Section 3. As illustrated in Figure 1, three classes of solid-precursor VPD techniques have been demonstrated in the literature [20]: (1) simple chalcogenization of predefined metal (or metal oxide) film (Figure 1a), where metal or metal oxide thin films are first deposited onto the substrates, then chalcogen powers are heated to be vapors and transported to the substrates and, finally, the metal/metal oxide films are annealed at the atmosphere of chalcogen vapors to produce TMDCs; (2) chemical vapor deposition (CVD) based on the reaction between metal precursors and chalcogen precursors (Figure 1b), where both solid metal precursors and chalcogen powders are heated separately into the vapor phase, and are transported to and react on the substrate surface to form 2D TMDC crystals; and (3) vapor-solid growth based on vapor phase transport and recrystallization of TMDCs (Figure 1c), where TMDC powders serve as the precursors which are vaporized and transported to the cool substrate region and recrystallize to 2D crystals.

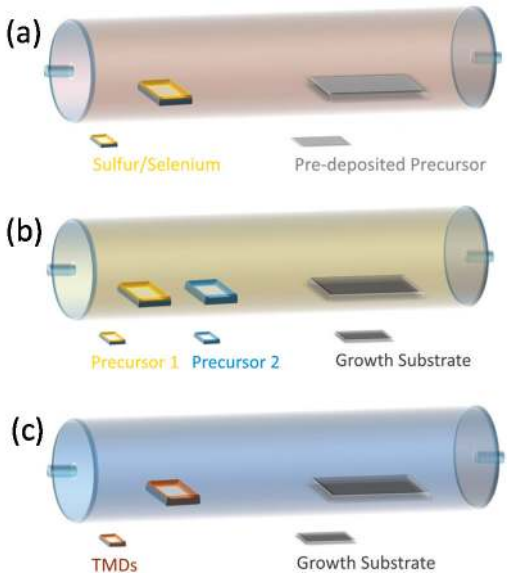

Figure 1. Schematic of three types of solid-precursor vapor phase deposition techniques for scalable synthesis of large-area transition metal dichalcogenides (TMDCs). (**a**) Vapor phase chalcogenization of pre-deposited precursor (metal, metal oxide, *etc.*) film; (**b**) chemical vapor deposition; (**c**) physical vapor deposition. Adapted with permission from [20]. Copyright 2015, The Royal Society of Chemistry.

The principle and methodology of the solid-precursor VPD techniques have been elaborated in a recent relevant review by Shi *et al.* [20]. In general, TMDCs synthesized through chalcogenization of predefined metal/metal oxide film (Class (1)) give rise to low carrier mobility (<0.1 $cm^2 V^{-1} s^{-1}$) [20,21]. In contrast, the chemical reaction-based synthesis (Class (2)) is more favorable because of the technique's simplicity, preference for monolayer growth and typically high mobility over

10 cm^2 V^{-1} s^{-1} [20,22]. For all of the techniques, a critical challenge is the limited spatial uniformity. In most cases, spatially inhomogeneous mixtures of monolayer, multi-layer and no-growth regions are obtained [23]. In this section, we focus on the introduction of recent innovative strategies that lead to higher uniformity and/or better controllability.

Pre-treated substrates: Most studies on VPD synthesis use SiO_2 as the growth substrates. However, because of the amorphous nature of the SiO_2 substrate and its relatively high surface roughness, the obtained TMDCs usually suffer from high-density grain boundaries and random orientation among domains. This inevitably generates severe non-uniformity and hinders the scalable growth of large-area high-quality 2D TMDCs. One effective solution is to use an atomically-smooth crystalline substrate [22] to control the crystallographic orientation of TMDC domains during growth and to attain a uniform layer with reduced grain boundary density.

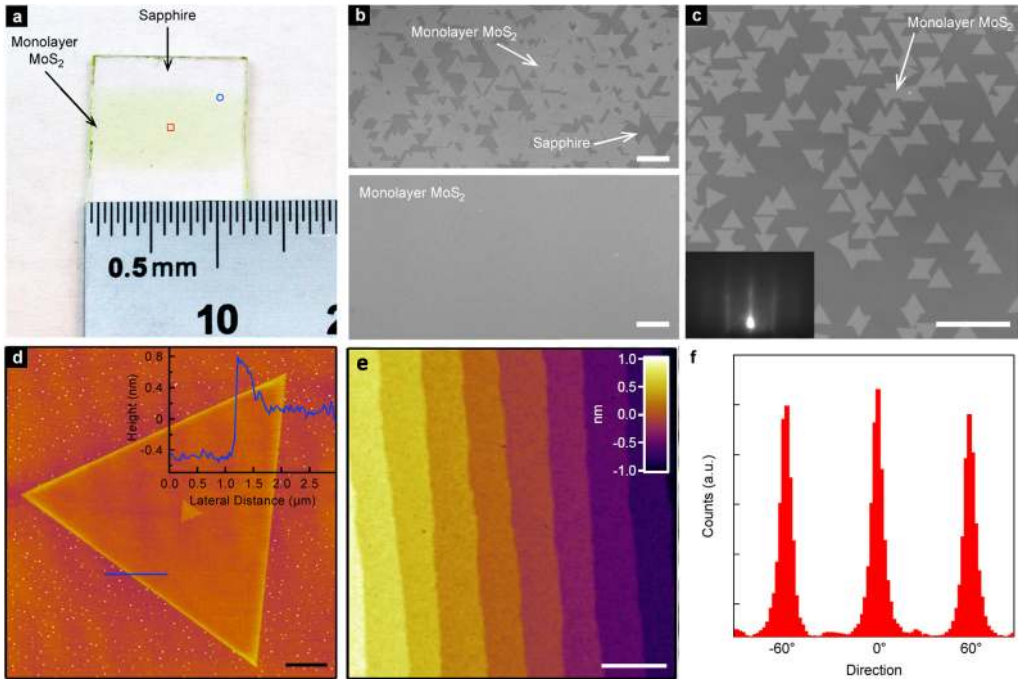

Figure 2. Monolayer MoS_2 growth on sapphire with controlled lattice orientation. (**a**) Photograph of centimeter-scale MoS_2 film on sapphire; (**b**) optical microscope images of the sample in (**a**) at the edge region (top, the circle region in (**a**), scale bar: 20 μm) and the center region (bottom, the square region in (**a**), scale bar: 10 μm); (**c**) optical microscope images of the grown monolayer MoS_2 grains, scale bar: 50 μm; the inset is a reflection a high-energy electron diffraction (RHEED) pattern showing a long-range structure order; (**d**) atomic force microscope (AFM) image of a monolayer MoS_2 grain (inset: thickness profile along the blue line; scale bar: 2 μm); (**e**) AFM image of annealed sapphire as the growth substrates, where atomically-smooth terraces occurs on the surface (scale bar: 100 nm); (**f**) the orientation histogram based on the area shown in (**c**) confirms good control over lattice orientation. Adapted with permission from [24]. Copyright 2015, American Chemical Society.

Sapphire is a suitable substrate for CVD growth of TMDCs [24,25]. In particular, Dumcenco *et al.* [24] have recently achieved good control over lattice orientation (Figure 2) during CVD growth (based on the reaction between vaporized MoO_3 and sulfur) and obtained high-quality monolayer MoS_2 with

centimeter-scale uniformity (Figure 2a,b). The key to the lattice orientation is the introduction of terraces on the sapphire surface (Figure 2e) via annealing in air at an elevated temperature of 1000 °C prior to the growth process. The CVD growth produces well-defined equilateral triangular single-crystal domains (Figure 2d) that merge into a continuous monolayer film with a typical coverage area of 6 mm × 1 cm in the center of the sapphire substrate (Figure 2b). In addition, over 90% of domains (Figure 2c,f) are well aligned with the relative edge orientation at multiples of 60°. A striking merit of the technique is that the relatively weak van der Waals interaction between sapphire and MoS_2, on the one hand, effectively induces lattice alignment, while on the other hand, allows easy transfer of the grown MoS_2 from the sapphire substrate to silicon wafers, which facilitates the fabrication of high-performance FETs. As a result, a high mobility of about 43 $cm^2\ V^{-1}\ s^{-1}$ has been attained for devices based on single grains of the grown MoS_2. Even for devices based on the large-area MoS_2 films, which contain grain boundaries, the mobility still retains about 25 $cm^2\ V^{-1}\ s^{-1}$. In particular, there is no evident mobility degradation when the channel length increasing from 4 μm to ~80 μm.

In addition to sapphire substrates, Najmaei *et al.* [21] developed a CVD process to grow centimeter-scale MoS_2 film directly on patterned SiO_2/Si wafers. Based on the observation that MoS_2 triangular domains and films are commonly nucleated and formed in the vicinity of substrates' edges, scratches, dust particles or rough surfaces, they used conventional lithography to strategically create step edges by patterning SiO_2/Si substrates with a uniform distribution of square SiO_2 pillars, as shown in Figure 3a. The pillars facilitate a high density of domain nucleation, and the continued growth allows the formation of large-area continuous film. The MoS_2 films, grown on both the pillar surface and the valley space in between (Figure 3b,c), are predominantly single layered (multiple layers typically accumulate at the preferred nucleation sites). The synthesized MoS_2 films can be readily transferred to other substrates (Figure 3d) or directly applied to fabricate devices. FETs based on these MoS_2 films can exhibit average mobility of about 4.8 $cm^2\ V^{-1}\ s^{-1}$ and a maximum on/off current ratio approaching 6×10^6.

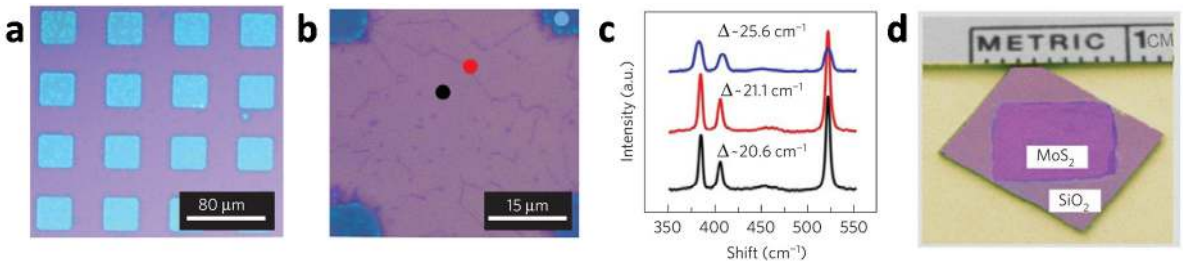

Figure 3. Controlled nucleation for CVD growth of large-area MoS_2 growth films on patterned SiO_2/Si substrates. (**a**) Optical image of a large-area continuous MoS_2 film on substrates with patterned square SiO_2 pillars; (**b**) the close-up view indicating monolayer and bilayer MoS_2 films in between pillars and a thicker MoS_2 film on top of pillars; (**c**) Raman spectra acquired at different regions in (**b**) confirming the thickness of the sample; (**d**) centimeter-scale MoS_2 film transferred to a new substrate. Adapted with permission from [21]. Copyright 2013, Nature Publishing Group.

Seeding promoters: In order to improve the uniformity of CVD-grown TMDC films directly on SiO_2/Si substrates, a simple and effective strategy is to use seeding promoters (Figure 4) [22,26]. In 2012, Lee *et al.* [26] obtained uniform, large-area monolayer MoS_2 by spinning aqueous solutions of

graphene-like molecules, such as reduced graphene oxides (rGO), perylene-3,4,9,10-tetra-carboxylic acid tetra-potassium salt (PTAS) and perylene-3,4,9,10-tetracarboxylic dianhydride (PTCDA), as the seeding promoters onto the SiO_2/Si substrates prior to growth. Later on, Ling *et al.* [22] identified more aromatic molecules, such as copper phthalocyanine (CuPc) and bathocuproine (BCP), as effective promoters. In particular, in contrast to the previous seeding promoters deposited via aqueous solution [26], the newly-identified seeding promoters can be deposited by thermal evaporation to various substrates, including hydrophobic substrates, to allow direct growth of a variety of hybrid structures (e.g., MoS_2/Au, MoS_2/BN and MoS_2/graphene). Besides, PTAS has also been used as seeding promoters for scalable synthesis of WS_2 [27]. However, possibly because of the presence of grain boundaries, back-gate FETs based on such TMDCs only attain a carrier mobility up to 1.2 $cm^2\ V^{-1}\ s^{-1}$ for MoS_2 and 0.01 $cm^2\ V^{-1}\ s^{-1}$ for WS_2, in spite of a high on/off ratio above 10^5 [27].

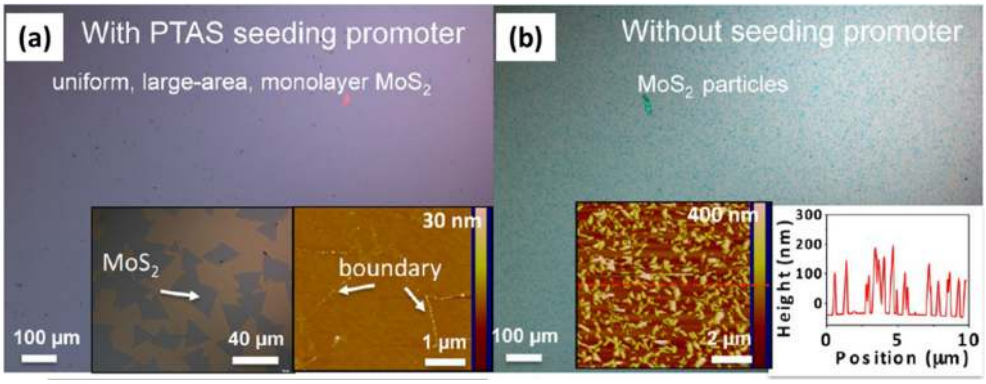

Figure 4. The effects of seeding promoter on the CVD growth of MoS_2 films. (**a**) Optical image of MoS_2 film grown on SiO_2/Si substrate with perylene-3,4,9,10-tetra-carboxylic acid tetra-potassium salt (PTAS) seeding promoter; (**b**) optical image of MoS_2 film grown on bare SiO_2/Si substrate without seeding promoter. The insets show a close-up view through optical or AFM images. Adapted with permission from [22], Copyright 2014, American Chemical Society.

Atomic layer-deposited precursors: In order to obtain layer-controlled wafer-scale WS_2 atomic layers on SiO_2/Si substrates, Song *et al.* [28] introduced an innovative synthesis technique through sulfurizing the WO_3 film prepared by atomic layer deposition (ALD). The precursor WO_3 film is first deposited on SiO_2/Si substrates by the ALD process and then sulfurized through the VDP technique (Figure 5a). Benefiting from the excellent controllability of the ALD process, the synthesis of WS_2 films exhibits systematic layer controllability, good reproducibility, wafer-level thickness uniformity and high conformity. In particular, the number of final WS_2 layers can be well controlled by controlling the number of the ALD cycles during WO_3 deposition. With 20, 30 and 50 ALD cycles, mono-, bi- and tetra-layer WS_2 are obtained, respectively (Figure 5b–g). Wafer-scale (2 cm × 13 cm) thickness uniformity has been demonstrated for all of the mono-, bi- and tetra-layer WS_2 films (Figure 5h,i). Top-gate FETs based on the WS_2 films exhibit high mobility of about 3.9 $cm^2\ V^{-1}\ s^{-1}$ with an on/off current ratio around 10^3.

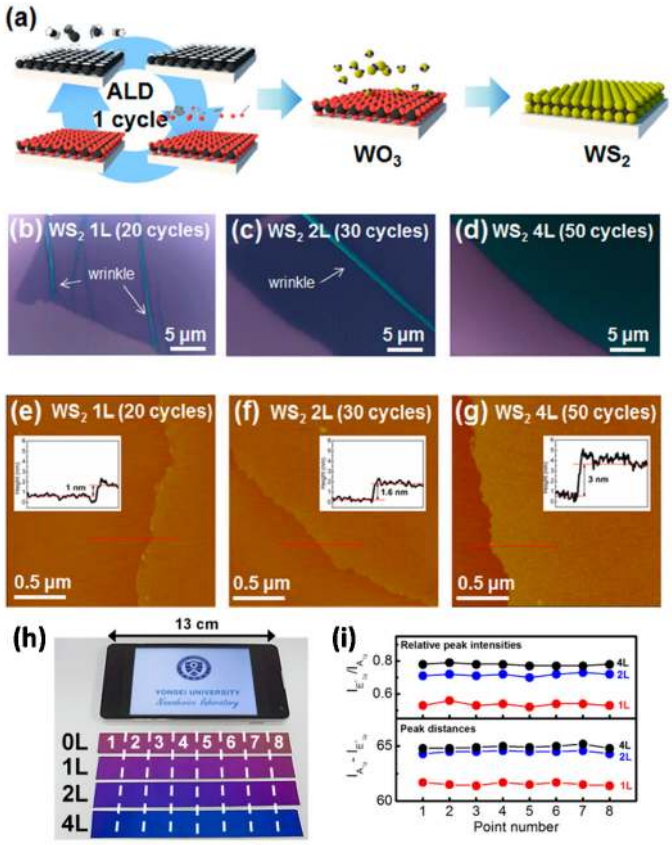

Figure 5. Atomic layer deposition (ALD)-based layer-controlled CVD growth of WS_2 films with precursors. (**a**) Schematic of the synthesis procedure; (**b**–**d**) optical microscope images and (**e**–**g**) AFM images and height profile (insets) of the mono-, bi- and tetra-layer WS_2 films transferred onto SiO_2 substrates, respectively; (**h**) wafer-sale (about 13 cm, comparable to the size of a cellular phone display screen) mono-, bi- and tetra-layer WS_2 films on SiO_2 substrates; (**i**) Raman peak intensity ratio (top) and peak distance (bottom) of the E^1_{2g} and A_{1g} bands for the WS_2 films at eight different measurement positions in (h) indicating the wafer-scale uniformity. Adapted with permission from [28]. Copyright 2013, American Chemical Society.

Oxygen plasma treatment: Besides the layer-controlled synthesis by ALD-deposited precursors, Jeon *et al.* [29] have recently developed another facile layer-controlled CVD growth technique for wafer-scale MoS_2 film on silicon substrates. Prior to the growth, the SiO_2/Si substrates are treated with oxygen plasma. With the low pressure CVD process, uniform MoS_2 film can be obtained in a large area (Figure 6a). In contrast, on untreated SiO_2/Si substrates, only small-scale (<100 nm) triangular MoS_2 nanoparticles are synthesized. Besides, by changing the duration of the oxygen plasma treatments, different MoS_2 layers can be adjusted in a controllable manner. With treatment durations of 90 s, 120 s and 300 s, mono-, bi- and tri-layer MoS_2 films have been obtained, respectively (Figure 6b–g). All back-gate FETs based on these MoS_2 show a high on/off current ratio between 10^5 and 10^6. The carrier mobility increases with the layer number, which is 3.6 $cm^2\ V^{-1}\ s^{-1}$, 8.2 $cm^2\ V^{-1}\ s^{-1}$ and 15.6 $cm^2\ V^{-1}\ s^{-1}$ for the mono-, bi- and tri-layer MoS_2 transistors, respectively. However, one may notice that the residual oxygen caused by the plasma treatment may impact the quality of the grown MoS_2 [30].

Further cleaning of the plasma-treated SiO_2/Si wafers (e.g., through purging with Ar at high temperature [29]) might be necessary to obtain high crystallinity.

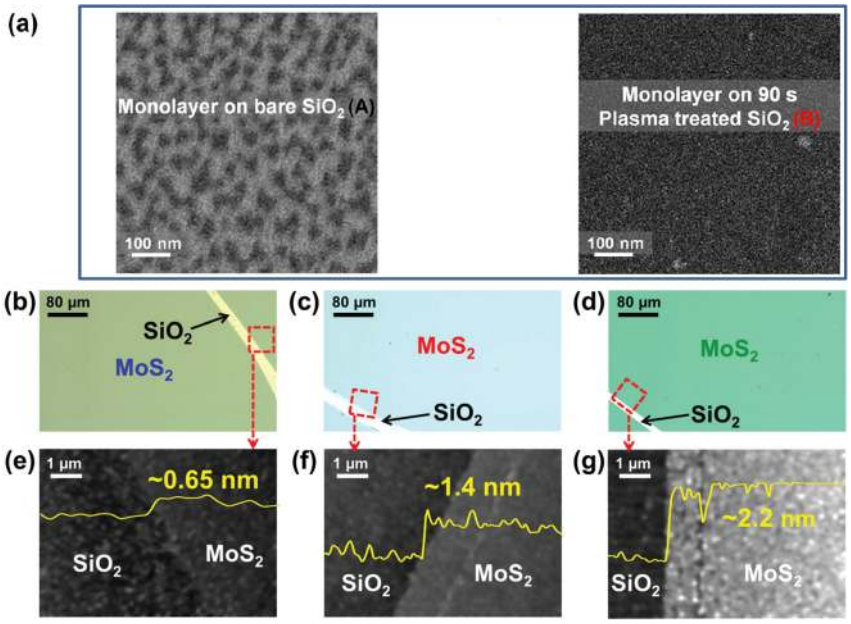

Figure 6. Layer-controlled CVD growth of MoS_2 film on plasma-treated SiO_2 substrates. (**a**) Scan electron microscope (SEM) images of the grown MoS_2 film on bare (left) and plasma-treated (right) SiO_2 substrates; (**b**–**d**) optical microscope images and (**e**–**g**) AFM images for the uniform mono-, bi- and tri-layer MoS_2 films, respectively. Adapted with permission from [29]. Copyright 2015, The Royal Society of Chemistry.

Self-limiting CVD: Yu *et al.* [31] developed a simple self-limiting CVD process to grow centimeter-scale MoS_2 films with precisely-controlled layer number ranging from 1–4. Highly uniform MoS_2 films (Figure 7) are synthesized on various substrates, including silicon oxide, sapphire and graphite. The MoS_2 films are grown at a high temperature (>800 °C) with $MoCl_5$ and sulfur as the precursors. At high temperature, precursors react to produce MoS_2 species, which then precipitate onto the substrates to form MoS_2 films. The layer number of the MoS_2 films is precisely controlled by the amount of $MoCl_5$ used in the source or the total pressure during the growth process. The greater the amount of $MoCl_5$ or the higher the total pressure used, the larger the layer number of MoS_2 films obtained. The obtained large-area, highly-uniform MoS_2 thin films suggest that the growth is a self-limiting process, *i.e.*, the growth automatically stops once the formation of each individual layer finishes. The self-limiting mechanism may lie in a thermodynamic balance between the partial pressure of gaseous MoS_2 species (P_1) and the vapor pressure of MoS_2 thin films on the substrate (P_2). P_2 could increase with the layer number. The initial force of $P_1 > P_2$ drives the formation of monolayer MoS_2. When the growth of the monolayer finishes, P_2 increases, and the driving force $P_1 > P_2$ may vanish, so that the growth ceases. To grow more layers, higher P_1 should be introduced. Therefore, the layer number can be well controlled by the precursor amount and environmental pressure. However, for thicker MoS_2 films, precise control becomes more difficult. Back-gate FETs based on monolayer MoS_2 films exhibit carrier mobility ranging from 0.003–0.03 $cm^2\ V^{-1}\ s^{-1}$.

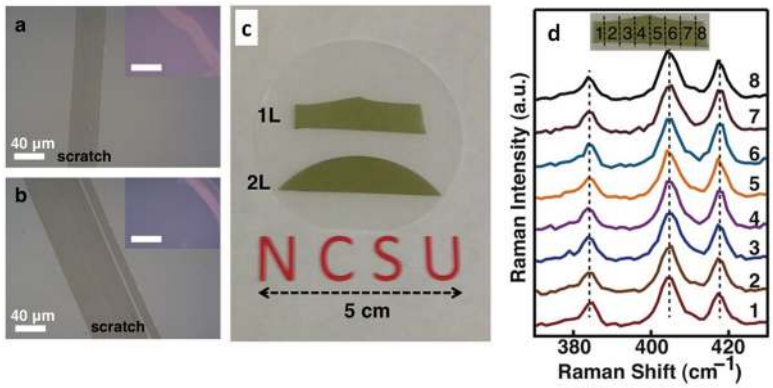

Figure 7. Controlled synthesis of monolayer and bilayer MoS_2 films by self-limiting CVD. Optical microscope images of highly uniform (**a**) monolayer and (**b**) bilayer MoS_2 films (scale bars in insets: 80 μm); (**c**) photograph of as-grown large-area monolayer and bilayer MoS_2 films; (**d**) Raman spectra acquired at different locations indicating the homogeneity. Adapted with permission from [31]. Copyright 2013, Nature Publishing Group.

Immediate-state precursor: Usually, CVD synthesis for MoS_2 is based on MoO_3 as the initial metal precursor. During growth, however, the conversion from MoO_3 to MoS_2 involves one intermediate step. MoO_3 is first partially reduced by the sulfur to a volatile state MoO_{3-x}, and then, MoO_{3-x} is further reduced to MoS_2. The incomplete reaction (partial reduction) may produce an uncontrollable intermediate phase, which provides extra binding sites to chemisorb oxygen. The absorbed oxygen can generate defects/vacancies in the final MoS_2 flakes and significantly degrade their electrical performance. To diminish the impacts arising from the intermediate chemistry, Bilgin *et al.* [30] developed a CVD process with MoO_2 powders as the metal precursor and directly sulfurized MoO_2 in the vapor phase. With this technique, monolayer, as well as few-layer MoS_2 with an edge-size (Figure 8) ranging from 10–50 μm have been grown in various substrates, including amorphous SiO_2, crystalline Si wafer, transparent quartz and silicon nitride, as well as conductive graphene. Through transferring the as-grown monolayer MoS_2 onto SiO_2/Si substrates and building up back-gate device structures, the obtained FETs exhibit excellent performance of high mobility of about 35 $cm^2\ V^{-1}\ s^{-1}$, and a large on/off current ratio about 10^8.

2.1.2. Gas-Precursor VPD

In addition to the solid-precursor VPD, conventionally with sulfur (or selenium) powder as the precursor, recent studies have also employed gas state precursors to improve the controllability during the course of VPD growth.

Cycle-based epitaxy on gold: Large-area epitaxial monolayer MoS_2 films have been recently grown on a Au(111) surface [32] under ultrahigh vacuum with H_2S gas and e-beam evaporated Mo as the precursors (Figure 9a). The synthesis is based on growth cycles, each of which consists of two sequent steps, Mo evaporation and sulfurization by H_2S gases. Upon the finishing of one growth cycle, the H_2S gases are pumped out, and the chamber is prepared for a second growth cycle. The first growth cycle is to nucleate MoS_2 nano-islands (Figure 9c), and the following cycles gradually increase the island size (Figure 9d,e). The growth cycles are repeated until a continuous film forms with coverage approaching

unity. Without such a cycle-based synthetic process, it is challenging to obtain high-coverage uniform MoS_2, since a single long Mo deposition in a H_2S atmosphere only produces low quality sub-monolayer films.

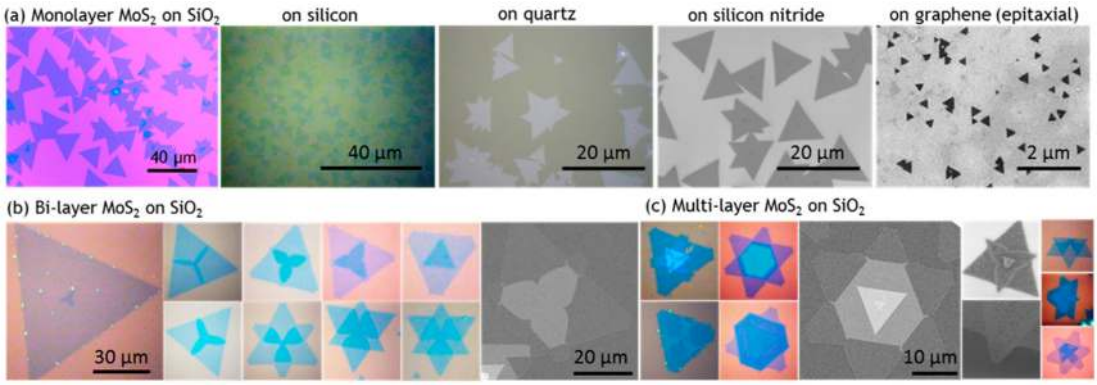

Figure 8. Optical (colored) and SEM (grey) images of (**a**) monolayer, (**b**) bilayer and (**c**) multi-layer MoS_2 films on various substrates grown by CVD with MoO_2 as the metal precursor. Reprinted with permission from [30]. Copyright 2015, American Chemical Society.

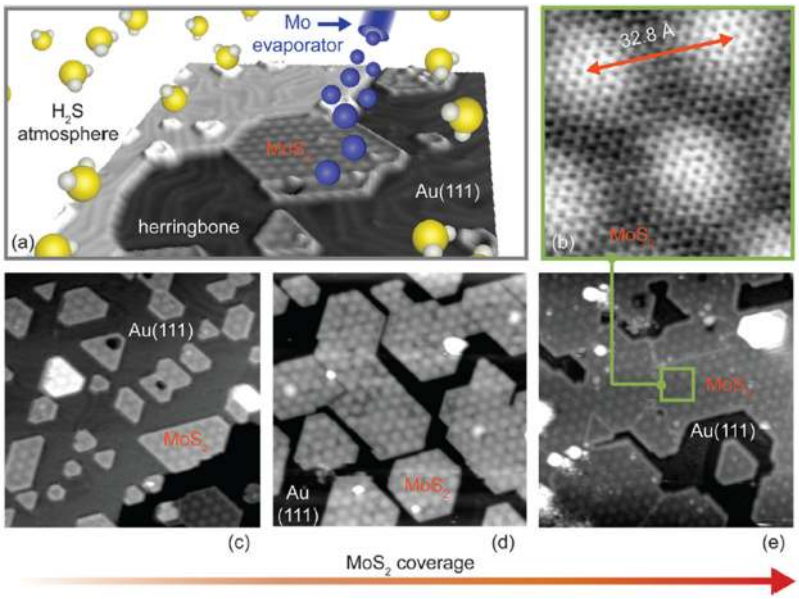

Figure 9. (**a**) Schematic of cycle-based epitaxy of MoS_2 on gold; (**b**) high resolution scan tunneling microscope (STM) image of the moiré lattice of MoS_2; (**c**–**e**) STM images acquired at different growth times. Reprinted with permission from [32]. Copyright 2015, American Chemical Society.

All-gas precursor CVD: Kang *et al.* [23] have developed a metal-organic chemical vapor deposition (MOCVD) technique to grow monolayer MoS_2 and WS_2 films with safer-scale homogeneity. Remarkably, only gas-phase precursors (Figure 10a) are used in the technique, including $Mo(CO)_6$ or $W(CO)_6$ as the metal precursors, $(C_2H_5)S$ as the sulfide precursors and H_2 to remove carbonaceous species generated during the MOCVD growth. All of the gases are diluted in the carrier gas, argon, so that their concentration can be precisely controlled throughout the growth period by regulating the corresponding partial pressure. In this way, the MoS_2 film is grown layer by layer, which is ideal for uniform layer control over a large scale. Figure 10b reveals the controllable growth process at different

times: initial nucleation on the SiO_2 surface ($t = 0.5t_0$), monolayer growth ($0.8t_0$), maximum monolayer coverage (t_0), secondary nucleation mainly at grain boundaries ($1.2t_0$) and bilayer growth ($2t_0$). In addition, the average grain size and inter-grain connection can be well controlled by the concentrations of H_2, $(C_2H_5)_2S$ and residual water (Figure 10c). The wafer-scale growth of a high-quality monolayer MoS_2 film allows mass production of 8100 FETs (Figure 10d) on a four-inch SiO_2/Si wafer with a yield as high as 99% and excellent electrical performance of the on/off current ratio of ~10^6 and mobility of ~29 $cm^2\ V^{-1}\ s^{-1}$. Similar devices based on a CVD-grown WS_2 monolayer also exhibit a high on/off current ratio of ~10^6 and mobility of ~18 $cm^2\ V^{-1}\ s^{-1}$.

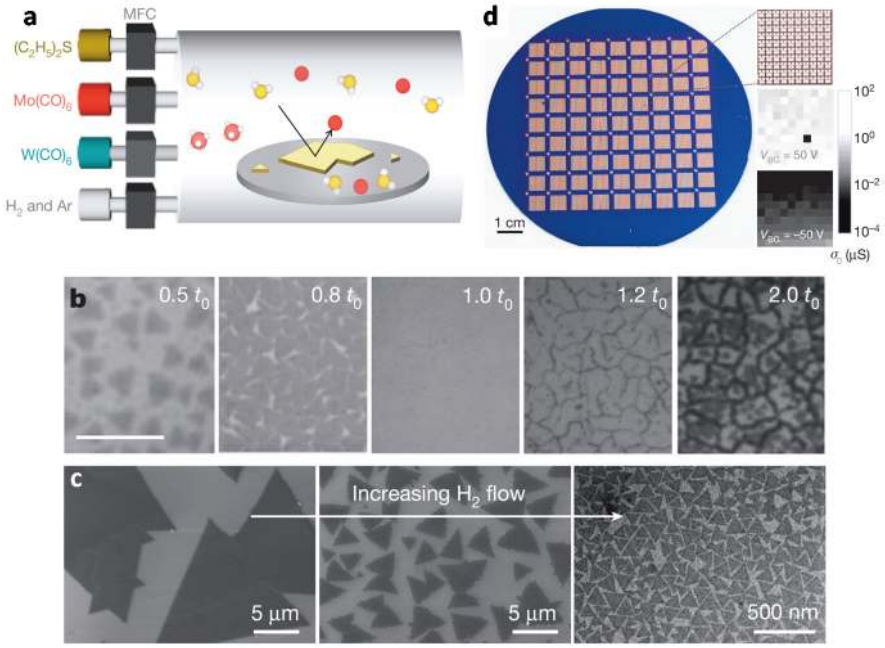

Figure 10. All-gas precursor metal-organic chemical vapor deposition (MOCVD) growth of continuous large-area MoS_2 film and device fabrication. (**a**) Diagram of the MOCVD setup; (**b**) optical images of the grown MoS_2 films at different growth times, where t_0 is the optimal growth time for full monolayer coverage (scale bar: 10 μm); (**c**) the effects on the H_2 flow rate on the grown MoS_2 grains; (**d**) mass production of 8100 MoS_2 FETs on a four-inch SiO_2/Si wafer. Adapted with permission from [23]. Copyright 2015, Nature Publishing Group.

2.2. Thermal Decomposition

In addition to the VPD techniques, other techniques have also been developed for scalable synthesis of 2D TMDC materials.

In 2011, Liu *et al.* [33] developed a thermal decomposition technique to produce large-area MoS_2 thin layers on insulating substrates (Figure 11). First, a thin and uniform film of the precursor, ammonium thiomolybdates, $(NH_4)_2MoS_4$, is coated onto insulating substrates (sapphire or SiO_2/Si wafer) through dip coating. Then, the precursor is annealed and converts to MoS_2. The annealing process comprises a first low-pressure (1 Torr) annealing at 500 °C in the presence of H_2 for the decomposition of $(NH_4)_2MoS_4$ to MoS_2 and a second high-pressure (500 Torr) annealing at 1000 °C in an atmosphere

of Ar (or a mixture of Ar and sulfur) to improve crystallinity and/or increase the grain domain size. Typically, uniform and continuous bi- or tri-layer MoS_2 films are obtained throughout the substrates (Figure 11). Bottom-gate FETs based on the synthesized MoS_2 annealed under the atmosphere of Ar and S exhibit a current ratio up to 1.6×10^5 and a mobility up to 4.7 $cm^2\ V^{-1}\ s^{-1}$.

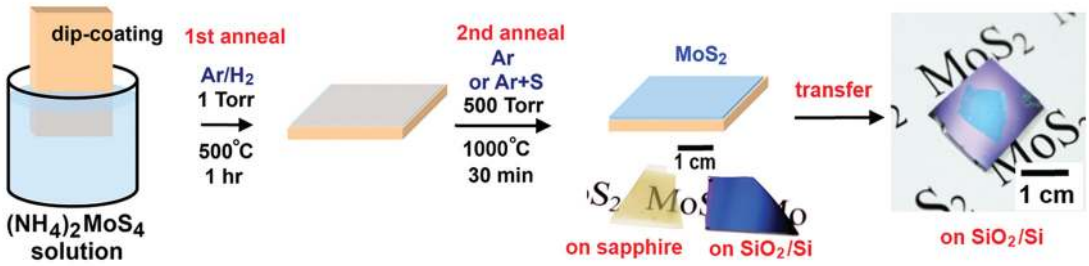

Figure 11. Schematic of the thermal decomposition process for the growth of MoS_2 films on insulating substrates. Adapted with permission from [33]. Copyright 2012, American Chemical Society.

2.3. Magnetron Sputtering

Tao *et al.* [34] recently developed a one-step magnetron sputtering technique to synthesize wafer-scale MoS_2 atomic layers on various substrates. As illustrated in Figure 12b, the growth is based on the reaction between vaporized S and sputtered Mo. Sulfur is first vaporized and then transported to the chamber, where the metal target is sputtered in an Ar atmosphere by a low power. The sputtered Mo is more reactive than Mo or MoO_3 in CVD processes and can easily react with the vaporized S. After the reaction, the product is deposited onto the hot substrate to form MoS_2 layers. Because of the low sputtering power, the growth rate is very low. Therefore, mono- or few-layer MoS_2 can be obtained in a controllable manner by adjusting the sputtering power or deposition time. Since magnetron sputtering is compatible with large-scale production, highly-homogeneous MoS_2 flakes with dimensions up to centimeter scale (Figure 12a) are obtained with a controllable layer number of 1, 2, 3 and more. The back-gate FETs based on the grown MoS_2 exhibit a p-type behavior with an on/off current ratio of about 10^3 and an average mobility of about 7 $cm^2\ V^{-1}\ s^{-1}$.

2.4. Molecular Beam Epitaxy

Recently, Yue *et al.* [35] developed a molecular beam epitaxy (MBE) to grow one 2D TMDC ($HfSe_2$) on another 2D material (highly-ordered pyrolytic graphite (HOPG) or MoS_2). Although MBE was introduced for hetero-epitaxial growth of TMDC (e.g., $NbSe_2$) three decades ago, few studies have demonstrated the MBE growth of 2D $HfSe_2$ on another 2D material to fabricate an all-2D heterostructure. Hf-based TMDCs have a small band gap, a large work function and reasonable mobility and, hence, are promising for a variety of applications in nanoelectronics and optoelectronics. In Yue's processing, the $HfSe_2$ films are grown on mechanically-exfoliated HOPG and MoS_2 through a VG-Semicon V80H molecular beam epitaxy system, where the growth chamber is equipped with a vertical e-beam evaporator to allow the growth of high melting-point metals (Hf, Ti, Mo, W, *etc.*) in addition to effusion cell evaporation of the chalcogen. Prior to growth, the substrates are cleaned by

heating for 2 h in the growth chamber, and the Hf and S sources are cleaned by outgassing. During the growth, the Se and Hf shutters were opened and closed simultaneously, and the Se:Hf flux was maintained at a ratio of 5:1. As shown in Figure 13, the interface is atomically sharp, and there are no detectable misfit dislocations or strains between the MBE-grown $HfSe_2$ and the HOPG or MoS_2 underneath, in spite of the large lattice mismatch (41% and 17%, respectively). The grains are typically larger than 100 nm × 100 nm, and the layer number depends on the growth time. The grown $HfSe_2$ is slightly n-type with a band gap of about 1.1 eV.

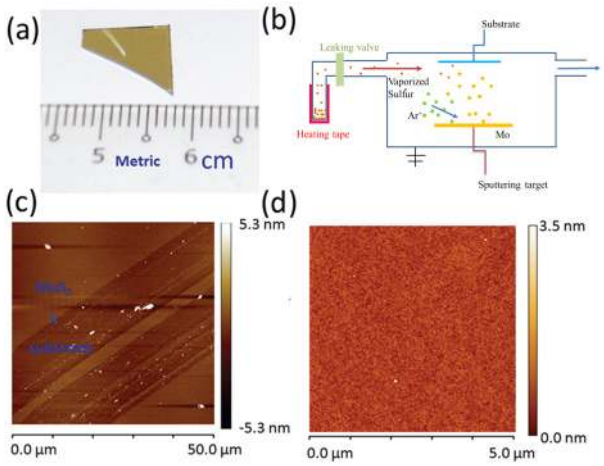

Figure 12. Large-area uniform MoS_2 film grown on sapphire by magnetron sputtering. (**a**) Photograph of a centimeter-scale film; (**b**) schematic of the magnetron sputtering growth process; (**c**) AFM image of as-grown MoS_2 film showing a clear film edge; (**d**) a close-up view of the AFM image showing good uniformity. Adapted with permission from [34]. Copyright 2015, The Royal Society of Chemistry.

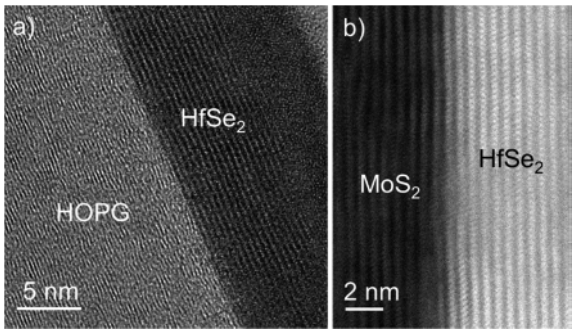

Figure 13. Transmission electron microscope (TEM) images of epitaxial $HfSe_2$ on (**a**) highly-ordered pyrolytic graphite (HOPG) and (**b**) MoS_2 with a sharp interface and layered crystallinity. Reprinted with permission from [35]. Copyright 2015, American Chemical Society.

3. Advanced Engineering for Materials, Heterostructures and Devices

As the scalable synthesis of 2D TMDC becomes mature, more and more techniques have been developed to allow advanced engineering in TMDC-based electronics at different levels, from synthesis

of the TDMC alloys (material level), to fabrication of various 2D heterostructures, to controllable and batch production of electronic devices at the wafer scale.

3.1. TMDC Alloys

Both theoretical calculation and experiments have demonstrated that the band gap of 2D TMDC alloys can be modulated in a wide spectrum range by changing the composition [36]. This is a desired property for many applications in electronic and optoelectronics and has stimulated great efforts in controllable fabrication of various 2D TMDC alloys. So far, two types of alloys have been synthesized through scalable VDP techniques. One is a mixture of chalcogens, e.g., $MoS_{2(1-x)}Se_{2x}$ alloys, and the other is a mixture of metals, e.g., $Mo_{1-x}W_xS_2$ alloys.

3.1.1. $MoS_{2(1-x)}Se_{2x}$ Alloys

Two CVD processes have been developed for scalable synthesis of $MoS_{2(1-x)}Se_{2x}$ alloys. One [37,38] uses $MoSe_2$ and MoS_2 powders as the precursors, which are placed separately, as illustrated in Figure 14a. The precursors are directly vaporized at a high temperature (940–975 °C), while the SiO_2/Si substrate is put in a relatively low temperature (600–700 °C) region. In order to optimize the supersaturation for the nucleation process, a moderately high temperature gradient of about 50 °C/cm in the substrate (deposition) region is applied [37,38]. Too low of a temperature gradient (<30 °C/cm) may suffer from insufficient supersaturation and nucleation for the alloy growth [37], whereas too high of a temperature gradient (>80 °C/cm) may cause surplus nucleation, which greatly reduces the domain size of the monolayer alloy [38] or even changes the morphology to a fiber-like structure [37]. By finely adjusting the evaporation temperature, the temperature gradient and the H_2 flow rate in the carrier gas, high-quality centimeter-scale $MoS_{2(1-x)}Se_{2x}$ monolayer alloy can grow on the substrate (Figure 14b). By fixing the evaporation temperature of MoS_2 at 940 °C and increasing the evaporation temperature of $MoSe_2$ from 940–975 °C, the composition in the $MoS_{2(1-x)}Se_{2x}$ alloy can be finely controlled with x ranging from 0–0.4. However, at an even higher evaporation temperature (>975 °C), $MoSe_2$ tends to decompose, and it becomes hard to further increase x in the alloy. Nevertheless, if extra Se vapor is introduced into the upstream of the furnace, more Se-rich alloy with $0.4 < x < 1$ can be obtained [38]. Atomic-resolution high-angle annular dark filed (HAADF) scanning transmission electron microscopy (STEM) imaging (Figure 14c,d) shows the distribution of S and Se atoms in the monolayer alloys. Raman and photoluminescence spectra (Figure 14e) also indicate the shift of characteristic peaks induced by composition change.

The other process [36,39] uses mixed S and Se fine powders as the chalcogen source and MoO_3 as the metal source (Figure 14f). By changing the ratio of the S and Se powders in the source, the fraction in the alloy can be well controlled with x ranging from 0–0.75. FETs based on the synthesized $MoS_{2(1-x)}Se_{2x}$ alloy exhibit a high on/off current ratio of about 10^6 and a mobility up to 15.3 $cm^2\ V^{-1}\ s^{-1}$ [39].

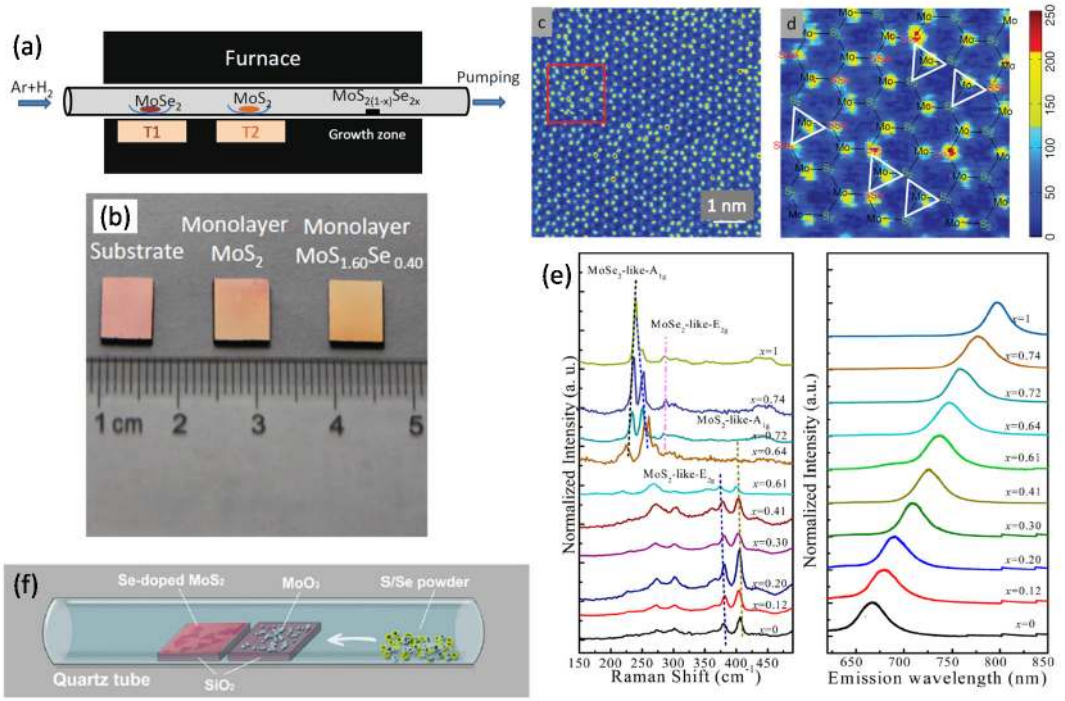

Figure 14. Two CVD processes for the synthesis of $MoS_{2(1-x)}Se_{2x}$ alloys. (**a**) Schematic of CVD with separate $MoSe_2$ and MoS_2 precursors; (**b**) photograph of bare SiO_2/Si substrate and centimeter-scale MoS_2 and $MoS_{1.60}Se_{0.4}$ monolayer films on substrates; (**c**,**d**) high-angle annular dark filed (HAADF)-STEM image of $MoS_{1.60}Se_{0.4}$ monolayer film in false color; (**e**) Raman (left) and photo-luminescence (right) spectra of $MoS_{2(1-x)}Se_{2x}$ alloys with x ranging from 0 to 1; (**f**) schematic of CVD with separate mixtures of S and Se powders as precursors. (**a**–**d**) Adapted with permission from [37]. Copyright 2014, WILEY-VCH Verlag GmbH. (**e**) Adapted with permission from [38]. Copyright 2015, American Chemical Society. (**f**) Adapted with permission from [39]. Copyright 2014, American Chemical Society.

3.1.2. $Mo_{1-x}W_xS_2$ Alloys

Song *et al.* [40] recently reported a synthesis method of $Mo_{1-x}W_xS_2$ alloys by sulfurization of super-cycle ALD $Mo_{1-x}W_xO_y$ alloy thin films. First, 10 cycles of WO_3 were pre-deposited through ALD to address the nucleation delay issues of ALD-grown WO_3. Then, one super-cycle ALD process (Figure 15a) comprising n cycles of ALD MoO_x and m cycles of ALD-grown WO_3 is performed to grow $Mo_{1-x}W_xO_y$ alloy thin films, followed by sulfurization to obtain 2D $Mo_{1-x}W_xS_2$ alloys. By adjusting the n/m ratio, the fraction of W in the final alloys, x, can be well controlled. Typically, one super-cycle gives rise to uniform monolayer $Mo_{1-x}W_xS_2$ alloys with a thickness of ~1 nm (Figure 15b), and two and three super-cycles produce bi- or tri-layer 2D alloys, respectively. In other words, the alloy composition and layer number can be well controlled during the ALD-based synthesis process. Consequently, the band gaps of the alloys can also be precisely controlled. Furthermore, vertically-composition-controlled (VCC) $Mo_{1-x}W_xS_2$ multilayer alloys (Figure 15c) have also been synthesized by using a sequential super-cycle ALD process, which consists of five continuous super-cycles with different n/m ratios for each super-cycle. The VCC $Mo_{1-x}W_xS_2$ multilayer alloys exhibit a broadband light absorption property

and are very promising for efficient photodetector applications. In particular, the ALD-based super-cycle process is anticipated to apply also to other 2D TMDC alloys than $Mo_{1-x}W_xS_2$.

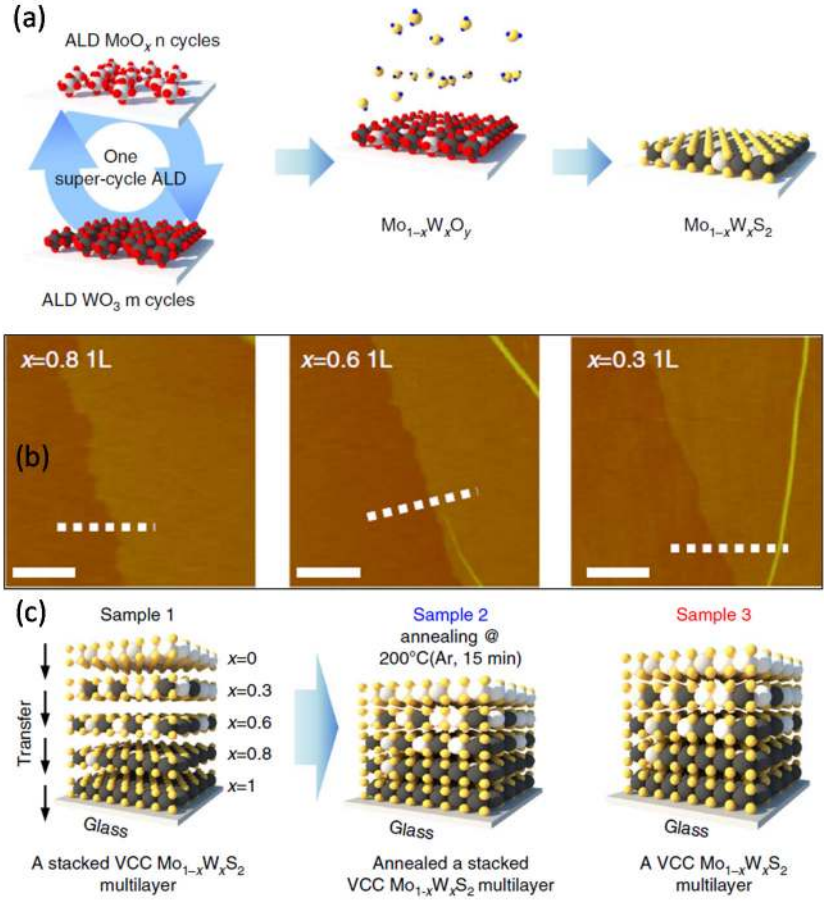

Figure 15. ALD-based synthesis of $Mo_{1-x}W_xO_y$ alloy. (**a**) Schematic of the synthesis procedure with the super-cycle of the ALD processes; (**b**) AFM images of the alloys with different *x* (scale bars: 500 nm); (**c**) schematics of three vertically-composition-controlled (VCC) $Mo_{1-x}W_xO_y$ multilayers. Adapted with permission from [40]. Copyright 2015, Nature Publishing Group.

Meanwhile, Zhang *et al.* [36] also developed a CVD process to synthesize 2D $Mo_{1-x}W_xS_2$ alloys. They used a mixture of WO_3 and MoO_3 powders as the metal precursor and sulfur powder as the chalcogen precursor. The band gaps of the grown $Mo_{1-x}W_xS_2$ alloys are tuned through adjusting the Mo/W ratio in the precursors.

3.2. 2D Heterostructures

One of the greatest interests in recent research is to reassemble isolated 2D materials into heterostructures in a layer-by-layer form and in a controllable sequence, just like building with atomic-scale Lego blocks [13]. The assembled 2D heterostructures, sometimes called van der Waals heterostructures, often reveal unusual properties and new phenomena and are anticipated to play an important role in future electronics and optoelectronics [8]. The van der Waals heterostructures can be readily fabricated by stacking different 2D materials through mechanical transfer techniques. However, the techniques suffer from

uncontrolled stacking orientation, contaminated interfaces and significant challenges for massive production. As a matter of fact, researchers have also begun to develop scalable synthesis techniques for various 2D heterostructures, including semiconductor/conductor (TMDC/graphene), semiconductor/insulator (TMDC/BN) and semiconductor/semiconductor (TMDC/ TMDC) 2D structures. Actually some techniques introduced above are already able to synthesize 2D TMDC heterostructures, such as the MBE-grown $HfSe_2$/HPOG and $HfSe_2$/MoS_2 heterostructures (Section 2.4, Figure 13, [35]) and the ALD-based CVD-grown VCC $Mo_{1-x}W_xO_y$ multilayers (Section 3.1.2, Figure 15c, [40]). Below, we briefly introduce other techniques for the 2D TMDC heterostructures.

3.2.1. TMDC/Graphene Heterostructures

In 2011, Shi *et al.* [41] introduced a method to synthesize MoS_2/graphene heterostructures (Figure 16). First, monolayer graphene is synthesized on copper foil through a CVD process. Then, the graphene/copper substrate is placed in a quartz tube chamber, and the $(NH_4)_2MoS_4$/DMF dispersion is carried by Ar gas to deposit onto the graphene surface as the MoS_2 precursor. Finally, after DMF evaporates, the samples are annealed at 400 °C in Ar/H_2 atmosphere to decompose $(NH_4)_2MoS_4$ and obtain the MoS_2/graphene heterostructures.

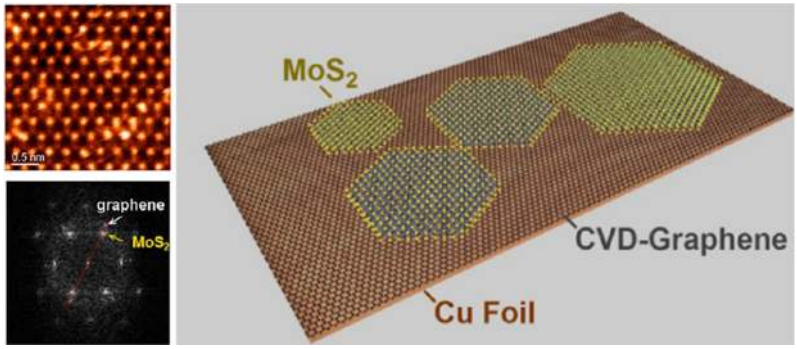

Figure 16. TEM analysis (left) and schematic (right) of the MoS_2/graphene heterostructure. Reprinted with permission from [41]. Copyright 2012, American Chemical Society.

Miwa *et al.* [42] recently demonstrated direct van der Waals epitaxy of MoS_2/graphene heterostructures on silicon carbide (SiC) substrates. The graphene/SiC substrate is first fabricated through direct current annealing of SiC under a mild flux of silicon atoms. Then, MoS_2 is synthesized in a similar way to the cycle-based MoS_2 growth on gold (Figure 9, [32]). The buffer layers coexisting with graphene on the substrates facilitate the MoS_2 growth. Due to the weak van der Waals interaction between graphene and MoS_2, the electronic structure of free-standing monolayer MoS_2 is retained in the heterostructure as confirmed by angle-resolved photoemission spectroscopy measurements.

3.2.2. TMDC/BN Heterostructures

Wang *et al.* [43] recently reported an all-CVD process to fabricate high-quality monolayer MoS_2/BN heterostructures with centimeter-scale MoS_2 domains. As illustrated in Figure 17a, first, few-layer hexagonal boron nitride (h-BN) is grown on copper substrates by CVD with an ammonia borane precursor. To suppress decomposition during MoS_2 growth, few-layer h-BN films (2–4 layers) are

preferred to monolayer h-BN. Then, the h-BN film is transferred to SiO_2/Si wafer. Finally, MoS_2 is grown on top of h-BN films by CVD with MoO_3 and S powders as the precursors. Possibly because of the relatively strong interaction between MoS_2 and h-BN, the directly-grown MoS_2 on h-BN films exhibits smaller lattice strain, a lower doping level, cleaner and sharper interfaces and better interlayer contact, as compared with those directly grown on SiO_2/Si wafer (Figure 17b).

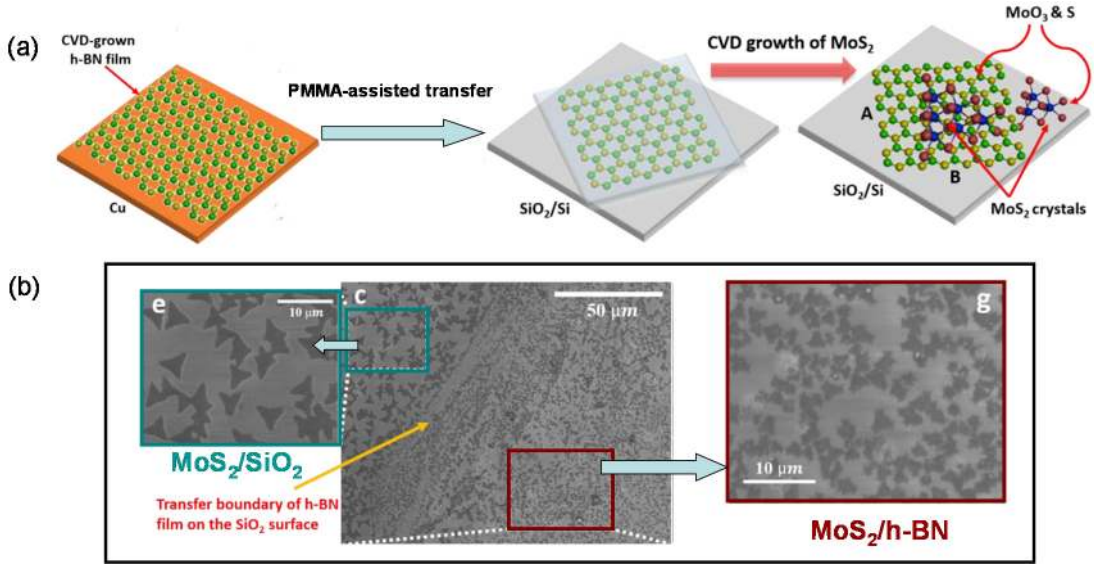

Figure 17. (**a**) Schematic of one fabrication process of the MoS_2/hexagonal boron nitride (h-BN) heterostructure; (**b**) SEM images of MoS_2 grown on the edge of the transferred h-BN indicating the difference in morphology of MoS_2 grown on SiO_2 and h-BN. Adapted with permission from [43]. Copyright 2015, American Chemical Society.

3.2.3. TMDC/TMDC Heterostructures

Gong *et al.* [44] report a scalable single-step VPD process to synthesize highly-crystalline MoS_2/WS_2 heterostructures with both a vertically-stacked bilayer structure (Figure 18a–d) and an in-plane inter-connected structure (Figure 18e–h). As shown in Figure 18i, in front of the SiO_2/Si substrate, MoO_3 powder is placed as the metal precursor for the growth of MoS_2. On top of the substrate, a mixture of tungsten (W) and tellurium (Te) powders is placed for the growth of WS_2. Here, the Te powder serves as the catalyst to accelerate the melting of W powder. Argon is used as the carrier gas to transport the S vapor from the upstream. Since MoS_2 and WS_2 have different nucleation and growth rates, this leads to sequential growth of the materials and, thereby, forms heterostructures, rather than growing the $Mo_{1-x}W_xS_2$ alloy. The structure of the final product is determined by the reaction temperature. High-temperature (~850 °C) growth produces mostly vertically-stacked bilayers, where WS_2 is grown epitaxially on top of monolayer MoS_2, while low-temperature (~650 °C) growth generates mostly in-plane lateral heterojunctions where MoS_2 and WS_2 locate within a single hexagonal monolayer lattice with seamless and atomically-sharp interfaces. Because of the clean interface, the vertically-stacked bilayers can retain the performance of individual monolayers and meanwhile generate an additional direct band gap via interlayer coupling. Remarkably, back-gate FETs based on the vertical MoS_2/WS_2 stacks exhibit an on/off current ratio over 10^6 at a high mobility ranging from 15–34 $cm^2\ V^{-1}\ s^{-1}$. The

in-plane MoS_2/WS_2 heterojunctions greatly enhance the localized photoluminescence and can serve as intrinsic monolayer p–n junctions with no need for external electrical tuning.

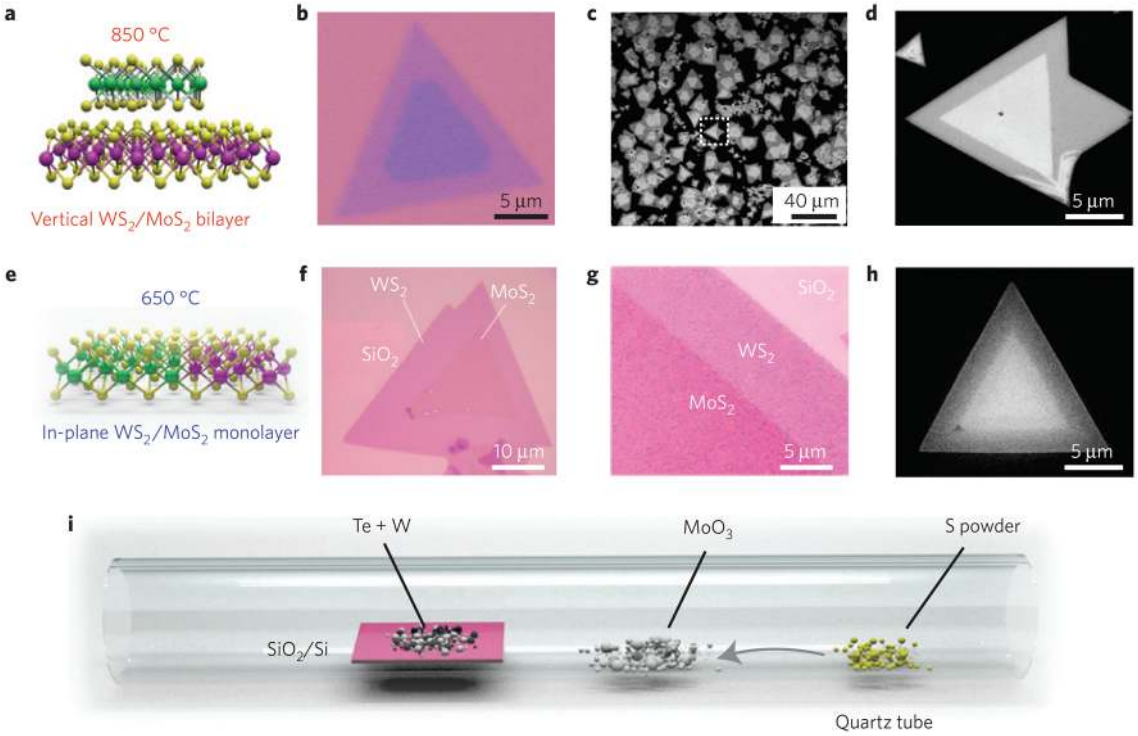

Figure 18. CVD growth of vertically-stacked and in-plane WS_2/MoS_2 heterostructures. (**a**–**d**) Schematic, optical and SEM images of vertically-stacked heterostructures; (**e**–**h**) schematic, optical and SEM images of in-plane heterostructures; (**i**) schematic of the synthesis process. Reprinted with permission from [44]. Copyright 2014, Nature Publishing Group.

Huang *et al.* [45] also demonstrate a technique based on direct physical vapor deposition (PVD) to synthesize high-quality monolayer $MoSe_2/WSe_2$ lateral heterojunctions. The precursor, a mixture of WSe_2 and $MoSe_2$ powders, is vaporized at high temperature (~950 °C) and carried by hydrogen gas to the downstream SiO_2/Si substrate and, finally, crystallizes on the substrate to form the lateral heterojunctions (Figure 19). The growth mechanism may rely on the different evaporation rates of the two materials. In the beginning, $MoSe_2$ evaporates quickly, and pure monolayer $MoSe_2$ crystals predominate in the substrate. After some time, the $MoSe_2$ source has considerable surface depletion of Se, so that its evaporation slows down. Meanwhile, the evaporation of WSe_2 increases, leading to predominant growth of WSe_2 on the substrate. The different evaporation rates prevent the formation of $Mo_{1-x}W_xSe_2$ alloy. Due to their great similarity, WSe_2 can epitaxially grow on the $MoSe_2$ crystal edges to form the lateral heterojunctions. The monolayer heterojunctions retain an undistorted honeycomb lattice and exhibit enhanced photoluminescence.

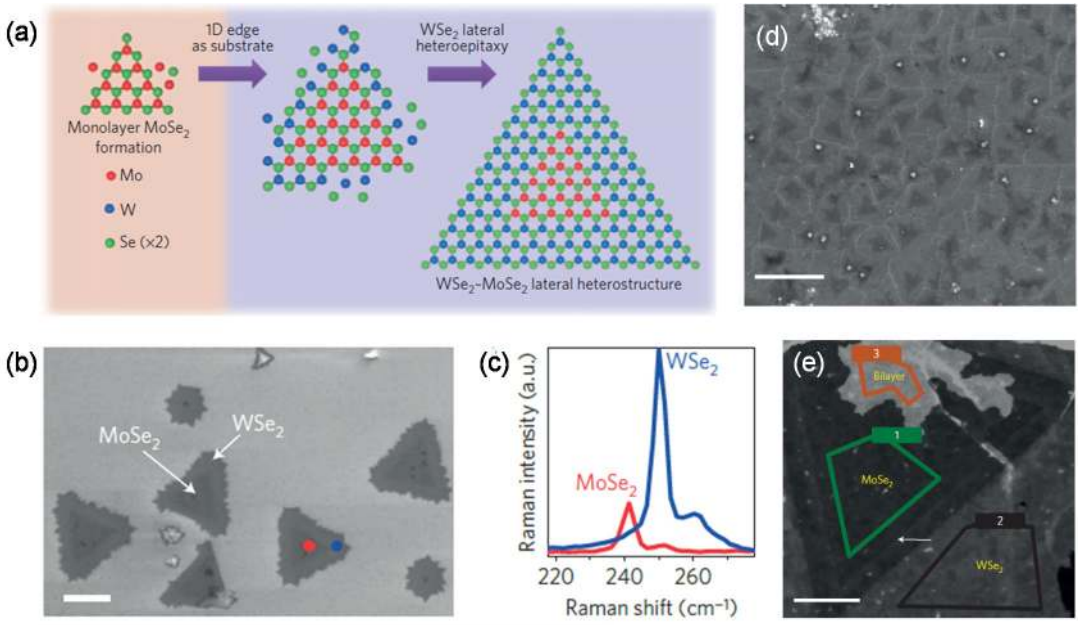

Figure 19. PVD growth of in-plane $WSe_2/MoSe_2$ heterostructures. (**a**) Schematic of the synthesis mechanism; (**b**) SEM image of the grown in-plane heterostructures (scale bar: 10 μm); (**c**) Raman spectra acquired at different regions in the heterostructure as indicated in (**b**); (**d**) SEM image of a film transfer film to a SiO_2 substrate (scale bar: 5 μm); (**e**) HAADF-STEM image of a triangle (scale bar: 100 nm). Adapted with permission from [45]. Copyright 2014, Nature Publishing Group.

3.3. Wafer-Scale Device Engineering

Despite the great progress in scalable and controllable synthesis of 2D TMDCs, with respect to device performance, however, most studies just explore a few devices in selected areas [23]. Large-scale device engineering still remains challenging. Fortunately, the increasing maturity of the VDP techniques has enabled some attempts in advanced engineering of 2D TMDC-based devices at the wafer scale.

3.3.1. Direct Growth of TMDC at Controlled Locations

Han *et al.* [46] use patterned Mo precursors to grow MoS_2 flakes at predefined locations at the resolution of micrometer scale. As illustrated in Figure 20a, first, lithography is employed to define the area for MoS_2 growth with photoresist. Then, the precursor, MoO_3 or ammonium heptamolybdate (AHM), is deposited into the area through thermal evaporation or spin coating. After the photoresist is stripped, a special aggregation step and chemical treatment by promoters, such as PTAS and PTCDA, are conducted to form spherical beads of precursors and to improve the uniformity of the following MoS_2 growth. Finally, the precursor is sulfurized by vaporized S in a nitrogen atmosphere. The grown MoS_2 shows high crystallinity and excellent optical properties. Back-gate FETs exhibit high carrier mobility between 8.2 and 14.4 $cm^2\ V^{-1}\ s^{-1}$ with the on/off current ratio around 10^6. In particular, the precise control over the location of discrete MoS_2 flakes (Figure 20b) facilitates direct integration and massive device production (Figure 20c) through conventional lithography without the need for an etching step.

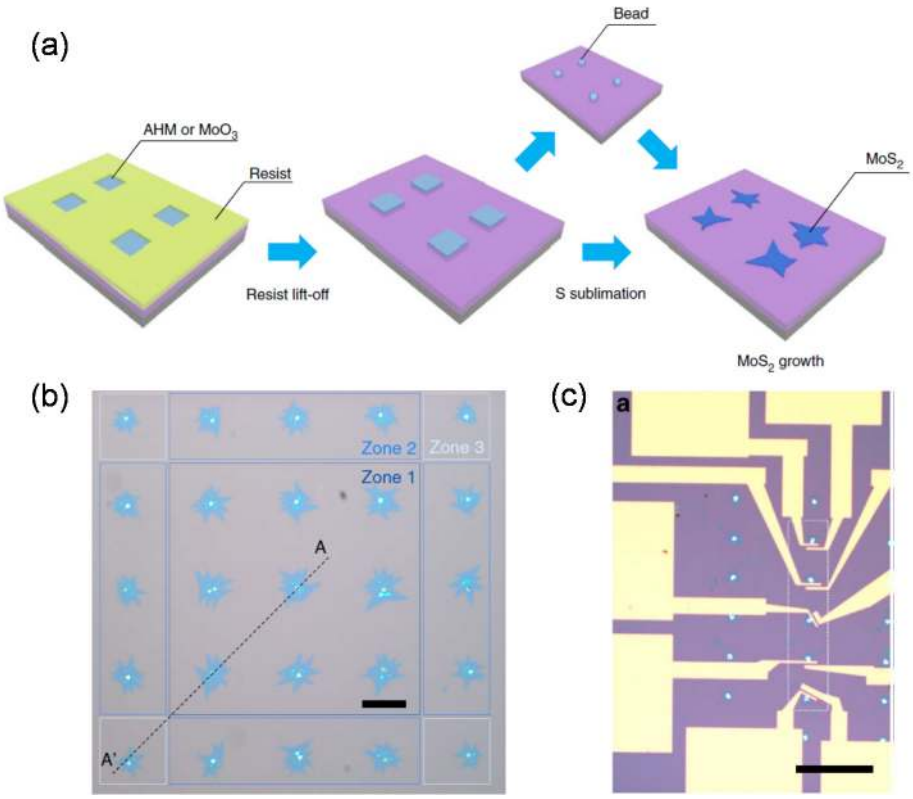

Figure 20. Selective CVD growth of MoS_2 using patterned precursors. (**a**) Schematic of growth process; (**b**) an array of CVD-grown MoS_2 monolayer flakes (scale bar: 50 μm); (**c**) batch production of FETs based on MoS_2 array (scale bar: 100 μm). Adapted with permission from [46]. Copyright 2015, Nature Publishing Group.

3.3.2. Multi-Level Stacking of TMDC Devices

As introduced in Section 2.1.2, the all-gas precursor MOCVD process developed by Kang *et al.* [23] enables wafer-scale growth of high-quality monolayer MoS_2 film directly on SiO_2 substrates. This opens opportunities to fabricate multi-level stacked monolayer MoS_2 films (Figure 21a,b) and devices (Figure 21c–e). As illustrated in Figure 21c, the multi-level stacked structure can be fabricated in the following sequence: growing the first MoS_2 monolayer on the SiO_2/Si wafer, fabricating first-level FETs, depositing SiO_2 (~500 nm thick) by plasma-enhanced CVD, growing the second MoS_2 monolayer, fabricating second-level FETs, and so on. Figure 21d indicates an array of two vertical levels of MoS_2 FETs, both of which can be well modulated through the global back gate (Figure 21e). Note that as compared to the first-level device, which has an on-state sheet conductance of about 2.5 μS and a mobility of about 11.5 $cm^2\ V^{-1}\ s^{-1}$, the second-level device only exhibits a little performance degradation with an on-state sheet conductance of about 1.5 μS and a mobility of about 8.8 $cm^2\ V^{-1}\ s^{-1}$. This suggests that the technique can be employed for 3D device architecture based on TMDCs, which may provide a new solution to the most attractive, yet challenging field in recent electronics research, monolithic 3D integration [47].

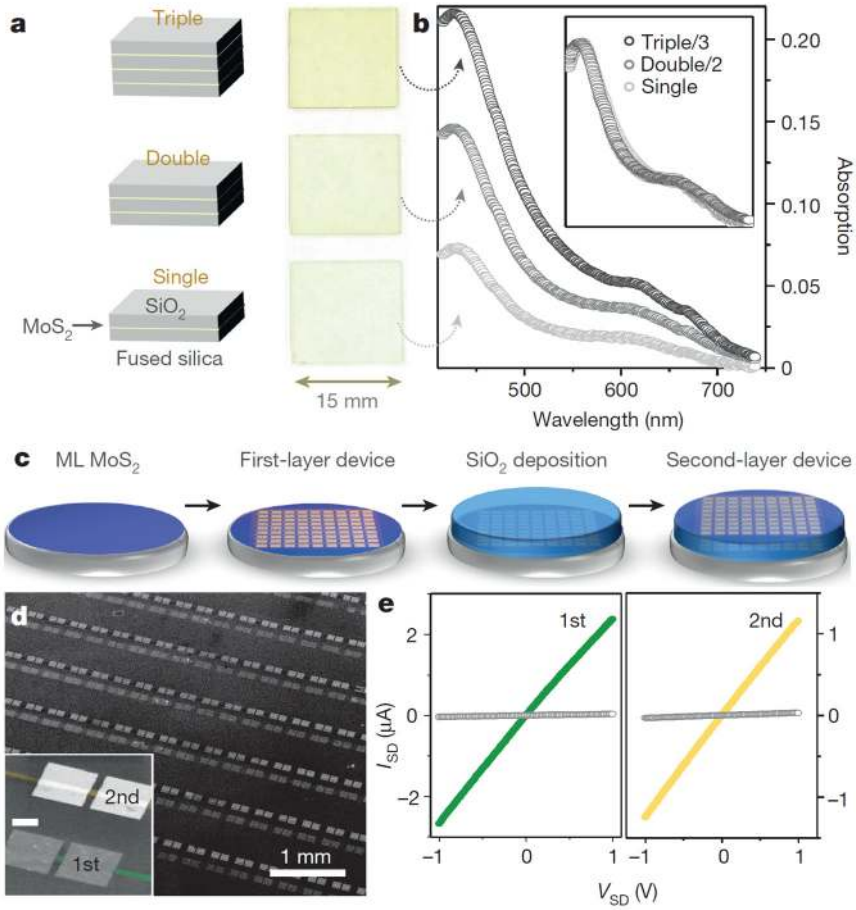

Figure 21. Multi-level stacking of MoS_2/SiO_2 structures. (**a**) Schematics (left) and optical images of 1–3 level stacking; (**b**) optical absorption of three levels of stacking; (**c**) schematic of the fabrication of multi-level stacking of MoS_2-based devices; (**d**) SEM image of MoS_2 FET arrays on the first (bottom) and second (top) layers (inset: close-up view; scale bar: 50 um); (**e**) current-voltage curves for a pair of devices on the first (left) and second (right) layers. The first-layer device is biased by the back gate of 50 V (green) and −50 V (grey), while the second-layer devices are at 100 V (yellow) and −100 V (grey). Reprinted with permission from [23]. Copyright 2015, Nature Publishing Group.

4. Discussions and Outlook

As introduced above, versatile scalable synthesis techniques for 2D semiconducting TMDCs have been developed in the literature, many of which have already led to commendable device performance (mobility >10 cm^2 V^{-1} s^{-1} with on/off current ratio >10^6) approaching the state-of-the-art performance acquired by the high-quality mechanically-exfoliated MoS_2 flakes (Figure 22) [14,48]. More importantly, the techniques tend to be mature and have been effective for advanced engineering of 2D TMDC alloys, various 2D heterostructures, wafer-scale device fabrication and vertical stacking of 2D transistors. These suggest that 2D TMDC-based devices have great potential for up-scaled manufacturing of high-end nanoelectronics in the near future. In particular, the unique properties of 2D TMDCs will enable innovative applications in emerging electronics and provide ideal solutions to the challenging research fields nowadays, such as monolithic 3D integration.

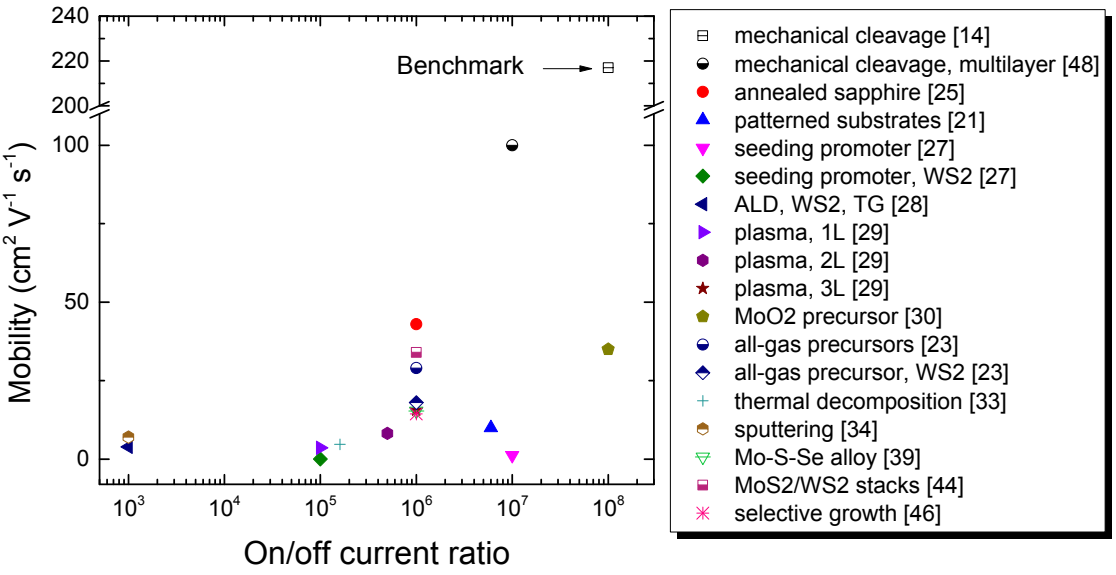

Figure 22. Plots of mobility against the on/off current ratio for FETs based on TMDCs synthesized by some techniques introduced above and the state-of-the-art performance acquired by the mechanically-exfoliated MoS_2 [14]. Unless specified in the legend, all devices are back-gate FETs with MoS_2 channels. "TG" in the legend means "top gate".

However, referring to Figure 22, one may see that despite the versatile scalable synthesis techniques demonstrated, none of them outperform the mechanically-exfoliated MoS_2 flakes with respect to device mobility and on/off current ratio. There is still great space for further advances in the fields of the scalable synthesis of 2D semiconducting materials. We foresee that the issues concerning material crystallinity, interface contamination, spatial uniformity, controlled layer number and integration with device engineering will remain critical for a relatively long time. Here, we envision several tendencies in the upcoming research: (1) The device performance boost may have to rely on effective integration among different synthetic techniques. Seemingly, one single technique can hardly make a breakthrough in addressing all of the issues. In contrast, a comprehensive technology integrating substrate treatment, seeding promoters, gas-phase precursors and growth cycle control will likely lead to higher crystallinity, better layer number controllability, higher uniformity at the wafer scale and, hence, substantially improved device performance. (2) Material synthesis will be integrated with device fabrication to enable advanced engineering at multiple levels. A good example has been demonstrated in [46], where the precursors are patterned before material growth to facilitate the following device fabrication. (3) More efforts will be transferred from synthesizing high-quality simple materials to fabricating complex materials and building advanced structures, such as the 2D alloys and van der Waals heterostructures, aiming to offer more flexibility to construct advanced device architectures. (4) The established synthesis techniques may extend to newly-discovered 2D semiconducting materials within or outside the family of TMDCs to seek a breakthrough through a new perspective.

It is worth mentioning that the final device performance is not merely determined by the material synthesis. The device engineering also plays an important role in the performance boost. For example, as shown in Figure 22, most TMDC-based FETs are of the back-gate device structure with exposed channels, which, although simplifying device fabrication, usually does not give rise to high device

performance. This might be an important reason that they cannot outperform the state-of-the-art FETs based on mechanically-exfoliated MoS_2 where a high-k gate oxide is deposited on top of the channel to generate dielectric screening and to improve the mobility [14]. In most cases, the synthesized TMDCs have to be transferred from the growth substrates to the SiO_2/Si substrates for device fabrication. Versatile techniques (Figure 23) have been developed for wafer-scale transfer of 2D materials [49–51]. They provide more flexibility for material synthesis and device fabrication. However, a common issue is that the residual contamination induced by the transfer processing may also degrade the device performance [52]. Therefore, in addition to improving material synthesis techniques, properly addressing the issues arising from device engineering is also crucial for 2D material-based electronic devices.

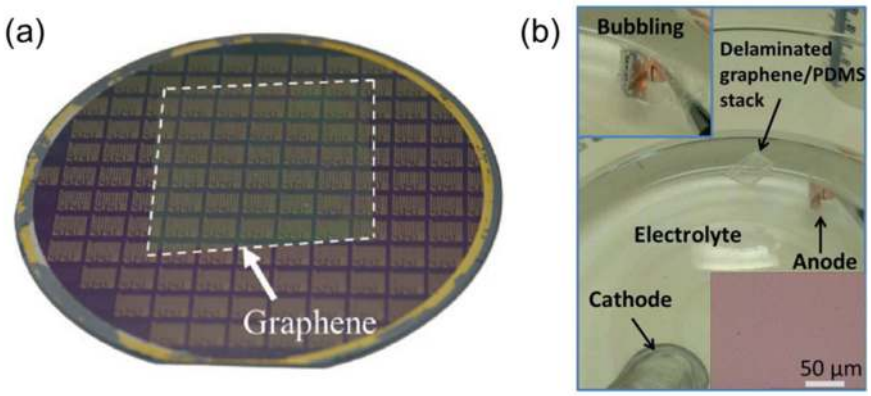

Figure 23. Wafer-scale transfer techniques for 2D materials. (**a**) Transferred graphene onto a 4-inch silicon wafer with poly(bisphenol A) carbonate (PC) as the carrier; (**b**) delamination of the graphene/polydimethylsiloxane (PDMS) stack using electrolysis (inset: optical microscope image of graphene transferred onto an SiO_2 layer). (**a**) Reprinted with permission from [49]. Copyright, 2014 IEEE. (**b**) Reprinted with permission from [50]. Copyright 2014, IEEE.

Finally, there are considerable efforts on computational simulations in order to understand the growth dynamics of 2D materials [53–59]. These theoretical studies provide mechanisms and explanations for experimental observations and useful suggestions for material quality improvement [56,58]. They also indicate optimal conditions for nucleation [57] and edge reconstruction [53] during growth, as well as predict the structure and stability of 2D materials grown on different substrates [54–57,59]. Such guidance is also valuable for experimentalists to improve their growth processes or to explore innovative techniques.

In summary, the review provides a systematic and comprehensive introduction of scalable synthesis techniques of 2D semiconducting materials for high-end applications in future nanoelectronics, most of which have shown promise in scaling up device fabrication. We hope the review is beneficial to the readers, either in establishing existing techniques for further research on 2D materials or in stimulating innovative ideas to enhance and extend the research on scalable synthesis techniques.

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Author Contributions

Jiantong Li and Mikael Östling discussed the topic, surveyed the literature and wrote the manuscript.

Conflicts of Interest

The authors declare no conflict of interest.

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