Scalable SiPh-InP Hybrid Switch Based on Low-Loss Building Blocks for Lossless Operation

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Abstract— We design and experimentally demonstrate scalable 2 × 2, 4 × 4 and 8 × 8 silicon photonic (SiPh) thermo-optic switch exhibiting low loss, low crosstalk, low power penalty, and BER below 10^{-10} for payload data transmission. Less than 3.13 dB insertion loss (IL) and approximately 20.5 dB crosstalk is measured in the 8 × 8 SiPh banyan switch with thermal phase shifters. We also report on a semiconductor optical amplifier (SOA) in an indium phosphide (InP) technology platform with 25 dB gain and 7 dB noise figure enabling to transmit optical signals with large OSNR. Combining SiPh and InP technologies, we propose a lossless hybrid switch matrix with distributed SOA-based gain capable of transmitting data with near zero loss and low crosstalk over a large switching matrix. In hybrid SiPh/InP switches, the SOA gain compensates for the SiPh switch loss at the cost of amplified spontaneous emission (ASE) noise but mitigated by bandpass optical filters. Lower IL from the SiPh switch requires less gain from the SOAs leading to less OSNR degradation. Experimentally validated building blocks confirmed scalability up to 64 × 64 in SiPh-InP hybrid platform.

Index Terms— Hybrid switches, optical switches, semiconductor optical amplifiers, silicon photonics.

I. INTRODUCTION

THE exponential growing network traffic is forcing data-centers to increase their communications bandwidth with high switching speed and low energy consumption. Future communication systems need higher capacity interconnects technology with high bandwidth, high switching speed, and low power consumption. Optical switches have all those potentials enabling rapidly increasing communication systems. Recently, researchers are focusing on high-radix silicon photonic switches, compatible with complementary metal-oxide-semiconductor (CMOS) for higher integration density and lower manufacturing cost. A major constraint of high radix switch in SiPh technology is the optical losses from the multiple stages. To reduce the insertion loss in large radix optical switches, lossless operation in large port count switches are also possible in other technologies such as III-V [1].

To combine the respective advantages of Si and InP materials, hybrid SiPh/InP integrated switches have been recently introduced [2], [3]. An InP-SOA based active gain block can amplify the optical signal to compensate for the on-chip loss in large SiPh switches. Furthermore, photonic wire bonded or flip-chip bonded semiconductor optical amplifier (SOA) can be an impactful candidate in opto-electronic industry for the implementation of SiPh-InP switches [4], [2].

In this letter, we demonstrate the design and characterization of a low loss SiPh switch and its application in SiPh/InP hybrid optical switch. This letter comprises four sections. In Section II, a multi-mode interferometer (MMI) based low-loss thermo-optic 2 × 2, 4 × 4 and 8 × 8 banyan switches have been demonstrated. In Section III, the novel design of 16 × 16, 32 × 32 and 64 × 64 hybrid banyan switch is proposed with the concept of distributed InP-SOA gain block. Its characteristics are discussed based on the building blocks presented in section II. Finally, the summary and result of these hybrid switches are reported in Section IV.

II. DESIGN AND CHARACTERIZATION OF SIPH SWITCH

The Mach-Zehnder Interferometer (MZI) is suitable for space switching in WDM systems compared to other techniques such as ring resonator-based switches which are challenged by thermal crosstalk [5]. A typical 2 × 2 MZI switch consists of two MMI as the 3-dB splitter/coupler and a dual-waveguide balanced arm to connect them shown in fig. 1(a). One of the arms has the phase shifter able to change the phase difference between two arms from 0 to π by thermally changing the Si refractive index. In our design, the slab waveguides used to connect each component in this switch have a width of 500 nm tapered to 1.4 μm over a 20 μm length before connecting with the MMI core to reduce the insertion loss between the MMI core and connecting waveguides. A 6 μm wide and 131 μm long 2 × 2 ports MMI (fig. 1(b)) is optimized according to its self-imaging property at 1550 nm. A 200 μm long and 5 μm wide Titanium Tungsten (TiW) heater is designed as a phase shifter placed between the two MMIs and 2 μm above one of the MZI balanced paths (fig. 1(c)).

The SiPh switch is designed for fabrication on a Silicon-on-Insulator (SOI) wafer through Applied Nanotools Inc. (ANT) [6]. The substrate is a 220 nm silicon device layer with a 2 μm buried oxide layer. The device is fabricated using an Electron Beam Lithography (EBL) and a Reactive Ion Etching (RIE) process. An anisotropic inductively-coupled-plasma reactive ion etching (ICP-RIE) process is conducted on the substrate to transfer the pattern into the underlying silicon layer. The TiW alloy and the Aluminum thin film are used for the metal heaters and the routing, respectively. In the last stage, a silicon
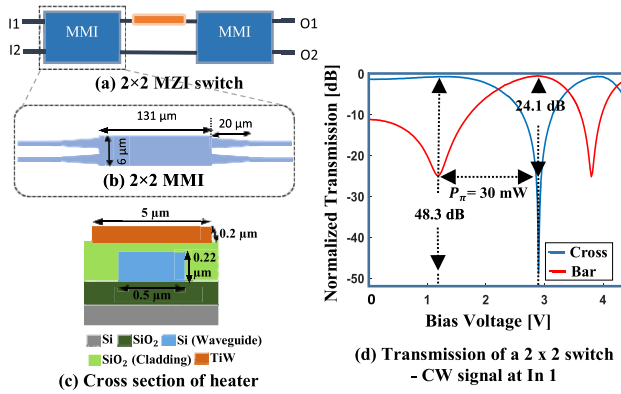
Fig. 1. (a) 2 × 2 MZI cell; (b) 2 × 2 MMI building block; (c) Cross section of heater; (d) Experimental optical transmission of the 2 × 2 switch at 1550 nm.

dioxide layer is deposited onto the device using a Chemical Vapor Deposition (CVD) process.

For characterization, a C-band tunable laser is used to perform the continuous wave (CW) measurements. A polarization controller (PC) is connected to the output of the laser source to maintain the on-chip polarization of the optical signal to a quasi-TE optical mode. The optical signal is coupled into the chip through a grating coupler with another grating used at the output of the chip. The output is measured by an optical power meter. The CW measurements are normalized to the grating couplers' losses.

The MZI with the thermal phase shifter works as a 2 × 2 thermo-optic switch and exhibits 0.6 dB insertion loss with crosstalk less than -24 dB over the wavelength range from 1500 nm to 1600 nm. The 4 × 4 and 8 × 8 switch are designed using a banyan topology for a more relax optical power budget at the cost of a blocking behavior which can be used in interconnect switches for WDM-based networks where the controller accounts for the blocking scenarios. The 4 × 4 banyan switch shown in Fig. 2(a) is comprised of four 2 × 2 MZI building blocks. At 1550 nm, the IL measured for the shortest switching path (I1-O1 & I4-O4) of the 4 × 4 switch is less than 1.4 dB and approximately 2.1 dB for the longest path (I1-O4 & I4-O1). The worst crosstalk recorded is -21.5 dB. For the 8 × 8 banyan switch, light passes through three cascaded MZIs as shown in Fig. 2(b). The IL of the shortest switching path (I1-O1 & I8-O8) is measured to be less than 3.1 dB with no waveguide crossing employed. For the longest path (I1-O8 & I8-O1) which includes four waveguide crossings, the IL is approximately 5.0 dB. Each crossing has an insertion loss of approximately 0.3 dB. The maximum crosstalk measured is at most -20.5 dB over the wavelength range from 1515 nm to 1585 nm. The 3 dB bandwidth of this switch is 25 nm. The performance of this switch is improved relative to than similar works [7], [8] enabling further scalability for greater port count.

Payload transmission is then experimentally performed to demonstrate the switching performance using the setup in fig. 3.

The corresponding bit error rate (BER) power penalties are shown in Fig. 4 for input-1 to all of the outputs at the BER of 10^{-10}. The penalty varies with routing paths with a worst case (best case) power penalties are 0.5 dB (0.3 dB), 0.7 dB (0.4 dB) and 4.4 dB (0.5 dB), respectively, for 2 × 2, 4 × 4 and 8 × 8. In the 8 × 8 switch, the longest paths (I1-O7 and I1-O8) have more crossings leading to higher loss, as well as possible
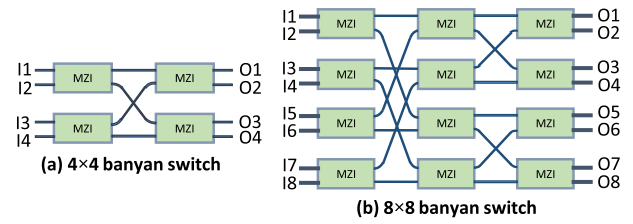

Fig. 2. Schematic structures of banyan blocking switching topology; (a) 4 × 4 thermal switch; (b) 8 × 8 thermal switch.
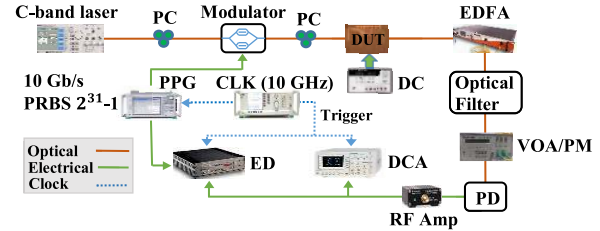

Fig. 3. Experimental setup of the switch (DUT) for 10 Gb/s data transmission. PC: Polarization Controller; EDFA: Erbium doped fiber amplifier; DC: Voltage Supply; PPG: Programmable Pattern Generator; CLK: Clock synthesizer; ED: Error Detector; DCA: Digital Communication Analyzer; VOA/PM: Variable Optical Amplifier/Optical Power Meter; RF Amp: RF Amplifier.
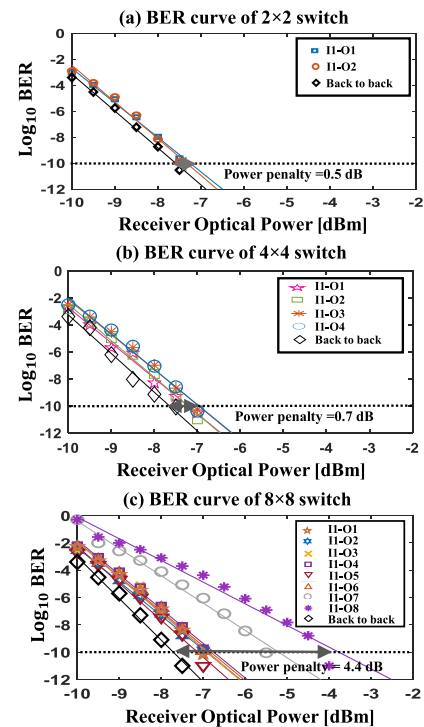

Fig. 4. Logarithmic BER as a function of received optical power for input I1 to all outputs and back-to-back connection; (a) BER curve for 2 × 2 banyan switch; (b) BER curve for 4 × 4 banyan switch; (c) BER curve for 8 × 8 banyan switch.

additional coupling loss from the fiber array due to the larger distance between input port I1 and output ports O7 and O8.

The corresponding output eye diagrams for input I1 to all outputs are shown in Fig. 5 for 10 Gb/s payload signal transmission. Clear open eye diagrams are observed for all the routing channels with a signal to noise ratio (SNR) of at least 7.5 at a BER of 10^{-10}. The grating coupler and corresponding fiber array used for the 8 × 8 switch is less lossy (-8.5 dB) and more stable than the ones used for the 4 × 4 and 2 × 2 switches
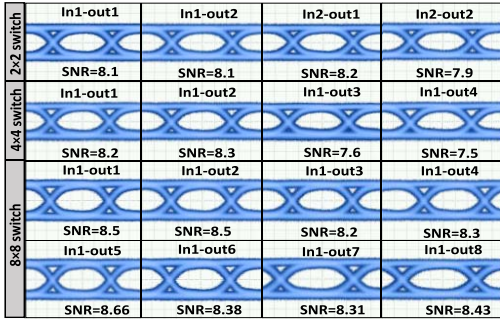
Fig. 5. Eye diagram of the 2×2, 4×4 and 8×8 switches for all the corresponding outputs (100 mV/div) with the data at input port I1.

(-11 dB) due to different polished angles. Consequently, testing the 8×8 switch requires less gain from the EDFA leading to better eye diagrams and SNR in the payload transmission.

III. PROPOSED HYBRID SWITCH DESIGN

We use the SiPh switch presented in section II in the design of lossless scalable SiPh/InP hybrid switches. We have reported on employing an InP gain block, coupled to the SiPh switch, providing over 25 dB of optical gain in SiPh/InP hybrid switch [7]. The SOA optical gain comes with inevitable amplified spontaneous emission (ASE) noise degrading the optical signal-to-noise ratio (OSNR) at the output of the hybrid switch. The ASE noise level and OSNR degradation are the main challenges in cascading the hybrid switches to realize a higher radix switch. Also, large gain from SOAs leads to non-linearity effects that degraded the payload integrity and increase the power penalty [9]. Furthermore, the sensitivity of the SOAs is limited (approximately to -20 dBm) [7]. As the switch radix increases, more than one gain blocks are needed to boost the signal power repeatedly, whereas, each gain block comes with inevitable coupling loss and fabrication cost. The low-loss SiPh switch presented in this study improves the optical power budget, and thereby reduces the required gain from the SOAs in gain block.

In Table I, the SiPh on-chip loss estimation for the longest path of the 4×4, 8×8, 16×16, 32×32 and 64×64 banyan switches are assessed. The measurement for the 16×16, 32×32 and 64×64 switches are done based on the experimental results of the building blocks and validated with simulated results using Lumerical Interconnect. The experimentally measured losses for the building blocks are 0.6 dB, 0.3 dB and 3.8 dB/cm for 2×2 switch cell (MZI), waveguide crossing, and waveguide, respectively. It is observed that the total on chip loss estimated from the building blocks for 4×4 and 8×8 switches are approximately same as the experimental measurement reported in section II, which validates the total on-chip losses estimated for 16×16, 32×32 and 64×64 switches shown in Table I.

Fig. 6 presents the design for lossless scalable 16×16 and 32×32 SiPh/InP hybrid switches with distributed gain. The SiPh and InP chips are assumed to be coupled using photonic wire-bonding technique [4], [10]. The SOAs are capable of compensating for the coupling losses (22 dB/path) along with the on-chip losses for lossless operation. Bandpass optical filters prior to the second stage SOA remove the out of band ASE noise generated by the first stage SOA and prevent the saturation of the second stage SOA leading to nonlinearities.

TABLE I
OPTICAL LOSS ESTIMATION FOR THE LONGEST CHANNEL
IN THE SIPH SWITCH

Banyan Switch Matrix	Number of MZI stages	Longest waveguide length (mm)	Number of waveguide crossing	Total on-chip loss (dB)	
				Estimation*	Simulation
4×4	2	1.5	1	2.1	1.7
8×8	3	5	4	4.9	4.4
16×16	4	7	11	8.4	7.7
32×32	5	10	26	14.6	13.8
64×64	6	15	57	26.4	25.4

* Data based on building block measurement results.

(a) 16×16 hybrid switch

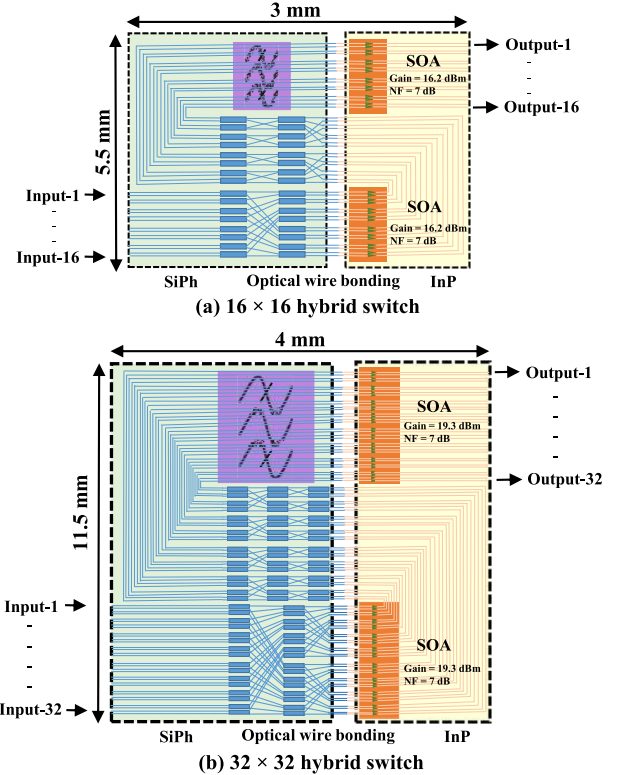(b) 32×32 hybrid switch

Fig. 6. Schematic of the hybrid switches with estimated dimensions. The SiPh bandpass filter removes the remaining out-of-band ASE noise generated by the first InP SOA gain block; (a) 16×16; (b) 32×32.
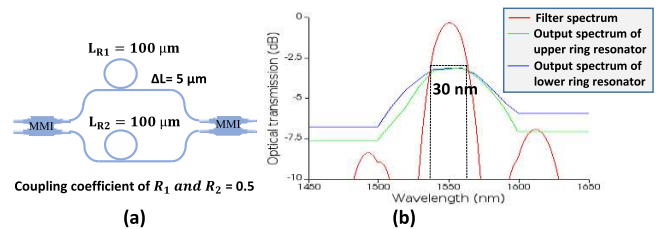

Fig. 7. Optical filter; (a) designed bandpass filter; (b) Optical spectrum with 3 dB bandwidth.

Using the combination of SiPh MZI and micro ring resonators, on-chip bandpass filters have been designed [11], [12]. In our work, we use an asymmetric MZI ($\Delta L = 5$ μm) and two micro ring resonators with 0.5 coupling coefficient shown in fig. 7(a) which exhibits a 30 nm wide bandwidth and an insertion loss below 0.5 dB at 1550 nm central wavelength (fig. 7(b)).

To calculate the noise factor of the proposed hybrid switch, we use the Friis formula that expresses the total noise factor
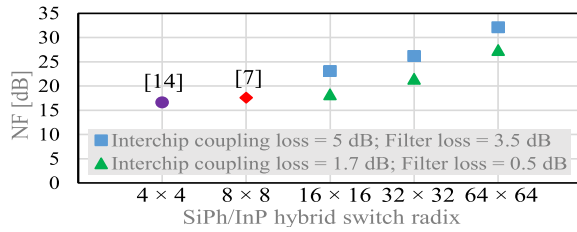
Fig. 8.   Hybrid switch noise figure (NF) versus switch radix.

of multiple cascaded stages:

$$F_{SiPh/InP} = F_1 + \frac{(F_{SOA1} - 1)}{1/L_1} + \frac{(F_2 - 1)}{1/L_1 \times G_{SOA1}}$$
$$+ \frac{(F_{SOA2} - 1)}{1/L_1 \times G_{SOA1} \times 1/L_2}$$
$$+ \frac{(F_3 - 1)}{1/L_1 \times G_{SOA1} \times 1/L_2 \times G_{SOA1}} \quad (1)$$

where, F_1 and L_1 are the noise factor and the aggregate loss of all the cascaded passive elements from the input to the first SOA (i.e., the input coupling to the SiPh chip, the switching elements in SiPh, the inter-chip coupling). F_{SOA1} and G_{SOA1} are the noise factor and gain of the first SOA. F_2 and L_2 are the noise factor and loss of the passive elements between the first and the second SOA (i.e., two inter-chip couplings, the switching elements in the SiPh and the bandpass filter). F_3 is the noise factor of the output coupling. The noise factor of a passive lossy device is identical to its loss (in a linear ratio) [13]. The noise figure (NF) of the hybrid switch is the noise factor expressed in decibel.

Fig. 8 presents the calculated NF for the 16×16 and 32×32 hybrid switches shown in Fig. 6. In calculating the NF, we use the values presented in Table I for the SiPh on-chip loss. The NF of SOAs is 7 dB [7]. We equally distribute the SiPh loss and the InP gain between the first and the second stages. We find the NF for two different scenarios: when the inter-chip coupling is budgeted 1.7 dB and 5 dB; and the filter loss is 0.5 dB and 3.5 dB, respectively. The NF of 4×4 and 8×8 switches are for the single stage gain hybrid switches presented in [14], [7]. Employing the distributed gain design, one can achieve lossless operation of 64×64 switch with NF below 30 dB. Although, the distributed gain design comes with inevitable extra coupling loss, it prevents the SOAs' saturation by dividing the gain between the stages. Considering the proper input signal to the switch, the output OSNR remain above 30 dB is sufficient for low noise data transmission [15]. Larger switch matrices greater than 64×64 with reasonable OSNR can be achieved using enough SOA gain blocks and the NF and output OSNR can be further improved by using an off-chip bandpass filter at the switch output. All the estimations are done based on the longest path of the switching matrix. Changing the bias current, the gain can be tuned accordingly for the shorter paths to prevent the gain saturation.

The electrical power dissipated by each 2×2 MZI switch in 'OFF' state and 'ON' state are 4.8 mW and 34.8 mW, respectively, requiring 30 mW/π-phase shift representing a $V\pi$ of 1.6 V (Fig. 1(d)). The total power consumption in SiPh switch is the summation of the individual power consumption from the thermal phase shifter of the 2×2 MZI switches. If all the switching channels are active the total power (energy) consumption of the 4×4, 8×8 thermal switches are around

139 mW (3.5 pJ/bit) and 417 mW (5.2 pJ/bit), respectively. For 25 dB of optical gain, the SOA gain block needs 115.5 mW electrical power where the biased current is 75 mA, corresponding to 1.54 V voltage [7]. Therefore, for the lossless operation of 16×16, 32×32 and 64×64 hybrid switches, the total power (energy) consumptions are approximately 2.96 W (18.5 pJ/bit), 6.48 W (20.2 pJ/bit) and 14.1 W (22 pJ/bit), respectively, while all the ports are on 'ON' state.

IV. CONCLUSION

In this letter, we experimentally demonstrated 2×2, 4×4 and 8×8 SiPh thermal banyan switches exhibiting low loss and low crosstalk. These MMI based switches show low power penalty and BER below 10^{-10} in payload transmission. We also demonstrated InP-SOA gain block with large gain and low NF compatible to use in a payload data transmission with a high OSNR. This letter proposes a hybrid switching approach in photonic switch design, combining SiPh switch and InP-SOA components, exhibits high scalability, sufficient crosstalk suppression and nearly lossless optical transmission at the output ports. The 64×64 hybrid switch is estimated to exhibit 22 pJ/bit for 10 Gb/s data transmission in the worst case when all building blocks are active.

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